ANALOG DEVICES

Micropower Single-Supply Rail-to-Rail Input/Output Op Amps

OP191/OP291/OP491

FEATURES

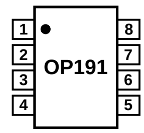
Single-Supply Operation: 2.7 V to 12 V
Wide Input Voltage Range
Rail-to-Rail Output Swing
Low Supply Current: 300 μA/Amp
Wide Bandwidth: 3 MHz
Slew Rate: 0.5 V/μs
Low Offset Voltage: 700 μV
No Phase Reversal

APPLICATIONS

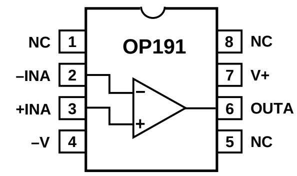
Industrial Process Control
Battery Powered Instrumentation
Power Supply Control and Protection
Telecom
Remote Sensors
Low Voltage Strain Gage Amplifiers
DAC Output Amplifier

OP191/OP291/OP491 PIN CONFIGURATIONS

8-Lead Narrow-Body SO (S Suffix)

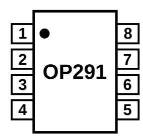


8-Lead Epoxy DIP (P Suffix)

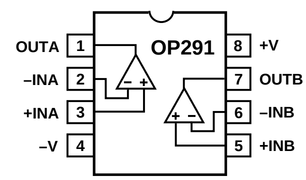


NC = NO CONNECT

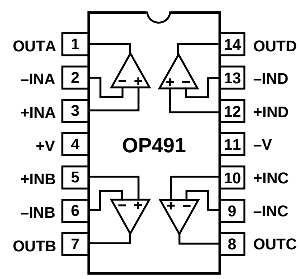
8-Lead Narrow-Body SO (S Suffix)



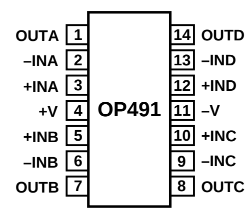
8-Lead Epoxy DIP (P Suffix)



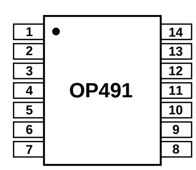
14-Lead Epoxy DIP (P Suffix)



14-Lead SO (S Suffix)



14-Lead TSSOP (RU Suffix)



GENERAL DESCRIPTION

The OP191, OP291 and OP491 are single, dual and quad micropower, single-supply, 3 MHz bandwidth amplifiers featuring rail-to-rail inputs and outputs. All are guaranteed to operate from a 3 volt single supply as well as ±5 volt dual supplies.

Fabricated on Analog Devices' CBCMOS process, the OP191 family has a unique input stage that allows the input voltage to safely extend 10 volts beyond either supply without any phase inversion or latch-up. The output voltage swings to within millivolts of the supplies and continues to sink or source current all the way to the supplies.

Applications for these amplifiers include portable telecom equipment, power supply control and protection, and interface for transducers with wide output ranges. Sensors requiring a rail-to-rail input amplifier include Hall effect, piezo electric, and resistive transducers.

The ability to swing rail-to-rail at both the input and output enables designers to build multistage filters in single-supply systems and maintain high signal-to-noise ratios.

The OP191/OP291/OP491 are specified over the extended industrial (–40°C to +125°C) temperature range. The OP191 single and OP291 dual amplifiers are available in 8-pin plastic DIPs and SO surface mount packages. The OP491 quad is available in 14-pin DIPs and narrow 14-pin SO packages. Consult factory for OP491 TSSOP availability.

REV. 0

One Technology Way, P.O. Box 9106, Norwood. MA 02062-9106, U.S.A.
Tel: 617/329-4700 **Fax: 617/326-8703**

OP191/OP291/OP491–SPECIFICATIONS

ELECTRICAL SPECIFICATIONS (@ V_S = +3.0 V, V_{CM} = 0.1 V, V_O = 1.4 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage OP191G	V_{OS}			80	500	µV
		$-40 \le T_A \le +125°C$			1	mV
OP291/OP491G	V_{OS}			80	700	µV
		$-40 \le T_A \le +125°C$			1.25	mV
Input Bias Current	I_B			30	50	nA
		$-40 \le T_A \le +125°C$			70	nA
Input Offset Current	I_{OS}			0.1	8	nA
		$-40 \le T_A \le +125°C$			16	nA
Input Voltage Range			0		3	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 2.9 V	70	90		dB
		$-40 \le T_A \le +125°C$	65	87		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ , V_O = 0.3 V to 2.7 V	25	70		V/mV
		$-40 \le T_A \le +125°C$		50		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			1.1		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			100		pA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$			20		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 100 kΩ to GND	2.95	2.99		V
		–40°C to +125°C	2.90	2.98		V
		R_L = 2 kΩ to GND	2.8	2.9		V
		–40°C to +125°C	2.70	2.8		V
Output Voltage Low	V_{OL}	R_L = 100 kΩ to V+		4.5	10	mV
		–40°C to +125°C			35	mV
		R_L = 2 kΩ to V+		40	75	mV
		–40°C to +125°C			130	mV
Short Circuit Limit	I_{SC}	Sink/Source	±8.75	±13.5		mA
		–40°C to +125°C	±6.0	±10.5		mA
Open Loop Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		200		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 12 V	80	110		dB
		$-40°C \le T_A \le +125°C$	75	110		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		200	350	µA
		$-40°C \le T_A \le +125°C$		330	480	µA
DYNAMIC PERFORMANCE						
Slew Rate	+SR	R_L = 10 kΩ		0.4		V/µs
Slew Rate	–SR	R_L = 10 kΩ		0.4		V/µs
Full-Power Bandwidth	BW_P	1% Distortion		1.2		kHz
Settling Time	t_S	To 0.01%		22		µs
Gain Bandwidth Product	GBP			3		MHz
Phase Margin	θ_O			45		Degrees
Channel Separation	CS	f = 1 kHz, R_L = 10 kΩ		145		dB
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		2		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		35		$nV/\sqrt{Hz}$
Current Noise Density	i_n			0.8		$pA/\sqrt{Hz}$

Specifications subject to change without notice.

ELECTRICAL SPECIFICATIONS (@ V_S = +5.0 V, V_{CM} = 0.1 V, V_O = 1.4 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage OP191	V_{OS}			80	500	µV
		$-40 \le T_A \le +125°C$			1.0	mV
OP291/OP491	V_{OS}			80	700	µV
		$-40 \le T_A \le +125°C$			1.25	mV
Input Bias Current	I_B			30	50	nA
		$-40 \le T_A \le +125°C$			60	nA
Input Offset Current	I_{OS}			0.1	8	nA
		$-40 \le T_A \le +125°C$			16	nA
Input Voltage Range			0		5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 4.9 V	70	93		dB
		$-40 \le T_A \le +125°C$	65	90		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ , V_O = 0.3 V to 4.7 V	25	70		V/mV
		$-40 \le T_A \le +125°C$		50		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40 \le T_A \le +125°C$		1.1		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			100		pA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$			20		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 100 kΩ to GND	4.95	4.99		V
		–40°C to +125°C	4.90	4.98		V
		R_L = 2 kΩ to GND	4.8	4.85		V
		–40°C to +125°C	4.65	4.75		V
Output Voltage Low	V_{OL}	R_L = 100 kΩ to V+		4.5	10	mV
		–40°C to +125°C			35	mV
		R_L = 2 kΩ to V+		40	75	mV
		–40°C to +125°C			155	mV
Short Circuit Limit	I_{SC}	Sink/Source	±8.75	±13.5		mA
		–40°C to +125°C	±6.0	±10.5		mA
Open Loop Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		200		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 12 V	80	110		dB
		$-40 \le T_A \le +125°C$	75	110		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		220	400	µA
		$-40 \le T_A \le +125°C$		350	500	µA
DYNAMIC PERFORMANCE						
Slew Rate	+SR	R_L = 10 kΩ		0.4		V/µs
Slew Rate	–SR	R_L = 10 kΩ		0.4		V/µs
Full-Power Bandwidth	BW_P	1% Distortion		1.2		kHz
Settling Time	t_S	To 0.01%		22		µs
Gain Bandwidth Product	GBP			3		MHz
Phase Margin	θ_O			45		Degrees
Channel Separation	CS	f = 1 kHz, R_L = 10 kΩ		145		dB
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		2		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		35		$nV/\sqrt{Hz}$
Current Noise Density	i_n			0.8		$pA/\sqrt{Hz}$

NOTES
+5 V specifications are guaranteed by +3 V and ±5 V testing.
Specifications subject to change without notice.

ELECTRICAL SPECIFICATIONS (@ V_O = ±5.0 V, –4.9 V ≤ V_{CM} ≤ +4.9 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage OP191	V_{OS}			80	500	µV
		–40 ≤ T_A ≤ +125°C			1	mV
OP291/OP491	V_{OS}			80	700	µV
		–40 ≤ T_A ≤ +125°C			1.25	mV
Input Bias Current	I_B			30	50	nA
		–40 ≤ T_A ≤ +125°C			70	nA
Input Offset Current	I_{OS}			0.1	8	nA
		–40 ≤ T_A ≤ +125°C			16	nA
Input Voltage Range			–5		+5	V
Common-Mode Rejection	CMR	V_{CM} = ±5 V	75	100		dB
		–40 ≤ T_A ≤ +125°C	67	97		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O = ±4.7 V,	25	70		
		–40 ≤ T_A ≤ +125°C		50		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			1.1		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			100		pA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$			20		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L = 100 kΩ to GND	±4.93	±4.99		V
		–40°C to +125°C	±4.90	±4.98		V
		R_L = 2 kΩ to GND	±4.80	±4.95		V
		–40 ≤ T_A ≤ +125°C	±4.65	±4.75		V
Short Circuit Limit	I_{SC}	Sink/Source	±8.75	±16		mA
		–40°C to +125°C	±6	±13		mA
Open Loop Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		200		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±5 V	80	110		dB
		–40 ≤ T_A ≤ +125°C	70	100		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		260	420	µA
		–40 ≤ T_A ≤ +125°C		390	550	µA
DYNAMIC PERFORMANCE						
Slew Rate	±SR	R_L =10 kΩ		0.5		V/µs
Full-Power Bandwidth	BW_P	1% Distortion		1.2		kHz
Settling Time	t_S	To 0.01%		22		µs
Gain Bandwidth Product	GBP			3		MHz
Phase Margin	θ_O			45		Degrees
Channel Separation	CS	f = 1 kHz		145		dB
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		2		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		35		$nV/\sqrt{Hz}$
Current Noise Density	i_n			0.8		$pA/\sqrt{Hz}$

Specifications subject to change without notice.

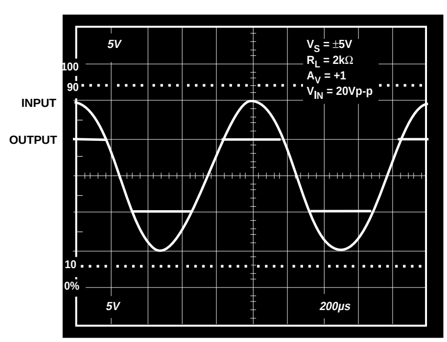


Figure 1. Input and Output with Inputs Overdriven by 5 V

WAFER TEST LIMITS (@ V_S = +3.0 V, V_{CM} = 0.1 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Limit	Units
Offset Voltage	V_{OS}		±300	µV max
Input Bias Current	I_B		50	nA max
Input Offset Current	I_{OS}		8	nA
Input Voltage Range	V_{CM}		V– to V+	V min
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to +2.9 V	70	dB min
Power Supply Rejection Ratio	PSRR	V = 2.7 V to +12 V	80	dB min
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ	50	V/mV min
Output Voltage High	V_{OH}	R_L = 2 kΩ to GND	2.8	V min
Output Voltage Low	V_{OL}	R_L = 2 kΩ to V+	75	mV max
Supply Current/Amplifier	I_{SY}	V_O = 0 V, R_L = ∞	350	µA max

NOTE
Electrical tests and wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . +16 V
Input Voltage . . . . GND to V_S + 10 V
Differential Input Voltage . . . . 7 V
Output Short-Circuit Duration to GND . . . . Indefinite
Storage Temperature Range
P, S, RU Packages . . . . –65°C to +150°C
Operating Temperature Range
OP191/OP291/OP491G . . . . –40°C to +125°C
Junction Temperature Range
P, S, RU Packages . . . . –65°C to +150°C
Lead Temperature Range (Soldering 60 sec) . . . . +300°C

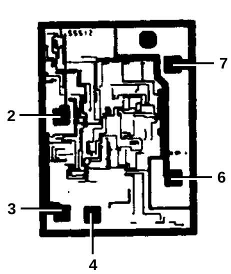
Package Type	θ_{JA}[2]	θ_{JC}	Units
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SOIC (S)	158	43	°C/W
14-Pin Plastic DIP (P)	76	33	°C/W
14-Pin SOIC (S)	120	36	°C/W
14-Pin TSSOP (RU)	180	35	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]θ_{JA} is specified for the worst case conditions; i.e., θ_{JA} is specified for device in socket for P-DIP packages; θ_{JA} is specified for device soldered in circuit board for TSSOP and SOIC packages.

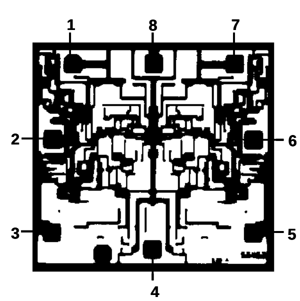
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
OP191GP	–40°C to +125°C	8-Pin Plastic DIP	N-8
OP191GS	–40°C to +125°C	8-Pin SOIC	SO-8
OP191GBC	+25°C	DICE	
OP291GP	–40°C to +125°C	8-Pin Plastic DIP	N-8
OP291GS	–40°C to +125°C	8-Pin SOIC	SO-8
OP291GBC	+25°C	DICE	
OP491GP	–40°C to +125°C	14-Pin Plastic DIP	N-14
OP491GS	–40°C to +125°C	14-Pin SOIC	SO-14
OP491HRU	–40°C to +125°C	14-Pin TSSOP	RU-14
OP491GBC	+25°C	DICE	

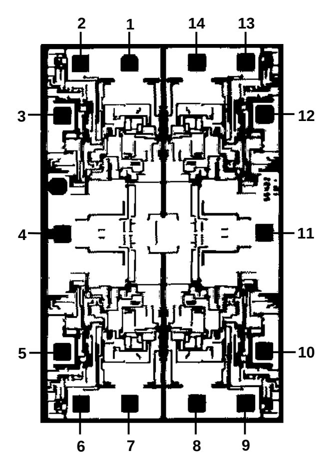
DICE CHARACTERISTICS



OP191 Die Size 0.047 × 0.066 Inch, 3,102 Sq. Mils. Substrate (Die Backside) Is Connected to V+. Transistor Count, 74.



OP291 Die Size 0.070 × 0.070 Inch, 4,900 Sq. Mils. Substrate (Die Backside) Is Connected to V+. Transistor Count, 146



OP491 Die Size 0.070 × 0.110 Inch, 7,700 Sq. Mils. Substrate (Die Backside) Is Connected to V+. Transistor Count, 290.

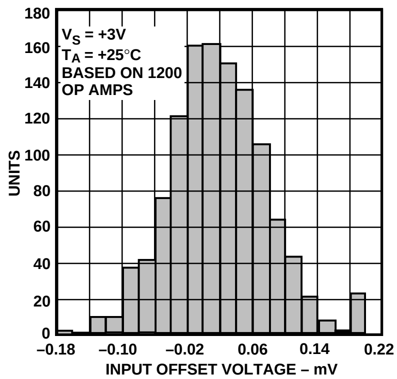


Figure 2. OP291 Input Offset Voltage Distribution, V_S = +3 V

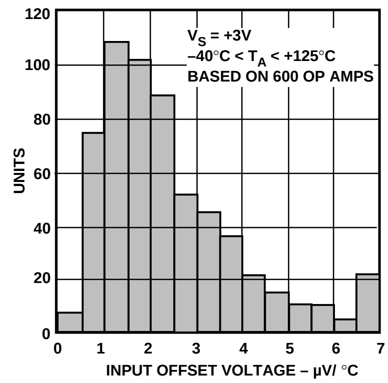


Figure 3. OP291 Input Offset Voltage Drift Distribution, V_S = +3 V

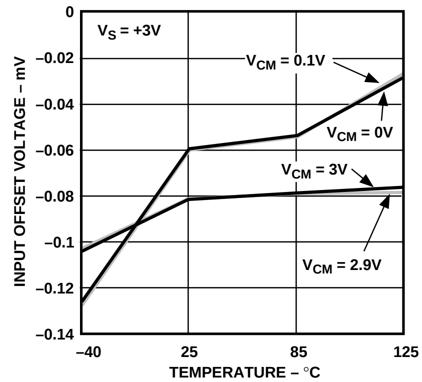


Figure 4. Input Offset Voltage vs. Temperature, V_S = +3 V

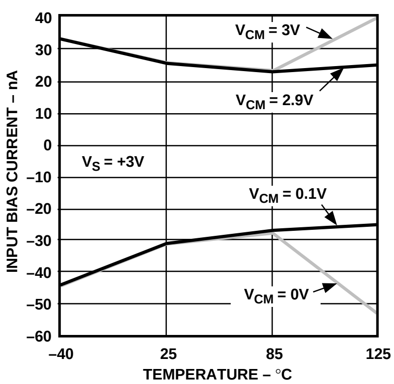


Figure 5. Input Bias Current vs. Temperature, V_S = +3 V

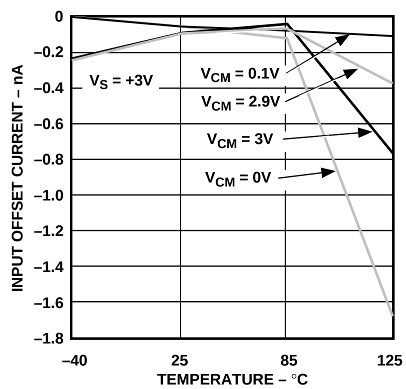


Figure 6. Input Offset Current vs. Temperature, V_S = +3 V

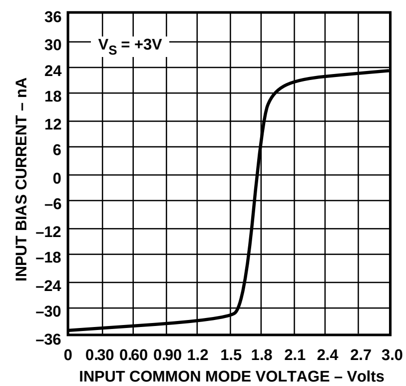


Figure 7. Input Bias Current vs. Common-Mode Voltage, V_S = +3 V

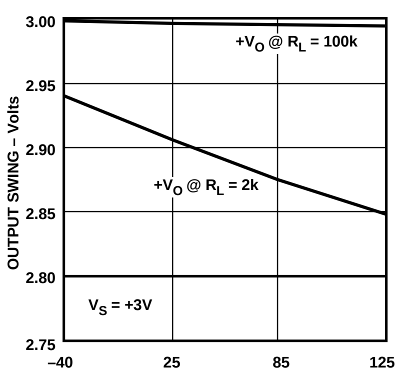


Figure 8. Output Voltage Swing vs. Temperature, V_S = +3 V

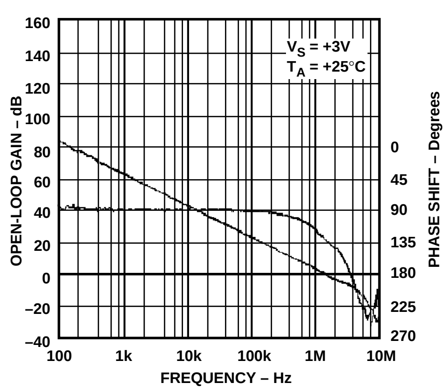


Figure 9. Open-Loop Gain & Phase vs. Frequency, V_S = +3 V

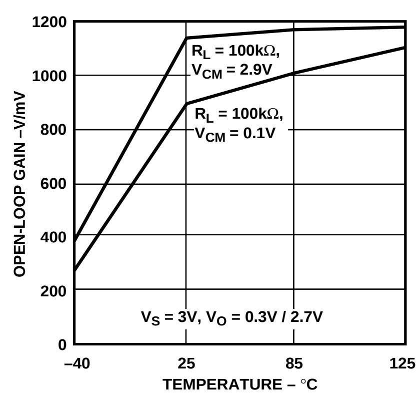


Figure 10. Open-Loop Gain vs. Temperature, V_S = +3 V

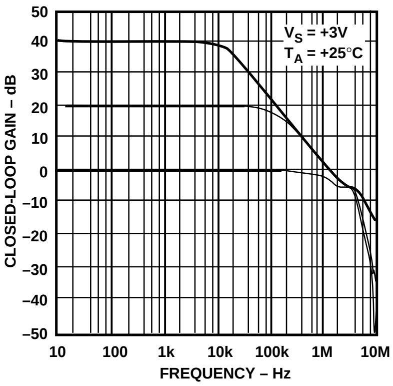


Figure 11. Closed-Loop Gain vs. Frequency, V_S = +3 V

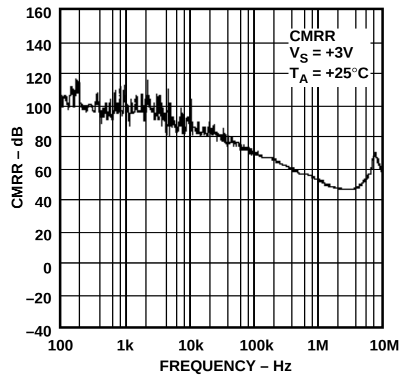


Figure 12. CMRR vs. Frequency, V_S = +3 V

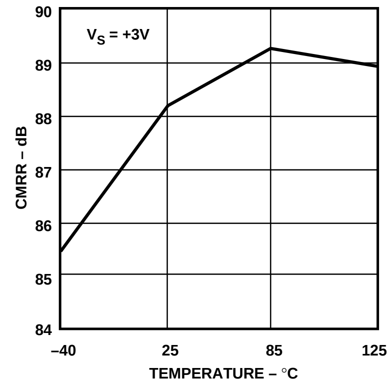


Figure 13. CMRR vs. Temperature, V_S = +3 V

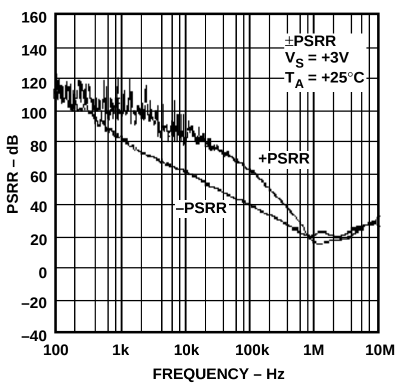


Figure 14. PSRR vs. Frequency, V_S = +3 V

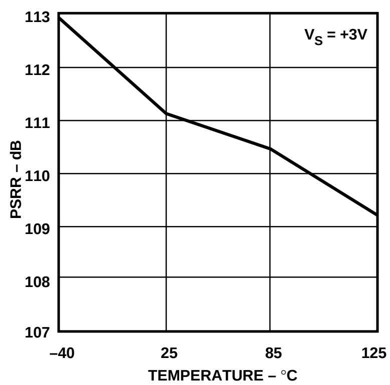


Figure 15. PSRR vs. Temperature, V_S = +3 V

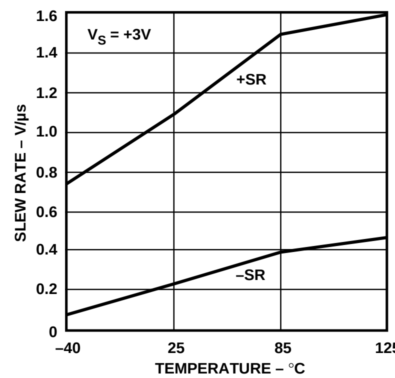


Figure 16. Slew Rate vs. Temperature, V_S = +3 V

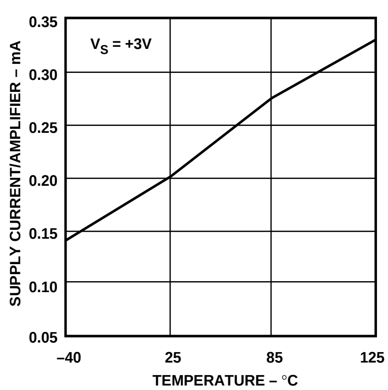


Figure 17. Supply Current vs. Temperature, V_S = +3 V, +5 V, ±5 V

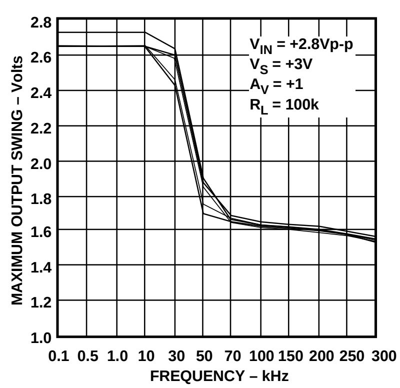


Figure 18. Maximum Output Swing vs. Frequency, V_S = +3 V

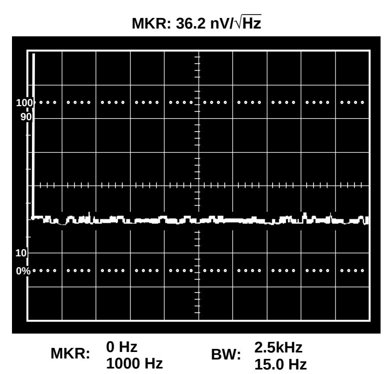


Figure 19. Voltage Noise Density, V_S = +3 V to ±5 V, A_{VO} = 1000

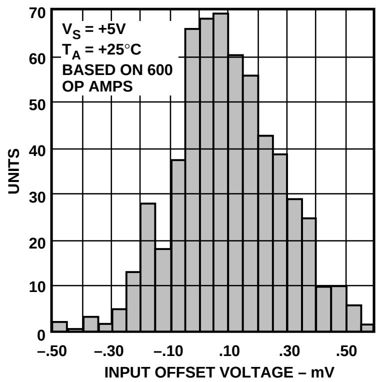


Figure 20. OP291 Input Offset Voltage Distribution, V_S = +5 V

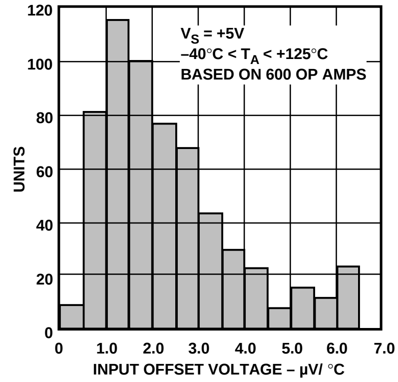


Figure 21. OP291 Input Offset Voltage Drift Distribution, V_S = +5 V

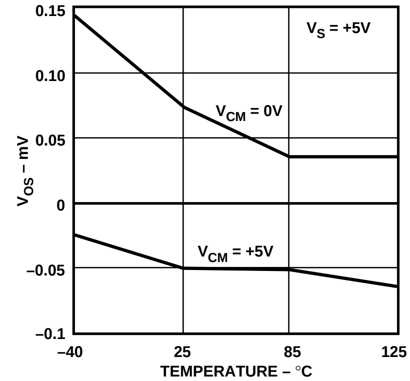


Figure 22. Input Offset Voltage vs. Temperature, V_S = +5 V

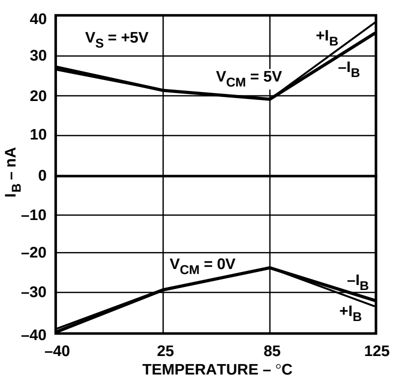


Figure 23. Input Bias Current vs. Temperature, V_S = +5 V

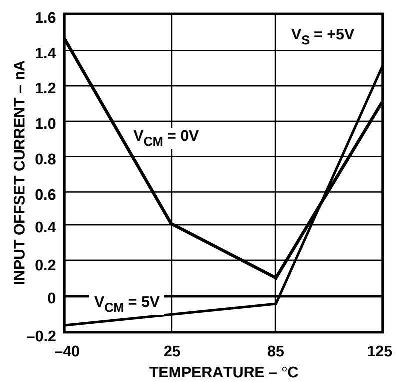


Figure 24. Input Offset Current vs. Temperature, V_S = +5 V

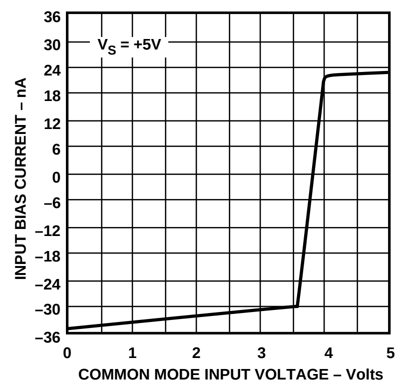


Figure 25. Input Bias Current vs. Common-Mode Voltage, V_S = +5 V

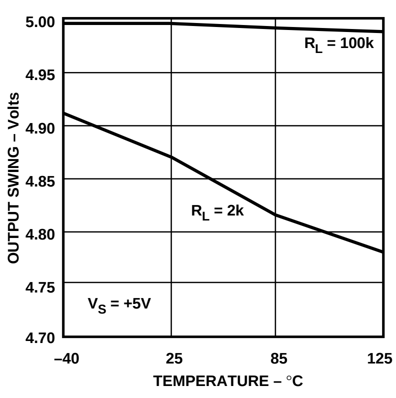


Figure 26. Output Voltage Swing vs. Temperature, V_S = +5 V

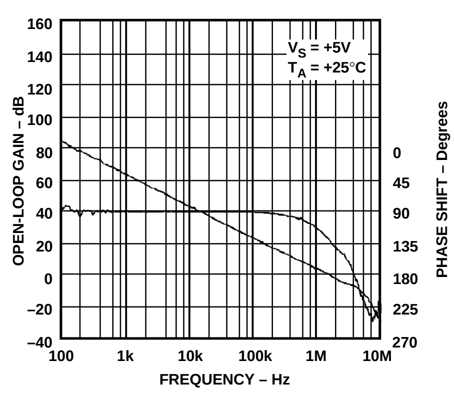


Figure 27. Open-Loop Gain & Phase vs. Frequency, V_S = +5 V

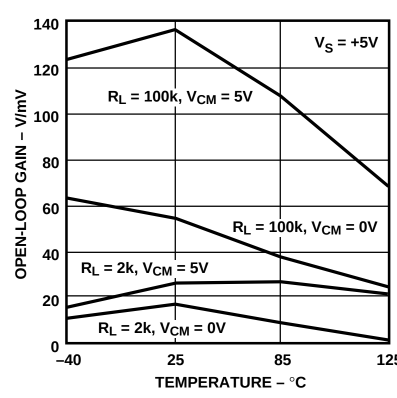


Figure 28. Open-Loop Gain vs. Temperature, V_S = +5 V

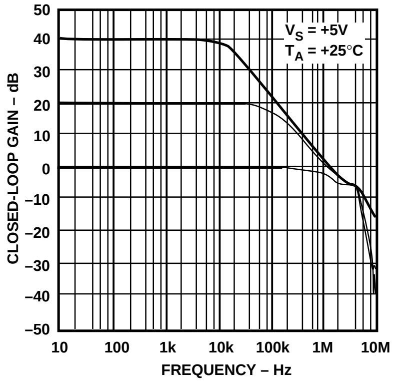


Figure 29. Closed-Loop Gain vs. Frequency, V_S = +5 V

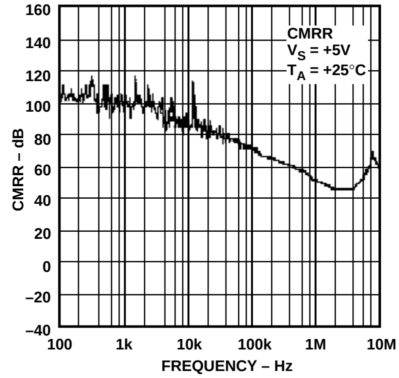


Figure 30. CMRR vs. Frequency, V_S = +5 V

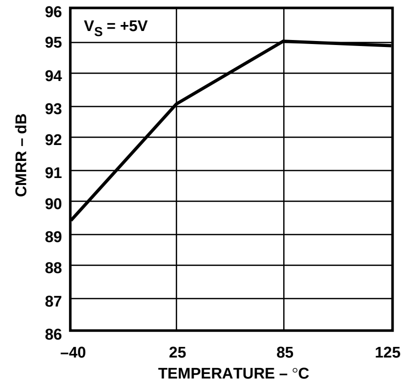


Figure 31. CMRR vs. Temperature, V_S = +5 V

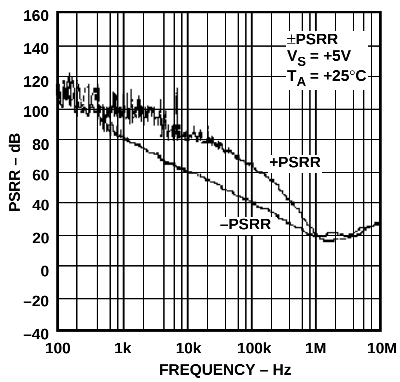


Figure 32. PSRR vs. Frequency, V_S = +5 V

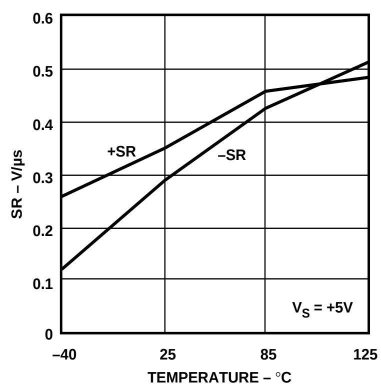


Figure 33. OP291 Slew Rate vs. Temperature, V_S = +5 V

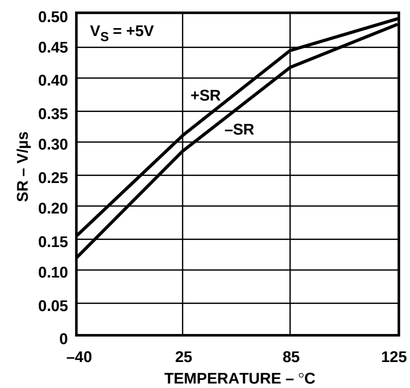


Figure 34. OP491 Slew Rate vs. Temperature, V_S = +5 V

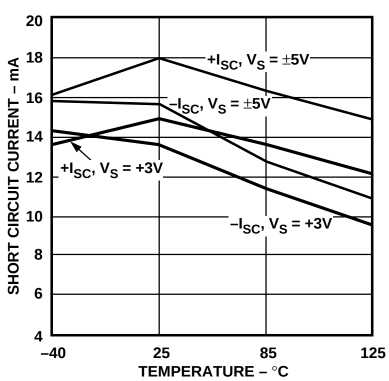


Figure 35. Short Circuit Current vs. Temperature, V_S = +3 V, +5 V, ±5 V

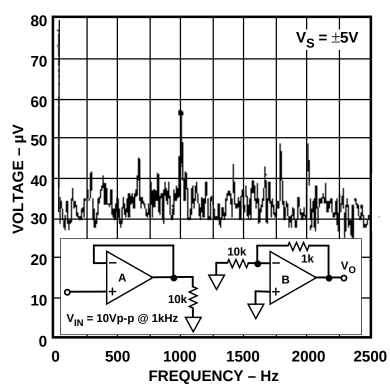


Figure 36. Channel Separation, V_S = ±5 V

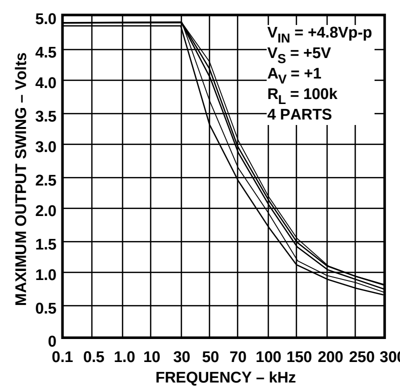


Figure 37. Maximum Output Swing vs. Frequency, V_S = +5 V

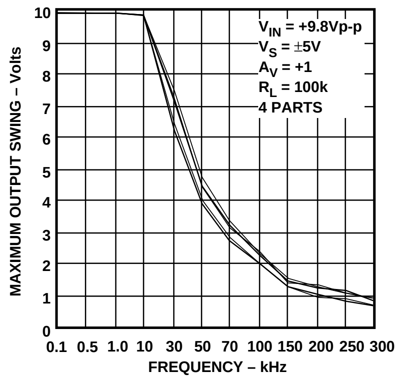


Figure 38. Maximum Output Swing vs. Frequency, $V_S = \pm 5$ V

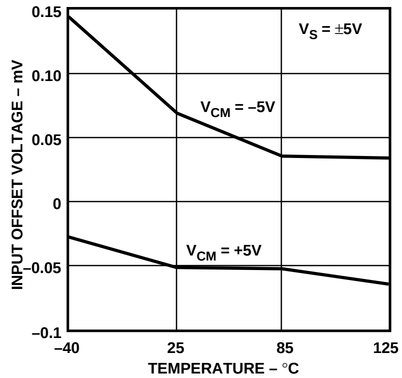


Figure 39. Input Offset Voltage vs. Temperature, $V_S = \pm 5$ V

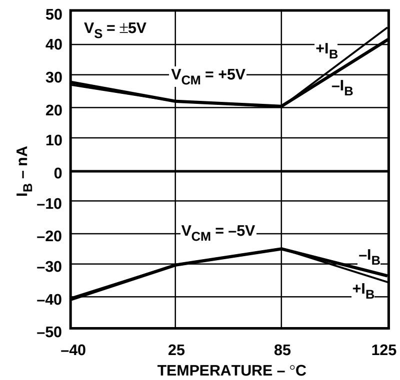


Figure 40. Input Bias Current vs. Temperature, $V_S = \pm 5$ V

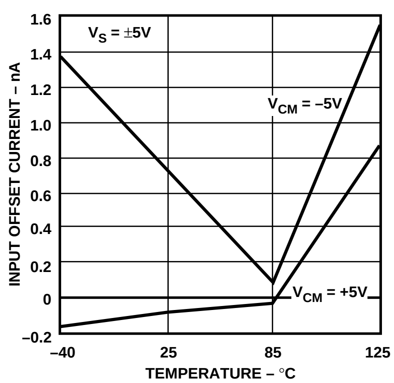


Figure 41. Input Offset Current vs. Temperature, $V_S = \pm 5$ V

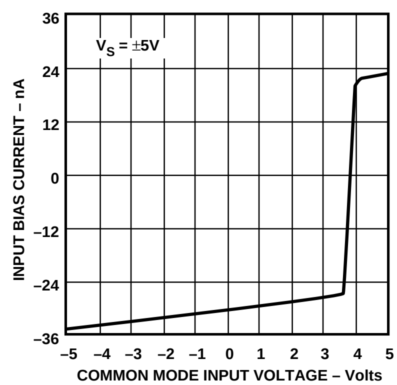


Figure 42. Input Bias Current vs. Common-Mode Voltage, $V_S = \pm 5$ V

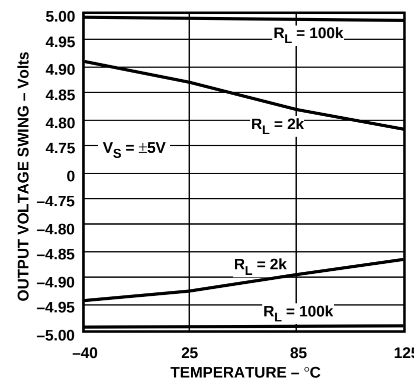


Figure 43. Output Voltage Swing vs. Temperature, $V_S = \pm 5$ V

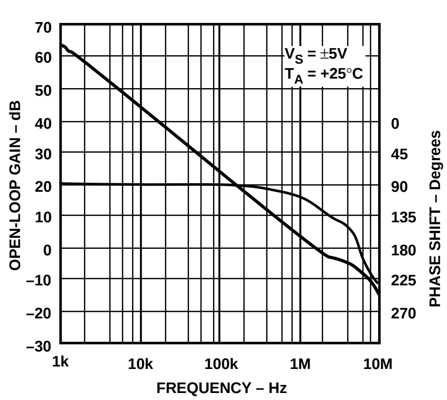


Figure 44. Open-Loop Gain & Phase vs. Frequency, $V_S = \pm 5$ V

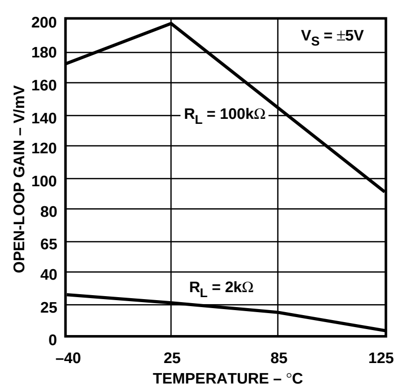


Figure 45. Open-Loop Gain vs. Temperature, $V_S = \pm 5$ V

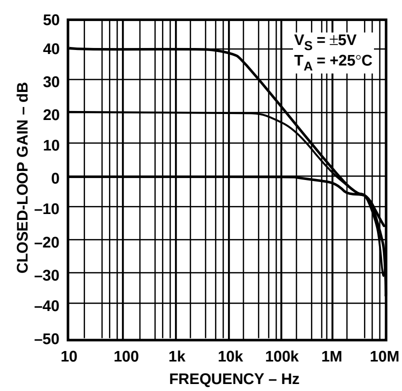


Figure 46. Closed-Loop Gain vs. Frequency, $V_S = \pm 5$ V

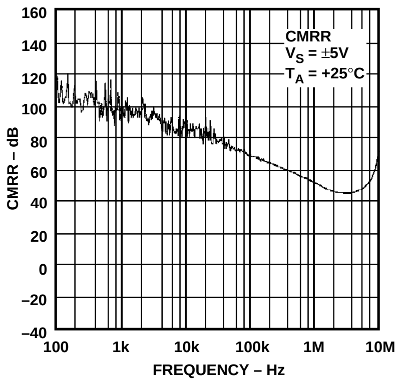


Figure 47. CMRR vs. Frequency, $V_S = \pm 5$ V

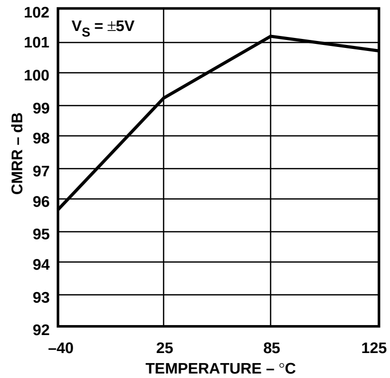


Figure 48. CMRR vs. Temperature, $V_S = \pm 5$ V

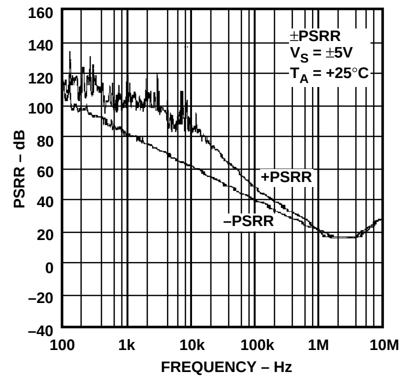


Figure 49. PSRR vs. Frequency, $V_S = \pm 5$ V

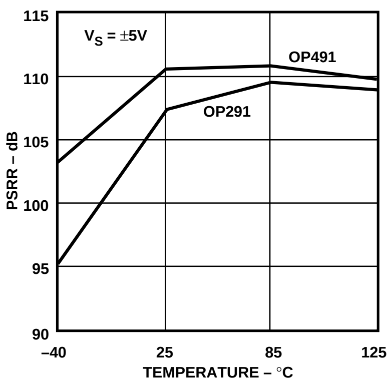


Figure 50. OP291/OP491 PSRR vs. Temperature, $V_S = \pm 5$ V

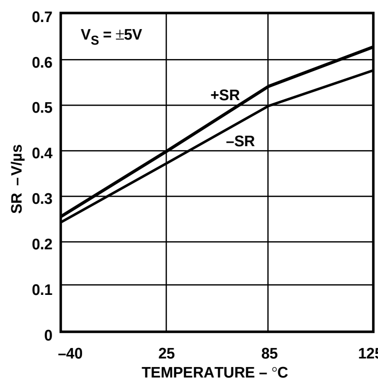


Figure 51. Slew Rate vs. Temperature, $V_S = \pm 5$ V

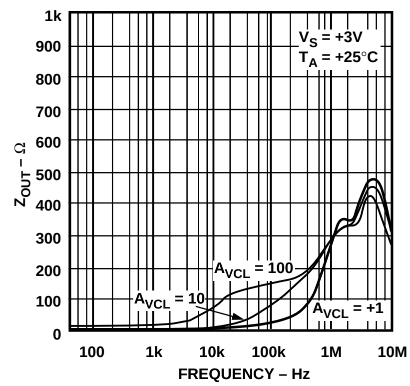


Figure 52. Output Impedance vs. Frequency

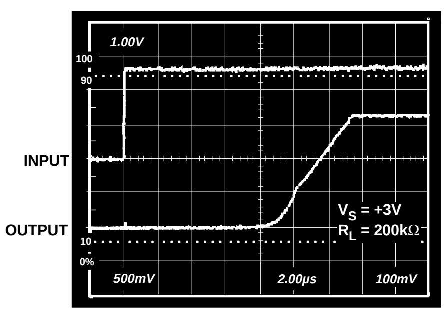


Figure 53. Large Signal Transient Response, $V_S = +3$ V

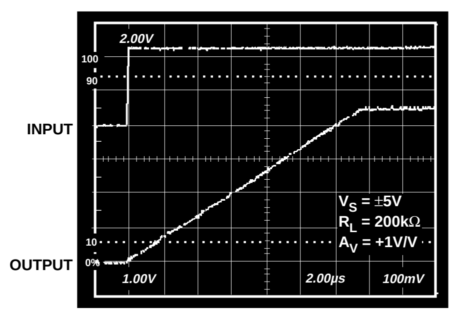


Figure 54. Large Signal Transient Response, $V_S = \pm 5$ V

FUNCTIONAL DESCRIPTION

The OP191/OP291/OP491 are single supply, micropower amplifiers featuring rail-to-rail inputs and outputs. In order to achieve wide input and output ranges, these amplifiers employ unique input and output stages. As the simplified schematic shows (Figure 55), the input stage is actually comprised of two differential pairs, a PNP pair and an NPN pair. These two stages do not actually work in parallel. Instead, only one or the other stage is on for any given input signal level. The PNP stage (transistors Q1 and Q2) is required to ensure that the amplifier remains in the linear region when the input voltage approaches and reaches the negative rail. On the other hand, the NPN stage (transistors Q5 and Q6) is needed for input voltages up to and including the positive rail.

For the majority of the input common-mode range, the PNP stage is active, as is evidenced by examining the graph of Input Bias Current vs. Common-Mode Voltage. Notice that the bias current switches direction at approximately 1.2 volts to 1.3 volts below the positive rail. At voltages below this, the bias current flows out of the OP291, indicating a PNP input stage. Above this voltage, however, the bias current enters the device, revealing the NPN stage. The actual mechanism within the amplifier for switching between the input stages is comprised of the transistors Q3, Q4, and Q7. As the input common-mode voltage increases, the emitters of Q1 and Q2 follow that voltage plus a diode drop. Eventually the emitters of Q1 and Q2 are high enough to turn Q3 on. This diverts the 8 μA of tail current away from the PNP input stage, turning it off. Instead, the current is mirrored through Q4 and Q7 to activate the NPN input stage.

Notice that the input stage includes 5 kΩ series resistors and differential diodes, a common practice in bipolar amplifiers to protect the input transistors from large differential voltages. These diodes will turn on whenever the differential voltage exceeds approximately 0.6 V. In this condition, current will flow between the input pins, limited only by the two 5 kΩ resistors. Being aware of this characteristic is important in circuits where the amplifier may be operated open-loop, such as a comparator. Evaluate each circuit carefully to make sure that the increase in current does not affect the performance.

The output stage of the OP191 family uses a PNP and an NPN transistor as do most output stages; however, the output transistors, Q32 and Q33, are actually connected with their collectors to the output pin to achieve the rail-to-rail output swing. As the output voltage approaches either the positive or negative rail, these transistors begin to saturate. Thus, the final limit on output voltage is the saturation voltage of these transistors, which is about 50 mV. The output stage does have inherent gain arising from the collectors and any external load impedance. Because of this, the open-loop gain of the amplifier is dependent on the load resistance.

Input Overvoltage Protection

As with any semiconductor device, whenever the condition exists for the input to exceed either supply voltage, attention needs to be paid to the input overvoltage characteristic. When an overvoltage occurs, the amplifier could be damaged depending on the voltage level and the magnitude of the fault current. Figure 56 shows the characteristic for the OP191 family. This graph was generated with the power supplies at ground and a curve tracer connected to the input. As can be seen, when the input voltage exceeds either supply by more than 0.6 V, internal pn-junctions energize allowing current to flow from the input to the supplies. As described above, the OP291/OP491 does have 5 kΩ resistors in series with each input, which helps limit the current. Calculating the slope of the current versus voltage in the graph confirms the 5 kΩ resistor.

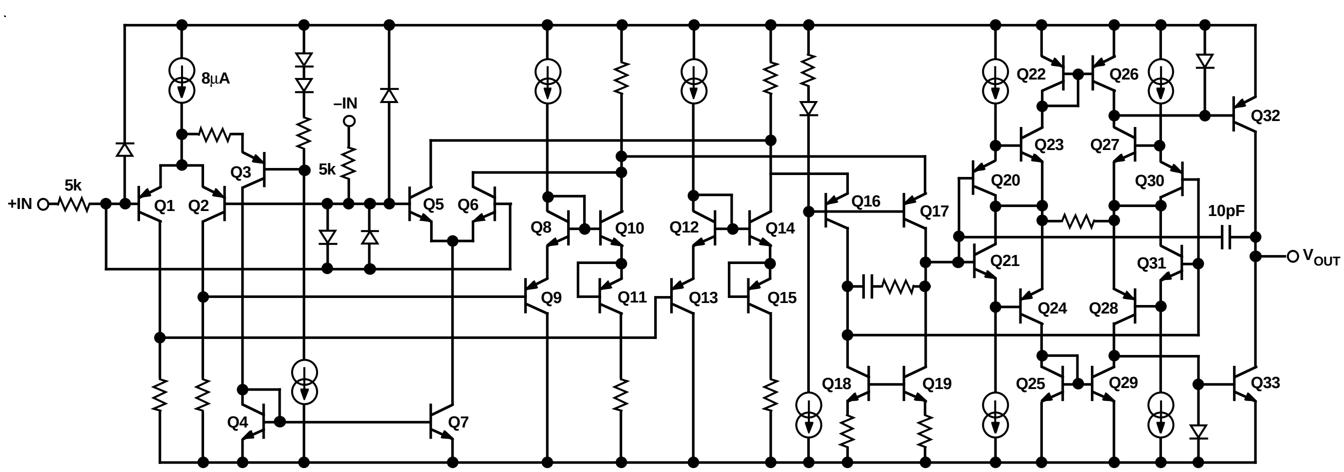


Figure 55. Simplified Schematic

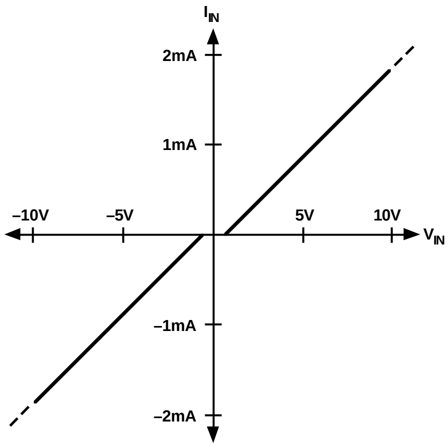


Figure 56. Input Overvoltage Characteristics

This input current is not inherently damaging to the device as long as it is limited to 5 mA or less. In the case shown, for an input of 10 V over the supply, the current is limited to 1.8 mA. If the voltage is large enough to cause more than 5 mA of current to flow, then an external series resistor should be added. The size of this resistor is calculated by dividing the maximum overvoltage by 5 mA and subtracting the internal 5 kΩ resistor. For example, if the input voltage could reach 100 V, the external resistor should be (100 V/5 mA) –5 k = 15 kΩ. This resistance should be placed in series with either or both inputs if they are subjected to the overvoltages. For more information on general overvoltage characteristics of amplifiers refer to the *1993 System Applications Guide*, available from the Analog Devices Literature Center.

Output Voltage Phase Reversal

Some operational amplifiers designed for single-supply operation exhibit an output voltage phase reversal when their inputs are driven beyond their useful common-mode range. Typically for single-supply bipolar op amps, the negative supply determines the lower limit of their common-mode range. With these devices, external clamping diodes, with the anode connected to ground and the cathode to the inputs, prevent input signal excursions from exceeding the device's negative supply (i.e., GND), preventing a condition which could cause the output voltage to change phase. JFET-input amplifiers may also exhibit phase reversal, and, if so, a series input resistor is usually required to prevent it.

The OP191 family is free from reasonable input voltage range restrictions due to its novel input structure. In fact, the input signal can exceed the supply voltage by a significant amount without causing damage to the device. As illustrated in Figure 57, the OP191 family can safely handle a 20 V p-p input signal on ±5 V supplies without exhibiting any sign of output voltage phase reversal or other anomalous behavior. Thus no external clamping diodes are required.

Overdrive Recovery

The overdrive recovery time of an operational amplifier is the time required for the output voltage to recover to its linear region from a saturated condition. This recovery time is important in applications where the amplifier must recover quickly after a large transient event, such as a comparator. The circuit shown in Figure 58 was used to evaluate the OP191 family's overload recovery time. The OP191 family takes approximately 8 µs to recover from positive saturation and approximately 6.5 µs to recover from negative saturation.

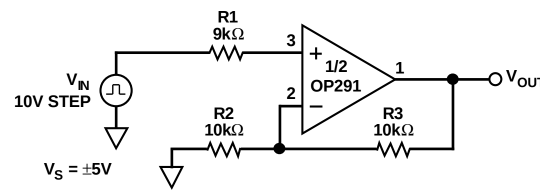


Figure 58. Overdrive Recovery Time Test Circuit

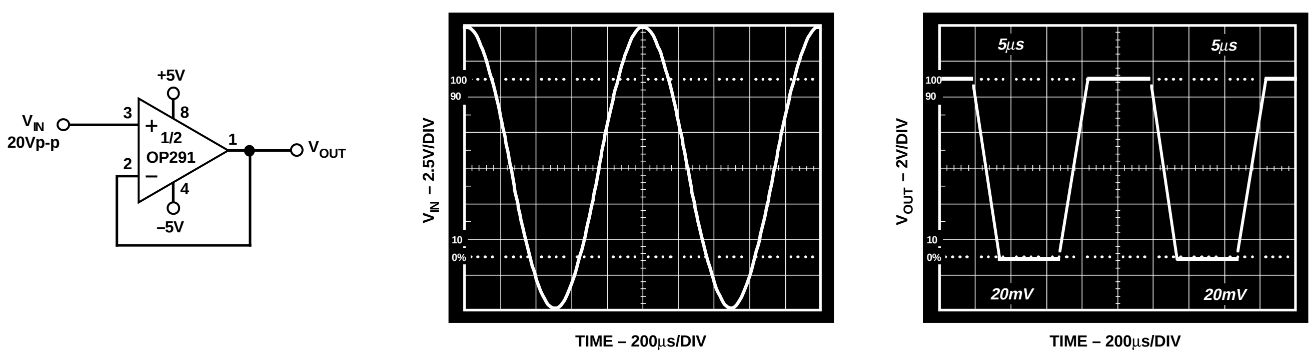


Figure 57. Output Voltage Phase Reversal Behavior

APPLICATIONS

Single +3 V Supply, Instrumentation Amplifier

The OP291's low supply current and low voltage operation make it ideal for battery powered applications such as the instrumentation amplifier shown in Figure 59. The circuit utilizes the classic two op amp instrumentation amplifier topology, with four resistors to set the gain. The equation is simply that of a noninverting amplifier as shown in the figure. The two resistors labeled R1 should be closely matched to each other as well as both resistors labeled R2 to ensure good common-mode rejection performance. Resistor networks ensure the closest matching as well as matched drifts for good temperature stability. Capacitor C1 is included to limit the bandwidth and, therefore, the noise in sensitive applications. The value of this capacitor should be adjusted depending on the desired closed-loop bandwidth of the instrumentation amplifier. The RC combination creates a pole at a frequency equal to $1/(2\pi \times R1C1)$. If AC-CMRR is critical, than a matched capacitor to C1 should be included across the second resistor labeled R1.

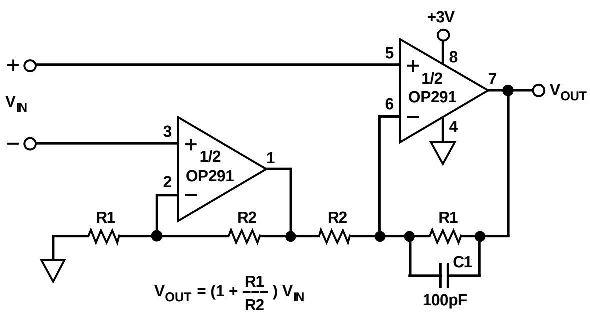


Figure 59. Single +3 V Supply Instrumentation Amplifier

Because the OP291 accepts rail-to-rail inputs, the input common-mode range includes both ground and the positive supply of 3 V. Furthermore, the rail-to-rail output range ensures the widest signal range possible and maximizes the dynamic range of the system. Also, with its low supply current of 300 µA/device, this circuit consumes a quiescent current of only 600 µA, yet still exhibits a gain bandwidth of 3 MHz.

A question may arise about other instrumentation amplifier topologies for single supply applications. For example, a variation on this topology adds a fifth resistor between the two inverting inputs of the op amps for gain setting. While that topology works well in dual supply applications, it is inherently not appropriate for single supply circuits. The same could be said for the traditional three op amp instrumentation amplifier. In both cases, the circuits simply will not work in single supply situations unless a false ground between the supplies is created.

Single Supply RTD Amplifier

The circuit in Figure 60 uses three op amps of the OP491 to develop a bridge configuration for an RTD amplifier that operates from a single +5 V supply. The circuit takes advantage of the OP491's wide output swing range to generate a high bridge excitation voltage of 3.9 V. In fact, because of the rail-to-rail output swing, this circuit will work with supplies as low as 4.0 V. Amplifier A1 servos the bridge to create a constant excitation current in conjunction with the AD589, a 1.235 V precision reference. The op amp maintains the reference voltage across the parallel combination of the 6.19 kΩ and 2.55 MΩ resistor, which generates a 200 µA current source. This current splits evenly and flows through both halves of the bridge. Thus, 100 µA flows through the RTD to generate an output voltage based on its resistance. A 3-wire RTD is used to balance the line resistance in both 100 Ω legs of the bridge to improve accuracy.

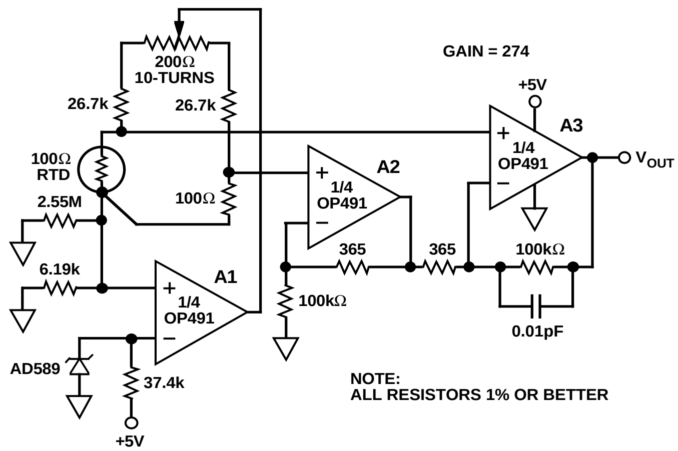


Figure 60. Single Supply RTD Amplifier

Amplifiers A2 and A3 are configured in the two op amp IA discussed above. Their resistors are chosen to produce a gain of 274, such that each 1°C increase in temperature results in a 10 mV change in the output voltage, for ease of measurement. A 0.01 µF capacitor is included in parallel with the 100 kΩ resistor on amplifier A3 to filter out any unwanted noise from this high gain circuit. This particular RC combination creates a pole at 1.6 kHz.

A +2.5 V Reference from a +3 V Supply

In many single-supply applications, the need for a 2.5 V reference often arises. Many commercially available monolithic 2.5 V references require at least a minimum operating supply voltage of 4 V. The problem is exacerbated when the minimum operating system supply voltage is + 3 V. The circuit illustrated in Figure 61 is an example of a +2.5 V that operates from a single +3 V supply. The circuit takes advantage of the OP291's rail-to-rail input and output voltage ranges to amplify an AD589's 1.235 V output to +2.5 V. The OP291's low TCV_{OS} of 1 μV/°C helps to maintain an output voltage temperature coefficient of less than 200 ppm/°C. The circuit's overall temperature coefficient is dominated by R2 and R3's temperature coefficient. Lower tempco resistors are recommended. The entire circuit draws less than 420 μA from a +3 V supply at +25°C.

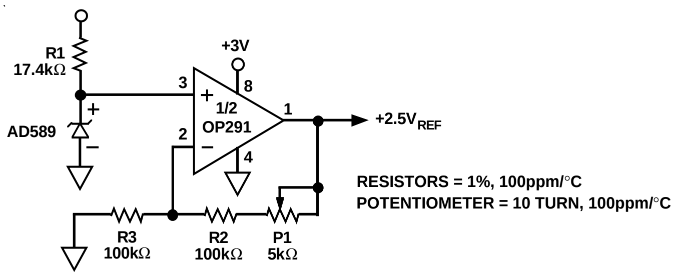


Figure 61. A +2.5 V Reference that Operates on a Single +3 V Supply

+5 V Only, 12-Bit DAC Swings Rail-to-Rail

The OP191 family is ideal for use with a CMOS DAC to generate a digitally controlled voltage with a wide output range. Figure 62 shows the DAC8043 used in conjunction with the AD589 to generate a voltage output from 0 V to 1.23 V The DAC is actually operated in "voltage switching" mode where the reference is connected to the current output, I_{OUT}, and the output voltage is taken from the V_{REF} pin. This topology is inherently noninverting as opposed to the classic current output mode, which is inverting and, therefore, unsuitable for single supply.

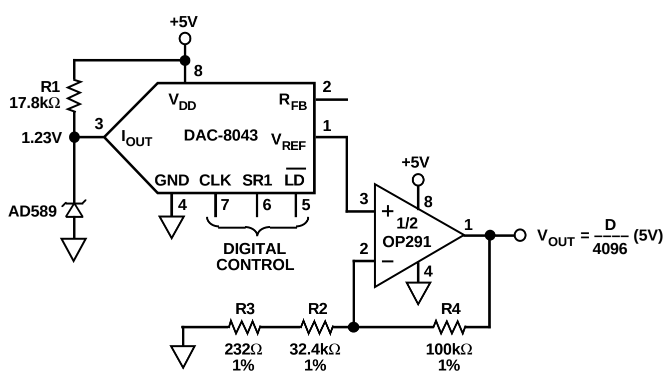


Figure 62. +5 V Only, 12-Bit DAC Swings Rail-to-Rail

The OP291 serves two functions. First, it is required to buffer the high output impedance of the DAC's V_{REF} pin, which is on the order of 10 kΩ. The op amp provides a low impedance output to drive any following circuitry. Secondly, the op amp amplifies the output signal to provide a rail-to-rail output swing. In this particular case, the gain is set to 4.1 to generate a 5.0 V output when the DAC is at full scale. If other output voltage ranges are needed, such as 0 to 4.095, the gain can easily be adjusted by altering the value of the resistors.

A High Side Current Monitor

In the design of power supply control circuits, a great deal of design effort is focused on ensuring a pass transistor's long-term reliability over a wide range of load current conditions. As a result, monitoring and limiting device power dissipation is of prime importance in these designs. The circuit illustrated in Figure 63 is an example of a +5 V, single-supply high side current monitor that can be incorporated into the design of a voltage regulator with fold-back current limiting or a high current power supply with crowbar protection. This design uses an OP291's rail-to-rail input voltage range to sense the voltage drop across a 0.1 Ω current shunt. A p-channel MOSFET used as the feedback element in the circuit converts the op amp's differential input voltage into a current. This current is then applied to R2 to generate a voltage that is a linear representation of the load current. The transfer equation for the current monitor is given by:

$$Monitor\ \ Output\ = R2 \times \left(\frac{R_{SENSE}}{R1}\right) \times I_L$$

For the element values shown, the Monitor Output's transfer characteristic is 2.5 V/A.

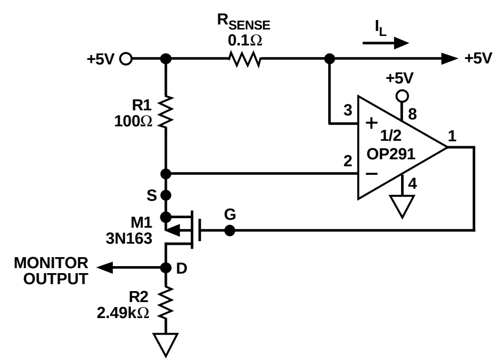


Figure 63. A High-Side Load Current Monitor

A +3 V, Cold Junction Compensated Thermocouple Amplifier

The OP291's low supply operation makes it ideal for +3 V battery powered applications such as the thermocouple amplifier shown in Figure 64. The K-type thermocouple terminates in an isothermal block where the junctions' ambient temperature is continuously monitored using a simple 1N914 diode. The diode corrects the thermal EMF generated in the junctions by feeding a small voltage, scaled by the 1.5 MΩ and 475 Ω resistors, to the op amp.

To calibrate this circuit, immerse the thermocouple measuring junction in a 0°C ice bath, and adjust the 500 Ω pot to zero volts out. Next, immerse the thermocouple in a 250°C temperature bath or oven and adjust the Scale Adjust pot for an output voltage of 2.50 V. Within this temperature range, the K-type thermocouple is accurate to within ±3°C without linearization.

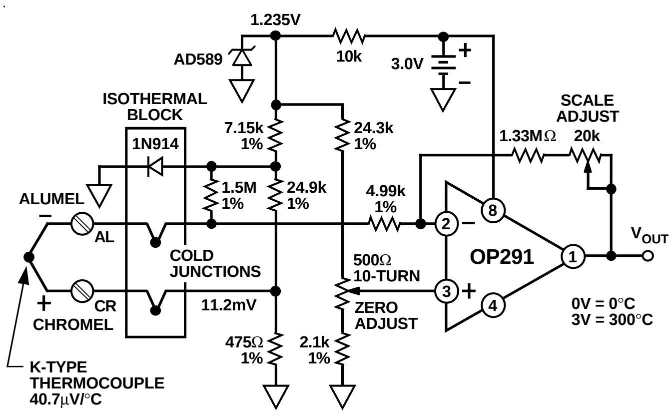


Figure 64. A 3 V, Cold Junction Compensated Thermocouple Amplifier

Single Supply, Direct Access Arrangement for Modems

An important building block in modems is the telephone line interface. In the circuit shown in Figure 65, a direct access arrangement is utilized for transmitting and receiving data from the telephone line. Amplifier A1 is the receiving amplifier, and amplifiers A2 and A3 are the transmitters. The forth amplifier, A4, generates a pseudo ground half way between the supply voltage and ground. This pseudo ground is needed for the ac coupled bipolar input signals.

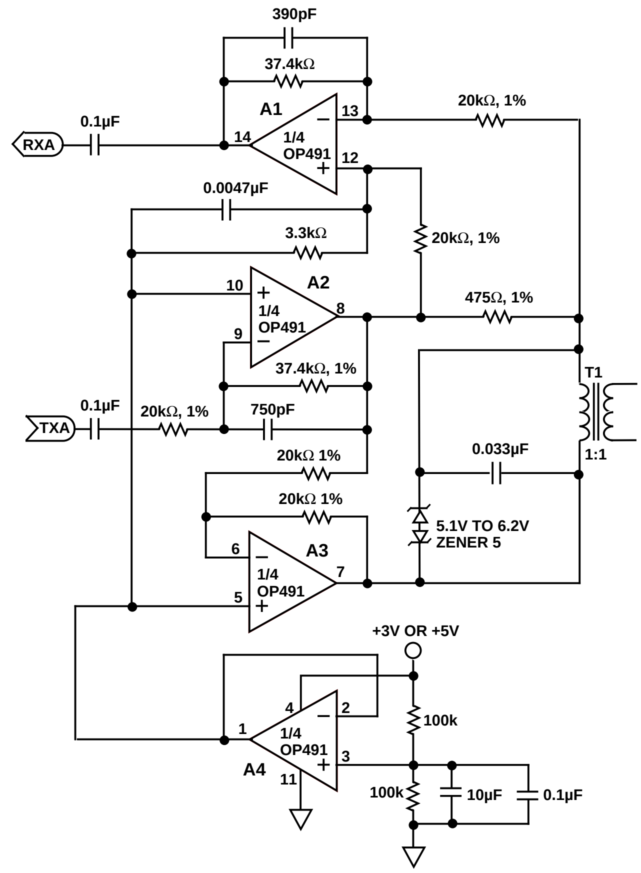


Figure 65. Single Supply Direct Access Arrangement for Modems

The transmit signal, TXA, is inverted by A2 and then reinverted by A3 to provide a differential drive to the transformer, where each amplifier supplies half the drive signal. This is needed because of the smaller swings associated with a single supply as opposed to a dual supply. Amplifier A1 provides some gain for the received signal, and it also removes the transmit signal present at the transformer from the receive signal. To do this, the drive signal from A2 is also fed to the noninverting input of A1 to cancel the transmit signal from the transformer. The OP491's bandwidth of 3 MHz and rail-to-rail output swings ensures that it can provide the largest possible drive to the transformer at the frequency of transmission.

A +3 V, 50 Hz/60 Hz Active Notch Filter with False Ground

To process ac signals in a single-supply system, it is often best to use a false-ground biasing scheme. A circuit that uses this approach is illustrated in Figure 66. In this circuit, a false-ground circuit biases an active notch filter used to reject 50 Hz/60 Hz power line interference in portable patient monitoring equipment. Notch filters are quite commonly used to reject power line frequency interference which often obscures low frequency physiological signals, such as heart rates, blood pressure readings, EEGs, EKGs, etcetera. This notch filter effectively squelches 60 Hz pickup at a filter Q of 0.75. Substituting 3.16 kΩ resistors for the 2.67 kΩ resistors in the twin-T section (R1 through R5) configures the active filter to reject 50 Hz interference.

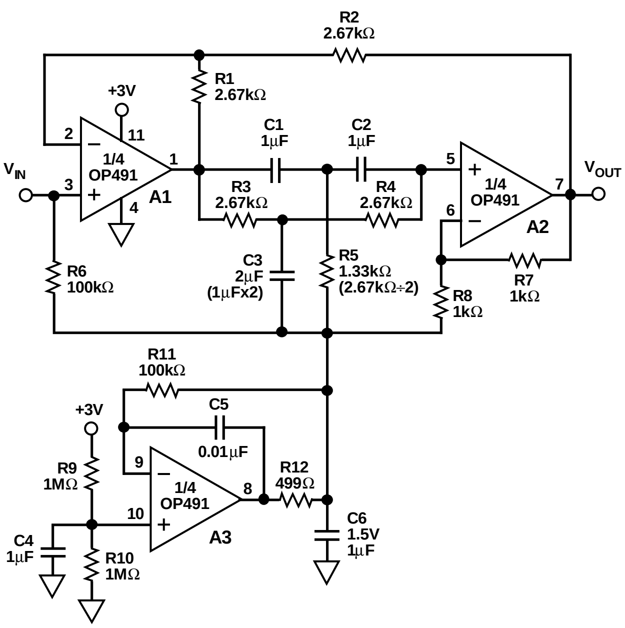


Figure 66. A +3 V Single-Supply, 50 Hz/60 Hz Active Notch Filter with False Ground

Amplifier A3 is the heart of the false-ground bias circuit. It simply buffers the voltage developed by R9 and R10 and is the reference for the active notch filter. Since the OP491 exhibits a rail-to-rail input common-mode range, R9 and R10 are chosen to split the +3 V supply symmetrically. An in-the-loop compensation scheme is used around the OP491 that allows the op amp to drive C6, a 1 µF capacitor, without oscillation. C6 maintains a low impedance ac ground over the operating frequency range of the filter.

The filter section uses a pair of OP491s in a twin-T configuration whose frequency selectivity is very sensitive to the relative matching of the capacitors and resistors in the twin-T section. Mylar is the material of choice for the capacitors, and the relative matching of the capacitors and resistors determines the filter's passband symmetry. Using 1% resistors and 5% capacitors produces satisfactory results.

Single-Supply Half-Wave and Full-Wave Rectifiers

An OP191 family configured as a voltage follower operating on a single supply can be used as a simple half-wave rectifier in low-frequency (<2 kHz) applications. A full-wave rectifier can be configured with a pair of OP291s as illustrated in Figure 67. The circuit works in the following way: When the input signal is above 0 V, the output of amplifier A1 follows the input signal. Since the noninverting input of amplifier A2 is connected to A1's output, op amp loop control forces the A2's inverting input to the same potential. The result is that both terminals of R1 are equipotential; i.e., no current flows. Since there is no current flow in R1, the same condition exists upon R2; thus, the output of the circuit tracks the input signal. When the input signal is below 0 V, the output voltage of A1 is forced to 0 V. This condition now forces A2 to operate as an inverting voltage follower because the noninverting terminal of A2 is at 0 V as well. The output voltage at $V_{OUT}A$ is then a full-wave rectified version of the input signal. If needed, a buffered, half-wave rectified version of the input signal is available at $V_{OUT}B$.

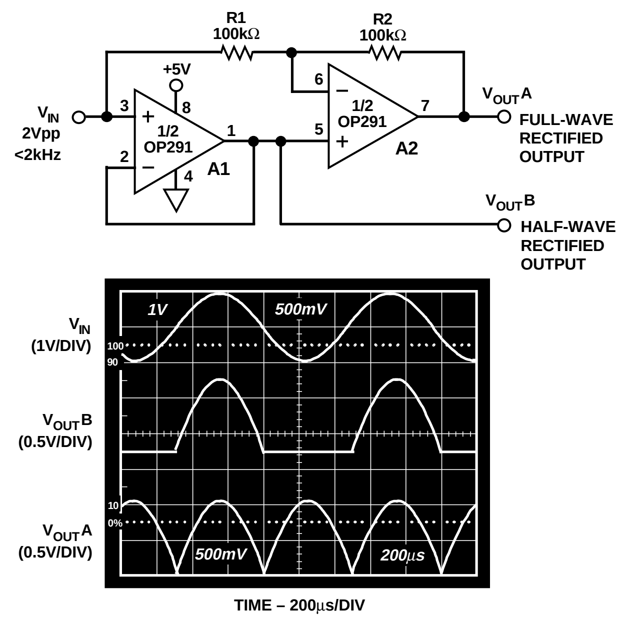


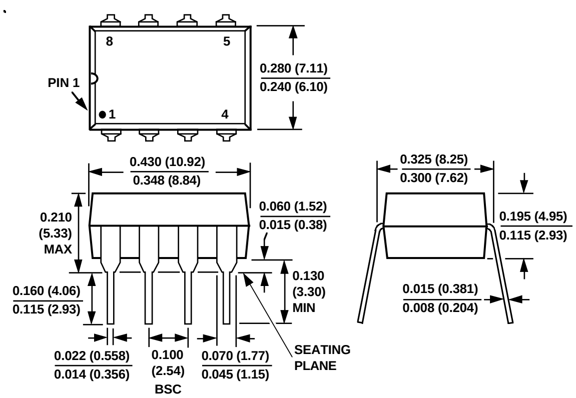
Figure 67. Single-Supply Half-Wave and Full-Wave Rectifiers Using an OP291

```
* OP491 SPICE Macro-model              Rev. A, 5/94
*                                      ARG/ADI
*
* Copyright 1994 by Analog Devices
*
* Refer to "README.DOC" file for License Statement. Use of
* this model indicates your acceptance of the terms and pro-
* visions in the License Statement.
*
* Node assignments
*                    noninverting input
*                    |   inverting input
*                    |   |    positive supply
*                    |   |    |     negative supply
*                    |   |    |     |    output
*                    |   |    |     |    |
.SUBCKT OP491        1   2    99    50   45
*
* INPUT STAGE
*
I1   99   7    8.06E-6
Q1   6    4    7    QP
Q2   5    3    7    QP
D1   3    99   DX
D2   4    99   DX
D3   3    4    DX
D4   4    3    DX
R1   3    8    5E3
R2   4    2    5E3
R3   5    50   6.4654E3
R4   6    50   6.4654E3
EOS  8    1    POLY(1)  (16,39)   –0.08E-3   1
IOS  3    4    50E-12
GB1  3    98   (21,98) 50E-9
GB2  4    98   (21,98) 50E-9
CIN  1    2    1E-12
*
* 1ST GAIN STAGE
*
EREF 98   0    (39,0)     1
G1   98   9    (6,5)      31.667E-6
R7   9    98   1E6
EC1  99   10   POLY(1)  (99,39)   –0.52   1
EC2  11   50   POLY(1)  (39,50)   –0.52   1
D5   9    10   DX
D6   11   9    DX
*
* 2ND GAIN STAGE AND DOMINANT POLE AT 1.25 Hz
*
G2   98   12   (9,39)     8E-6
R8   12   98   276.311E6
C2   12   98   16E-12
D7   12   13   DX
D8   14   12   DX
V1   99   13   0.58
V2   14   50   0.58
*
* COMMON-MODE STAGE
*
ECM  15   98   POLY(2) (1,39) (2,39) 0 0.5 0.5
R9   15   16   1E6
R10  16   98   10
*
* POLE AT 2.5 MHz
*
G3   98   18   (12,39) 1E-6
R11  18   98   1E6
C4   18   98   63.662E-15
*
* BIAS CURRENT-VS-COMMON-MODE VOLTAGE
*
EP   97   0    (99,0) 1
VB   99   17   1.3
RB   17   50   1E9
E3   19   0    (15,17) 16
D13  19   20   DX
R12  20   0    1E6
G4   98   21   (20,0) 1E-3
R13  21   98   5E3
D14  21   22   DY
E4   97   22   (POLY(1) (99,98) -0.765 1
*
* POLE AT 100 MHz
*
G6   98   40   (18,39) 1E-6
R20  40   98   1E6
C10  40   98   1.592E-15
*
* OUTPUT STAGE
*
RS1  99   39   109.375E3
RS2  39   50   109.375E3
RO1  99   45   41.667
RO2  45   50   41.667
G7   45   99   (99,40) 24E-3
G8   50   45   (40,50) 24E-3
G9   98   60   (45,40) 24E-3
D9   60   61   DX
D10  62   60   DX
V7   61   98   DC 0
V8   98   62   DC 0
FSY  99   50   POLY(2) V7 V8 0.207E-3  1  1
D11  41   45   DZ
D12  45   42   DZ
V5   40   41   0.131
V6   42   40   0.131
.MODEL DX D()
.MODEL DY D(IS=1E-9)
.MODEL DZ D(IS=1E-6)
.MODEL QP PNP(BF=66.667)
.ENDS
```

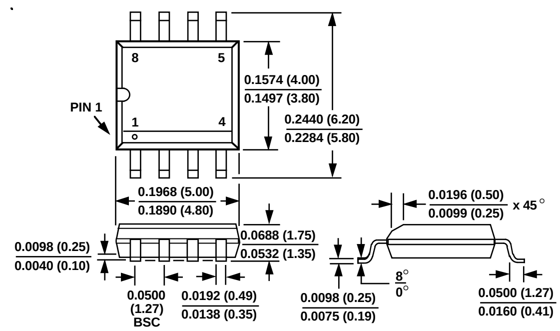
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

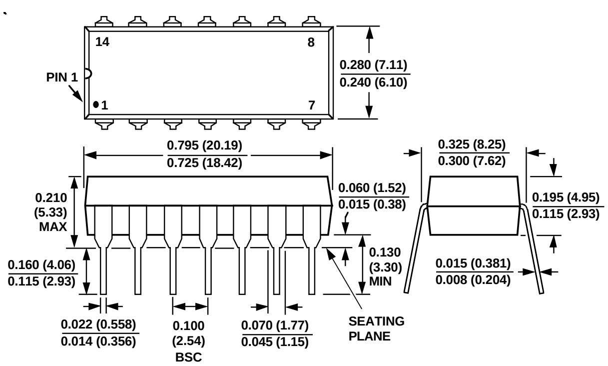
8-Lead Epoxy DIP (P Suffix)



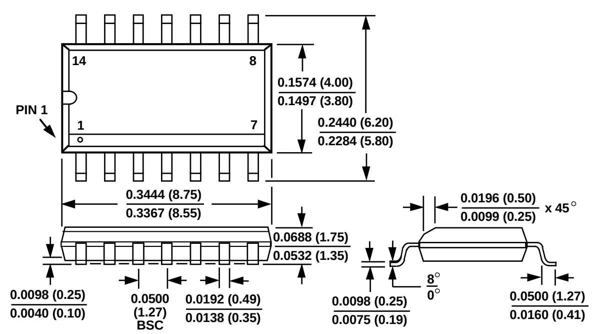
8-Lead Narrow-Body SO (S Suffix)



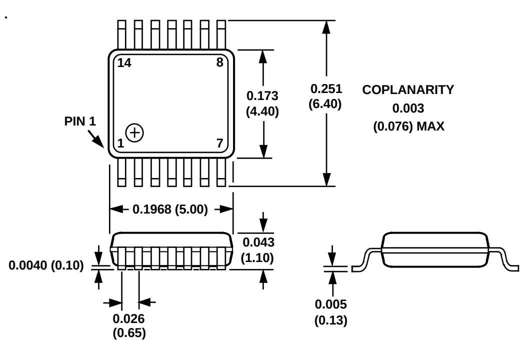
14-Lead Epoxy DIP (P Suffix)



14-Lead Narrow-Body SO (S Suffix)



14-Lead TSSOP (RU Suffix)



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