

### FEATURES

**Single-supply operation: 2.7 V to 6 V**  
**High output current:  $\pm 250$  mA**  
**Low supply current: 750  $\mu$ A/amplifier**  
**Wide bandwidth: 3 MHz**  
**Slew rate: 5 V/ $\mu$ s**  
**No phase reversal**  
**Low input currents**  
**Unity gain stable**  
**Rail-to-rail input and output**

### APPLICATIONS

**Multimedia audio**  
**LCD driver**  
**ASIC input or output amplifier**  
**Headphone driver**

### GENERAL DESCRIPTION

The AD8531, AD8532, and AD8534 are single, dual, and quad rail-to-rail input and output single-supply amplifiers featuring 250 mA output drive current. This high output current makes these amplifiers excellent for driving either resistive or capacitive loads. AC performance is very good with 3 MHz bandwidth, 5 V/ $\mu$ s slew rate, and low distortion. All are guaranteed to operate from a 3 V single supply as well as a 5 V supply.

The very low input bias currents enable the AD853x to be used for integrators, diode amplification, and other applications requiring low input bias current. Supply current is only 750  $\mu$ A per amplifier at 5 V, allowing low current applications to control high current loads.

Applications include audio amplification for computers, sound ports, sound cards, and set-top boxes. The AD853x family is very stable, and it is capable of driving heavy capacitive loads such as those found in LCDs.

The ability to swing rail-to-rail at the inputs and outputs enables designers to buffer CMOS DACs, ASICs, or other wide output swing devices in single-supply systems.

The AD8531, AD8532, and AD8534 are specified over the extended industrial ( $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ) temperature range. The AD8531 is available in 8-lead SOIC and 5-lead SC70 and SOT-23 packages. The AD8532 is available in 8-lead SOIC, MSOP, and TSSOP surface-mount packages. The AD8534 is available in narrow SOIC-14 and 14-lead TSSOP surface-mount packages.

#### Rev. E

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### PIN CONFIGURATIONS

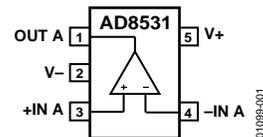


Figure 1. 5-Lead SC70 and SOT-23  
(KS and RT Suffixes)

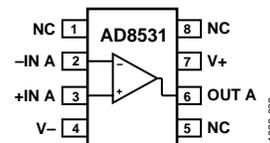


Figure 2. 8-Lead SOIC  
(R Suffix)

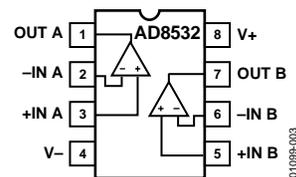


Figure 3. 8-Lead SOIC, TSSOP, and MSOP  
(R, RU, and RM Suffixes)

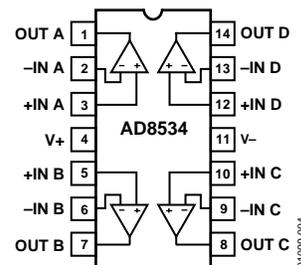


Figure 4. 14-Lead SOIC and TSSOP  
(R and RU Suffixes)

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## REVISION HISTORY

### 04/05—Rev. D to Rev. E

Updated Format.....	Universal
Changes to Pin Configurations.....	1
Changes to Table 4.....	5
Updated Outline Dimensions.....	18
Changes to Ordering Guide.....	19

### 10/02—REV. C to REV. D.

Deleted 8-Lead PDIP (N-8).....	Universal
Deleted 14-Lead PDIP (N-14).....	Universal
Edits to Figure 34.....	9
Updated OUTLINE DIMENSIONS.....	15

### 8/96—Revision 0: Initial Version

# SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS

@  $V_S = 3.0\text{ V}$ ,  $V_{CM} = 1.5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	$V_{OS}$	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$			25 30	mV mV
Input Bias Current	$I_B$	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		5	50	pA
Input Offset Current	$I_{OS}$	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		1	25 30	pA pA
Input Voltage Range			0		3	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to }3\text{ V}$	38	45		dB
Large Signal Voltage Gain	$A_{VO}$	$R_L = 2\text{ k}\Omega$ , $V_O = 0.5\text{ V to }2.5\text{ V}$		25		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			20		$\mu\text{V}/^\circ\text{C}$
Bias Current Drift	$\Delta I_B/\Delta T$			50		fA/ $^\circ\text{C}$
Offset Current Drift	$\Delta I_{OS}/\Delta T$			20		fA/ $^\circ\text{C}$
OUTPUT CHARACTERISTICS						
Output Voltage High	$V_{OH}$	$I_L = 10\text{ mA}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	2.85 2.8	2.92		V V
Output Voltage Low	$V_{OL}$	$I_L = 10\text{ mA}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		60	100 125	mV mV
Output Current	$I_{OUT}$			$\pm 250$		mA
Closed-Loop Output Impedance	$Z_{OUT}$	$f = 1\text{ MHz}$ , $A_V = 1$		60		$\Omega$
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = 3\text{ V to }6\text{ V}$	45	55		dB
Supply Current/Amplifier	$I_{SY}$	$V_O = 0\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		0.70	1 1.25	mA mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$		3.5		V/ $\mu\text{s}$
Settling Time	$t_S$	To 0.01%		1.6		$\mu\text{s}$
Gain Bandwidth Product	GBP			2.2		MHz
Phase Margin	$\phi_O$			70		Degrees
Channel Separation	CS	$f = 1\text{ kHz}$ , $R_L = 2\text{ k}\Omega$		65		dB
NOISE PERFORMANCE						
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$ $f = 10\text{ kHz}$		45 30		nV/ $\sqrt{\text{Hz}}$ nV/ $\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 1\text{ kHz}$		0.05		pA/ $\sqrt{\text{Hz}}$

# AD8531/AD8532/AD8534

## ELECTRICAL CHARACTERISTICS

@  $V_S = 5.0\text{ V}$ ,  $V_{CM} = 2.5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$			25	mV
Input Bias Current	$I_B$	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		5	50	pA
Input Offset Current	$I_{OS}$	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		1	25	pA
Input Voltage Range		$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$			30	pA
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to } 5\text{ V}$	0		5	V
Large Signal Voltage Gain	$A_{VO}$	$R_L = 2\text{ k}\Omega$ , $V_O = 0.5\text{ V to } 4.5\text{ V}$	38	47		dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		20		$\mu\text{V}/^\circ\text{C}$
Bias Current Drift	$\Delta I_B/\Delta T$			50		$\text{fA}/^\circ\text{C}$
Offset Current Drift	$\Delta I_{OS}/\Delta T$			20		$\text{fA}/^\circ\text{C}$
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$I_L = 10\text{ mA}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	4.9 4.85	4.94		V V
Output Voltage Low	$V_{OL}$	$I_L = 10\text{ mA}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		50	100	mV mV
Output Current	$I_{OUT}$			$\pm 250$		mA
Closed-Loop Output Impedance	$Z_{OUT}$	$f = 1\text{ MHz}$ , $A_V = 1$		40		$\Omega$
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_S = 3\text{ V to } 6\text{ V}$	45	55		dB
Supply Current/Amplifier	$I_{SY}$	$V_O = 0\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		0.75	1.25	mA mA
					1.75	
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$		5		$\text{V}/\mu\text{s}$
Full-Power Bandwidth	$BW_p$	1% distortion		350		kHz
Settling Time	$t_s$	To 0.01%		1.4		$\mu\text{s}$
Gain Bandwidth Product	GBP			3		MHz
Phase Margin	$\phi_o$			70		Degrees
Channel Separation	CS	$f = 1\text{ kHz}$ , $R_L = 2\text{ k}\Omega$		65		dB
<b>NOISE PERFORMANCE</b>						
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$ $f = 10\text{ kHz}$		45 30		$\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 1\text{ kHz}$		0.05		$\text{pA}/\sqrt{\text{Hz}}$

## ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage ( $V_S$ )	7 V
Input Voltage	GND to $V_S$
Differential Input Voltage <sup>1</sup>	$\pm 6$ V
Storage Temperature Range	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Operating Temperature Range	$-40^\circ\text{C}$ to $+85^\circ\text{C}$
Junction Temperature Range	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Lead Temperature Range (Soldering, 60 sec)	$300^\circ\text{C}$

<sup>1</sup> For supplies less than +6 V, the differential input voltage is equal to  $\pm V_S$ .

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



Table 4. Package Information

Package Type	$\theta_{JA}$ <sup>1</sup>	$\theta_{JC}$	Unit
5-Lead SC70 (KS)	376	126	$^\circ\text{C}/\text{W}$
5-Lead SOT-23 (RT)	230	146	$^\circ\text{C}/\text{W}$
8-Lead SOIC (R)	158	43	$^\circ\text{C}/\text{W}$
8-Lead MSOP (RM)	210	45	$^\circ\text{C}/\text{W}$
8-Lead TSSOP (RU)	240	43	$^\circ\text{C}/\text{W}$
14-Lead SOIC (R)	120	36	$^\circ\text{C}/\text{W}$
14-Lead TSSOP (RU)	240	43	$^\circ\text{C}/\text{W}$

<sup>1</sup>  $\theta_{JA}$  is specified for the worst-case conditions; that is,  $\theta_{JA}$  is specified for device soldered onto a circuit board for surface-mount packages.

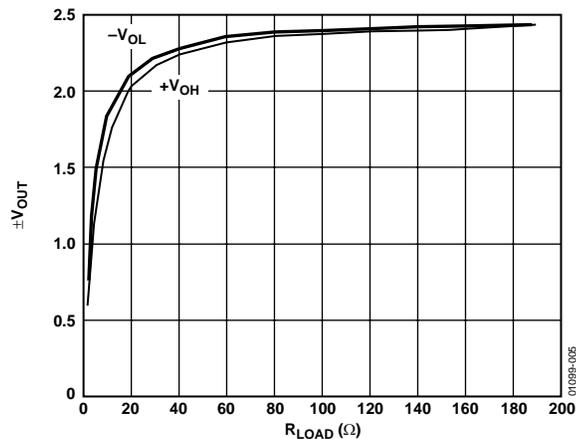


Figure 5. Output Voltage vs. Load.  $V_S = \pm 2.5$  V,  $R_i$  Is Connected to GND (0 V)

TYPICAL PERFORMANCE CHARACTERISTICS

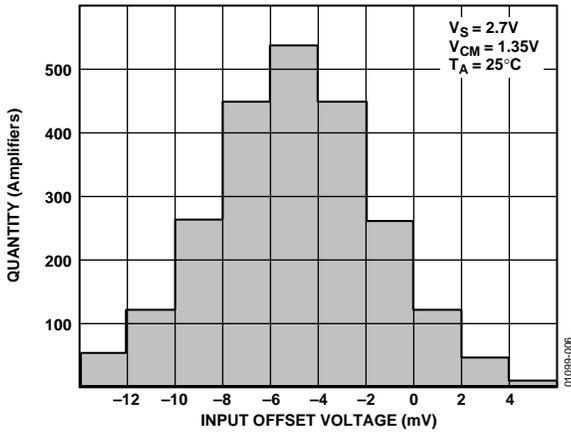


Figure 6. Input Offset Voltage Distribution

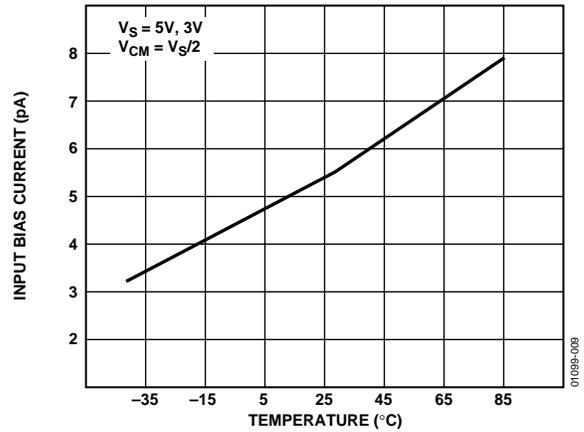


Figure 9. Input Bias Current vs. Temperature

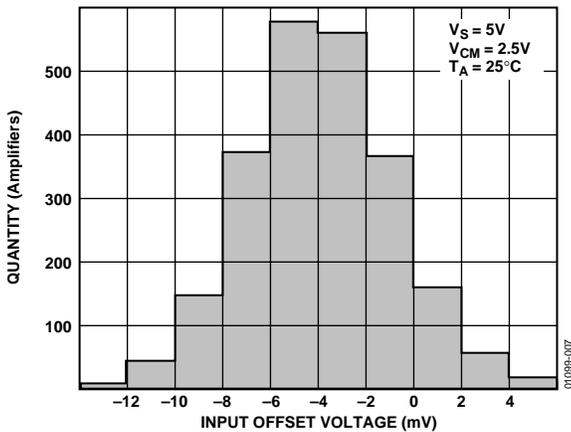


Figure 7. Input Offset Voltage Distribution

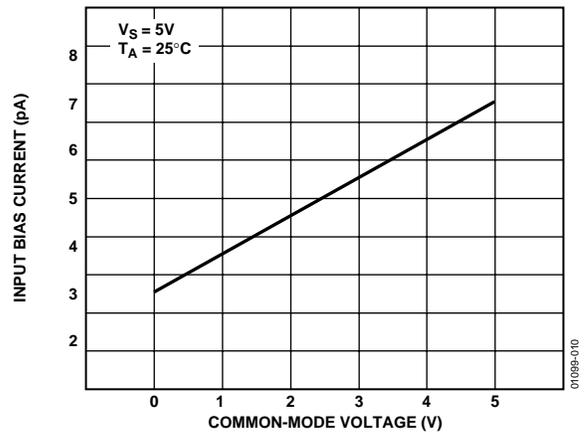


Figure 10. Input Bias Current vs. Common-Mode Voltage

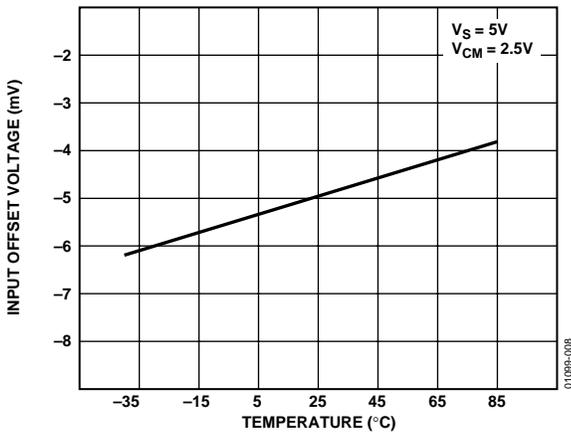


Figure 8. Input Offset Voltage vs. Temperature

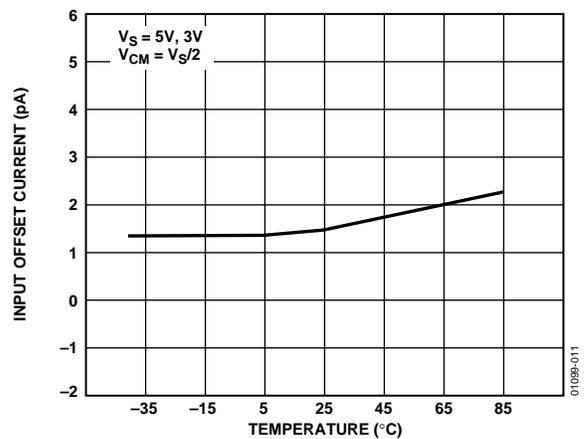


Figure 11. Input Offset Current vs. Temperature

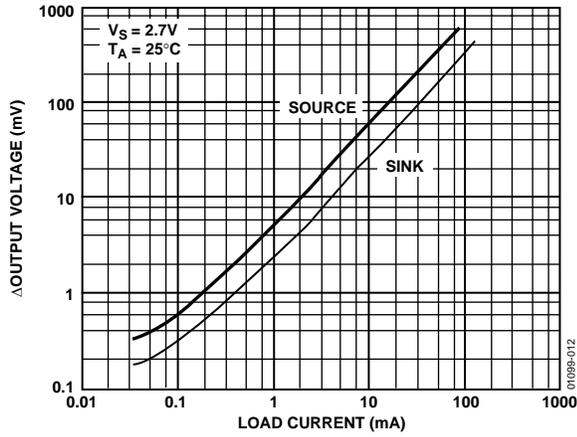


Figure 12. Output Voltage to Supply Rail vs. Load Current

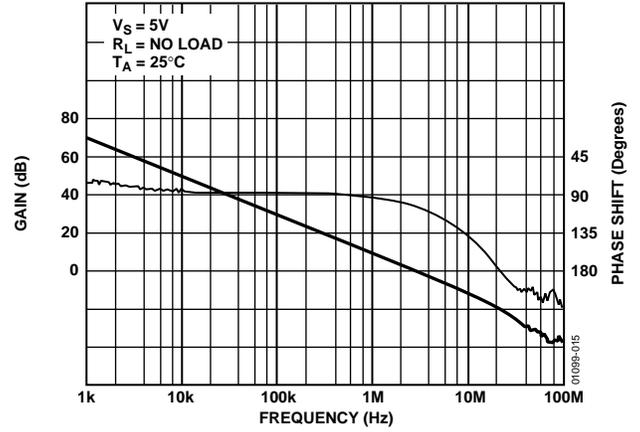


Figure 15. Open-Loop Gain and Phase vs. Frequency

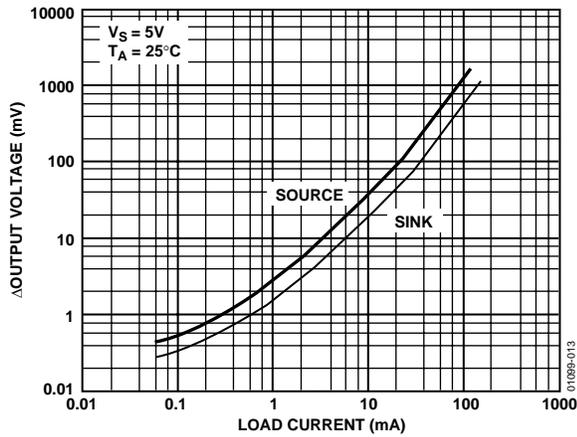


Figure 13. Output Voltage to Supply Rail vs. Load Current

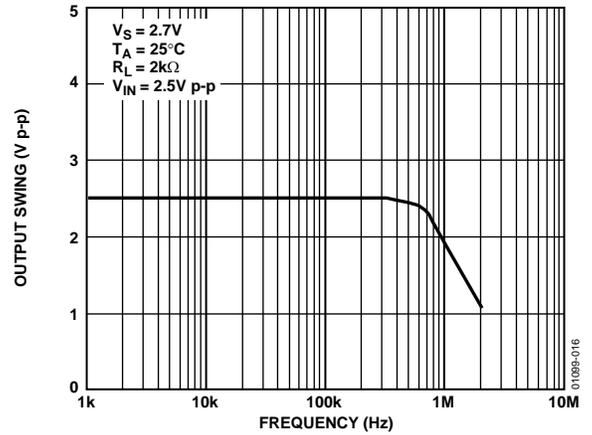


Figure 16. Closed-Loop Output Voltage Swing vs. Frequency

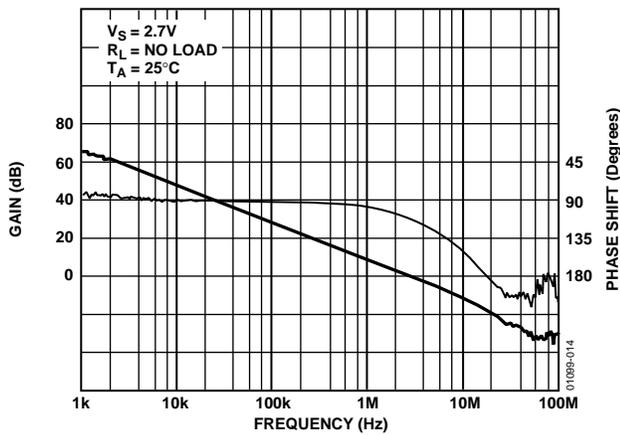


Figure 14. Open-Loop Gain and Phase vs. Frequency

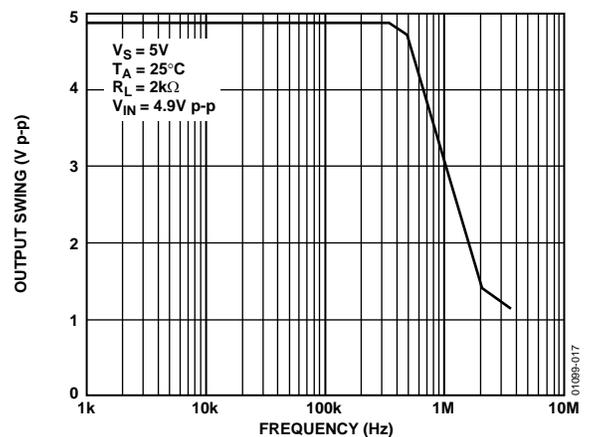


Figure 17. Closed-Loop Output Voltage Swing vs. Frequency

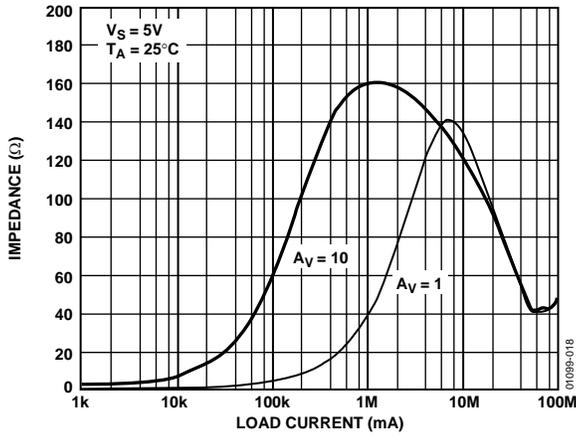


Figure 18. Closed-Loop Output Impedance vs. Frequency

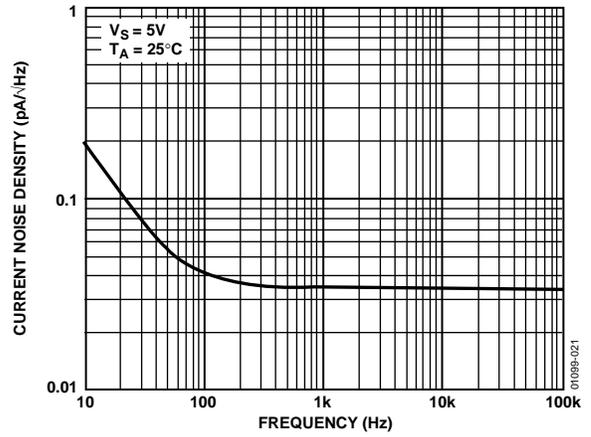


Figure 21. Current Noise Density vs. Frequency

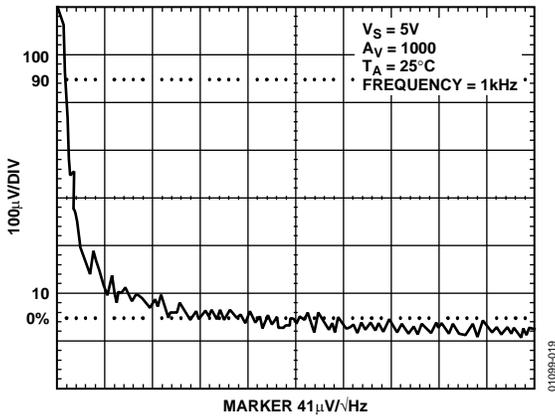


Figure 19. Voltage Noise Density vs. Frequency

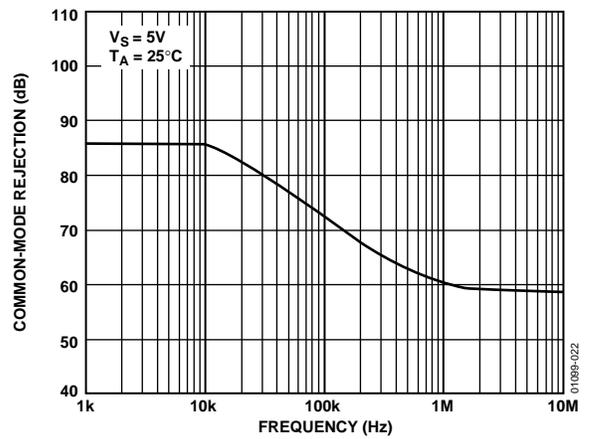


Figure 22. Common-Mode Rejection vs. Frequency

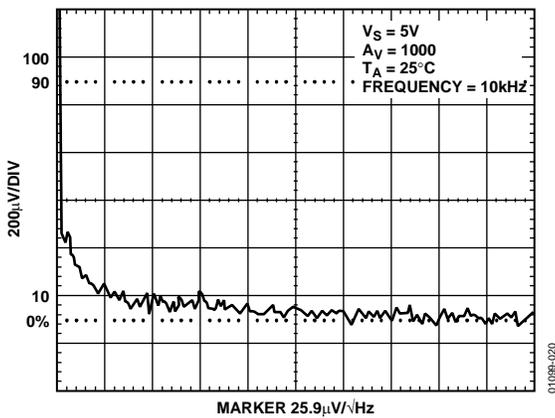


Figure 20. Voltage Noise Density vs. Frequency

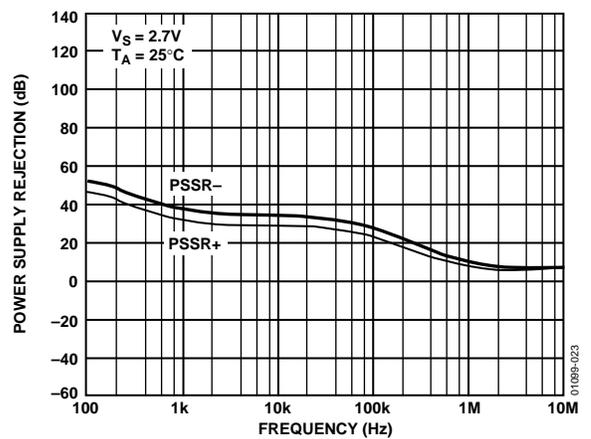


Figure 23. Power Supply Rejection vs. Frequency

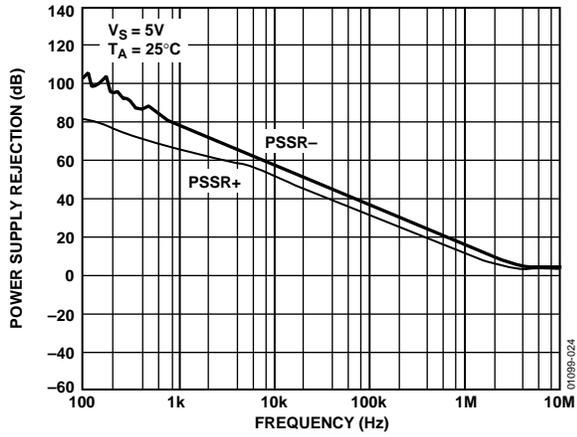


Figure 24. Power Supply Rejection vs. Frequency

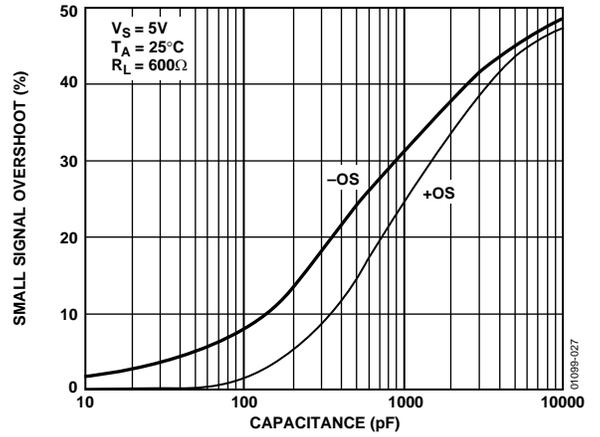


Figure 27. Small Signal Overshoot vs. Load Capacitance

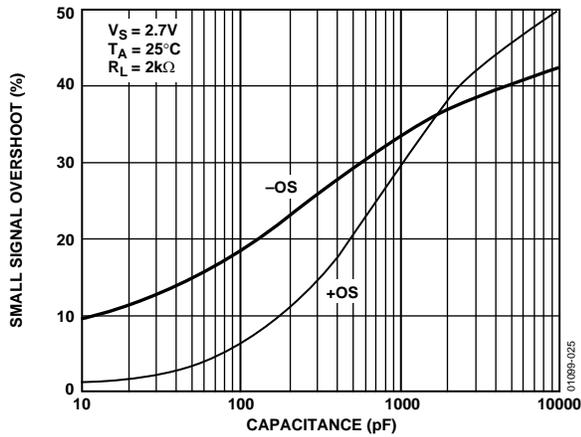


Figure 25. Small Signal Overshoot vs. Load Capacitance

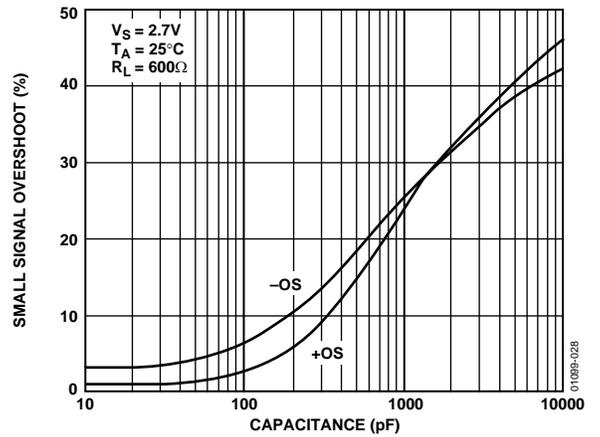


Figure 28. Small Signal Overshoot vs. Load Capacitance

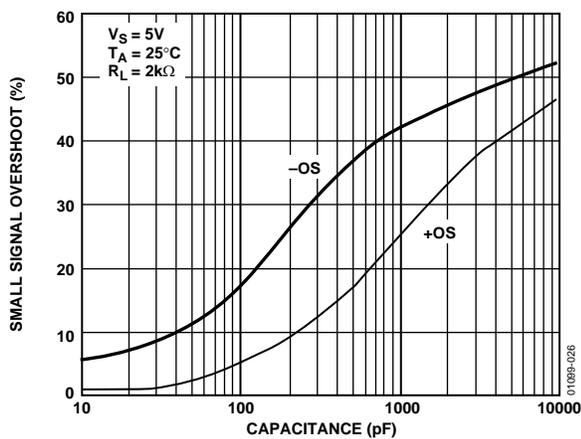


Figure 26. Small Signal Overshoot vs. Load Capacitance

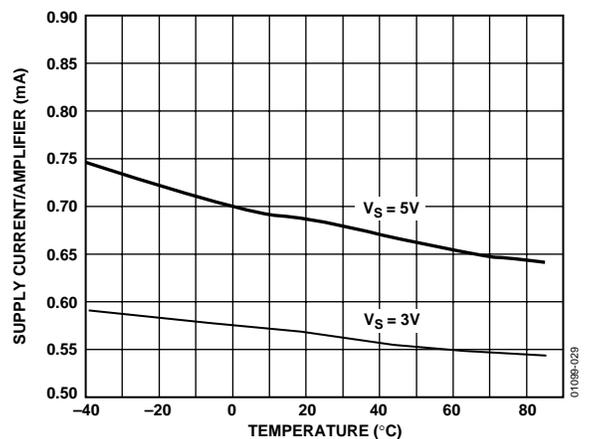


Figure 29. Supply Current per Amplifier vs. Temperature

# AD8531/AD8532/AD8534

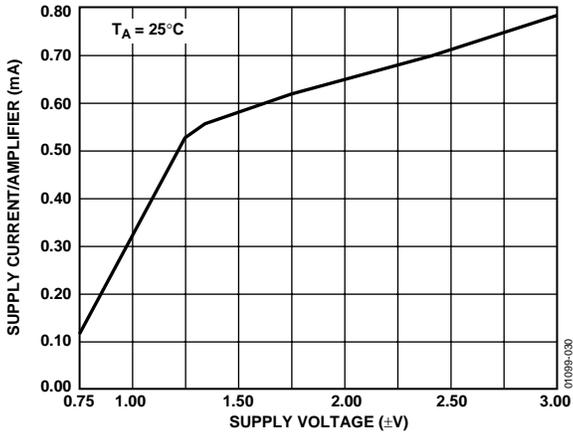


Figure 30. Supply Current per Amplifier vs. Supply Voltage

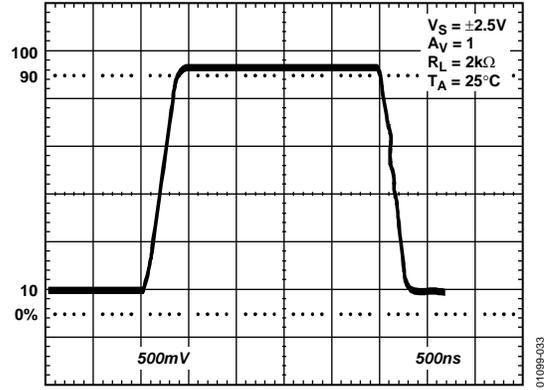


Figure 33. Large Signal Transient Response

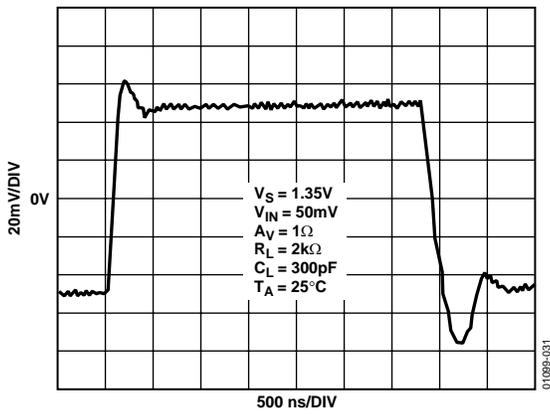


Figure 31. Small Signal Transient Response

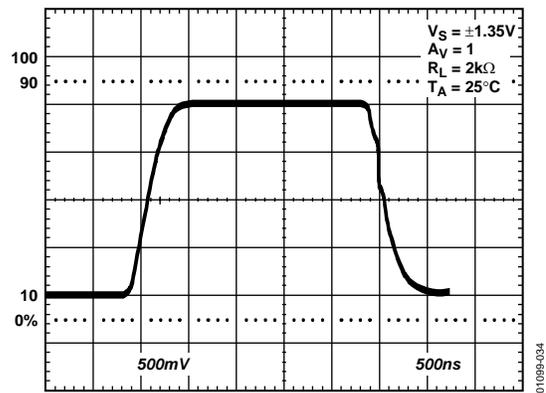


Figure 34. Large Signal Transient Response

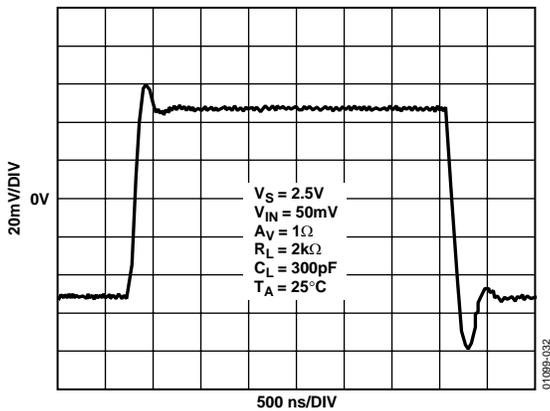


Figure 32. Small Signal Transient Response

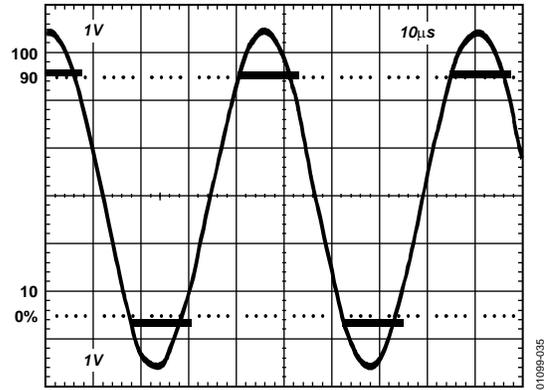


Figure 35. No Phase Reversal

## THEORY OF OPERATION

The AD8531/AD8532/AD8534 are all CMOS, high output current drive, rail-to-rail input/output operational amplifiers. Their high output current drive and stability with heavy capacitive loads make the AD8531/AD8532/AD8534 excellent choices as drive amplifiers for LCD panels.

Figure 36 illustrates a simplified equivalent circuit for the AD8531/AD8532/AD8534. Like many rail-to-rail input amplifier configurations, it comprises two differential pairs, one N-channel (M1 to M2) and one P-channel (M3 to M4). These differential pairs are biased by  $50\ \mu\text{A}$  current sources, each with a compliance limit of approximately  $0.5\ \text{V}$  from either supply voltage rail. The differential input voltage is then converted into a pair of differential output currents. These differential output currents are then combined in a compound folded-cascade second gain stage (M5 to M9). The outputs of the second gain stage at M8 and M9 provide the gate voltage drive to the rail-to-rail output stage. Additional signal current recombination for the output stage is achieved through the use of Transistor M11 to Transistor M14.

To achieve rail-to-rail output swings, the AD8531/AD8532/AD8534 design employs a complementary, common source output stage (M15–M16). However, the output voltage swing is directly dependent on the load current, as the difference between the output voltage and the supply is determined by the AD8531/AD8532/AD8534's output transistors on channel resistance (see Figure 12 and Figure 13). The output stage also exhibits voltage gain by virtue of the use of common source amplifiers; as a result, the voltage gain of the output stage (thus, the open-loop gain of the device) exhibits a strong dependence to the total load resistance at the output of the AD8531/AD8532/AD8534.

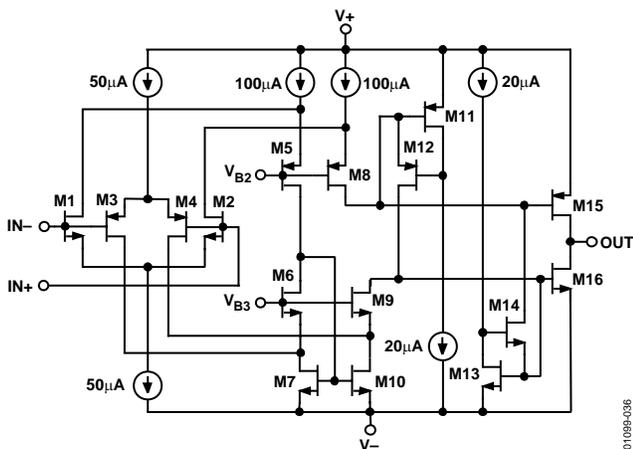


Figure 36. AD8531/AD8532/AD8534 Simplified Equivalent Circuit

## SHORT-CIRCUIT PROTECTION

As a result of the design of the output stage for maximum load current capability, the AD8531/AD8532/AD8534 do not have any internal short-circuit protection circuitry. Direct connection of the output of the AD8531/AD8532/AD8534 to the positive supply in single-supply applications destroys the device. In those applications where some protection is needed, but not at the expense of reduced output voltage headroom, a low value resistor in series with the output, as shown in Figure 37, can be used. The resistor, connected within the feedback loop of the amplifier, has very little effect on the performance of the amplifier other than limiting the maximum available output voltage swing. For single  $5\ \text{V}$  supply applications, resistors less than  $20\ \Omega$  are not recommended.

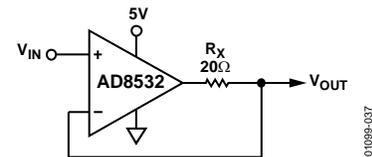


Figure 37. Output Short-Circuit Protection

## POWER DISSIPATION

Although the AD8531/AD8532/AD8534 are capable of providing load currents to  $250\ \text{mA}$ , the usable output load current drive capability is limited to the maximum power dissipation allowed by the device package used. In any application, the absolute maximum junction temperature for the AD8531/AD8532/AD8534 is  $150^\circ\text{C}$ . The maximum junction temperature should never be exceeded because the device could suffer premature failure. Accurately measuring power dissipation of an integrated circuit is not always a straightforward exercise, so Figure 38 has been provided as a design aid for either setting a safe output current drive level or selecting a heat sink for the package options available on the AD8531/AD8532/AD8534.

# AD8531/AD8532/AD8534

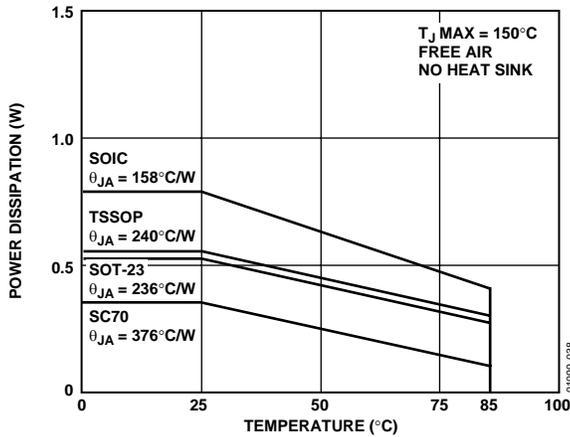


Figure 38. Maximum Power Dissipation vs. Ambient Temperature

These thermal resistance curves were determined using the AD8531/AD8532/AD8534 thermal resistance data for each package and a maximum junction temperature of 150°C. The following formula can be used to calculate the internal junction temperature of the AD8531/AD8532/AD8534 for any application:

$$T_j = P_{DISS} \times \theta_{JA} + T_A$$

where:

$T_j$  is the junction temperature.

$P_{DISS}$  is the power dissipation.

$\theta_{JA}$  is the package thermal resistance, junction-to-case.

$T_A$  is the ambient temperature of the circuit.

To calculate the power dissipated by the AD8531/AD8532/AD8534, the following equation can be used:

$$P_{DISS} = I_{LOAD} \times (V_S - V_{OUT})$$

where:

$I_{LOAD}$  is the output load current.

$V_S$  is the supply voltage.

$V_{OUT}$  is the output voltage.

The quantity within the parentheses is the maximum voltage developed across either output transistor. As an additional design aid in calculating available load current from the AD8531/AD8532/AD8534, Figure 5 illustrates the output voltage of the AD8531/AD8532/AD8534 as a function of load resistance.

## POWER CALCULATIONS FOR VARYING OR UNKNOWN LOADS

Often, calculating power dissipated by an integrated circuit to determine if the device is being operated in a safe range is not as simple as it might seem. In many cases power cannot be directly measured. This may be the result of irregular output waveforms or varying loads; indirect methods of measuring power are required.

There are two methods to calculate power dissipated by an integrated circuit. The first can be done by measuring the package temperature and the board temperature. The other is to directly measure the circuit's supply current.

## CALCULATING POWER BY MEASURING AMBIENT AND CASE TEMPERATURE

Given the two equations for calculating junction temperature

$$T_j = T_A + P\theta_{JA}$$

where:

$T_j$  is the junction temperature.

$T_A$  is the ambient temperature.

$\theta_{JA}$  is the junction to ambient thermal resistance.

$$T_j = T_C + P\theta_{JC}$$

where:

$T_C$  is the case temperature.

$\theta_{JA}$  and  $\theta_{JC}$  are given in the data sheet.

The two equations can be solved for  $P$  (power):

$$T_A + P\theta_{JA} = T_C + P\theta_{JC}$$

$$P = (T_A - T_C) / (\theta_{JC} - \theta_{JA})$$

Once power has been determined, it is necessary to go back and calculate the junction temperature to assure that it has not been exceeded.

The temperature measurements should be directly on the package and on a spot on the board that is near the package but definitely not touching it. Measuring the package could be difficult. A very small bimetallic junction glued to the package could be used, or measurement could be done using an infrared sensing device if the spot size is small enough.

## CALCULATING POWER BY MEASURING SUPPLY CURRENT

Power can be calculated directly, knowing the supply voltage and current. However, supply current may have a dc component with a pulse into a capacitive load. This could make rms current very difficult to calculate. It can be overcome by lifting the supply pin and inserting an rms current meter into the circuit. For this to work, be sure all of the current is being delivered by the supply pin being measured. This is usually a good method in a single supply system; however, if the system uses dual supplies, both supplies may need to be monitored.

## INPUT OVERVOLTAGE PROTECTION

As with any semiconductor device, whenever the condition exists for the input to exceed either supply voltage, the device's input overvoltage characteristic must be considered. When an overvoltage occurs, the amplifier could be damaged, depending on the magnitude of the applied voltage and the magnitude of the fault current. Although not shown here, when the input voltage exceeds either supply by more than 0.6 V, pn junctions internal to the AD8531/AD8532/AD8534 energize, allowing current to flow from the input to the supplies. As illustrated in the simplified equivalent input circuit (Figure 36), the AD8531/AD8532/AD8534 do not have any internal current limiting resistors, so fault currents can quickly rise to damaging levels.

This input current is not inherently damaging to the device, as long as it is limited to 5 mA or less. For the AD8531/AD8532/AD8534, once the input voltage exceeds the supply by more than 0.6 V, the input current quickly exceeds 5 mA. If this condition continues to exist, an external series resistor should be added. The size of the resistor is calculated by dividing the maximum overvoltage by 5 mA. For example, if the input voltage could reach 10 V, the external resistor should be  $(10 \text{ V}/5 \text{ mA}) = 2 \text{ k}\Omega$ . This resistance should be placed in series with either or both inputs if they are exposed to an overvoltage condition. For more information on general overvoltage characteristics of amplifiers, refer to the 1993 Seminar Applications Guide, available from the Analog Devices Literature Center.

## OUTPUT PHASE REVERSAL

Some operational amplifiers designed for single-supply operation exhibit an output voltage phase reversal when their inputs are driven beyond their useful common-mode range. The AD8531/AD8532/AD8534 are free from reasonable input voltage range restrictions, provided that input voltages no greater than the supply voltage rails are applied. Although the device's output does not change phase, large currents can flow

through internal junctions to the supply rails, as was pointed out in the previous section. Without limit, these fault currents can easily destroy the amplifier. The technique recommended in the input overvoltage protection section should therefore be applied in those applications where the possibility of input voltages exceeding the supply voltages exists.

## CAPACITIVE LOAD DRIVE

The AD8531/AD8532/AD8534 exhibit excellent capacitive load driving capabilities. They can drive up to 10 nF directly, as shown in Figure 25 through Figure 28. However, even though the device is stable, a capacitive load does not come without a penalty in bandwidth. As shown in Figure 39, the bandwidth is reduced to under 1 MHz for loads greater than 10 nF. A "snubber" network on the output won't increase the bandwidth, but it does significantly reduce the amount of overshoot for a given capacitive load. A snubber consists of a series R-C network ( $R_S$ ,  $C_S$ ), as shown in Figure 40, connected from the output of the device to ground. This network operates in parallel with the load capacitor,  $C_L$ , to provide phase lag compensation. The actual value of the resistor and capacitor is best determined empirically.

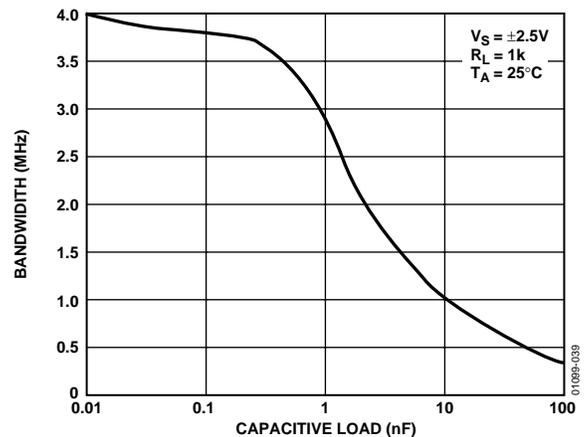


Figure 39. Unity-Gain Bandwidth vs. Capacitive Load

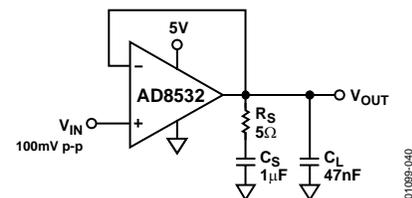


Figure 40. Snubber Network Compensates for Capacitive Loads

# AD8531/AD8532/AD8534

The first step is to determine the value of the resistor,  $R_s$ . A good starting value is  $100\ \Omega$ . This value is reduced until the small signal transient response is optimized. Next,  $C_s$  is determined;  $10\ \mu\text{F}$  is a good starting point. This value is reduced to the smallest value for acceptable performance (typically,  $1\ \mu\text{F}$ ). For the case of a  $47\ \text{nF}$  load capacitor on the AD8531/AD8532/AD8534, the optimal snubber network is a  $5\ \Omega$  in series with  $1\ \mu\text{F}$ . The benefit is immediately apparent, as seen in the scope photo in Figure 41. The top trace was taken with a  $47\ \text{nF}$  load, and the bottom trace was taken with the  $5\ \Omega$  in series with  $1\ \mu\text{F}$  snubber network in place. The amount of overshoot and ringing is dramatically reduced. Table 5 illustrates a few sample snubber networks for large load capacitors.

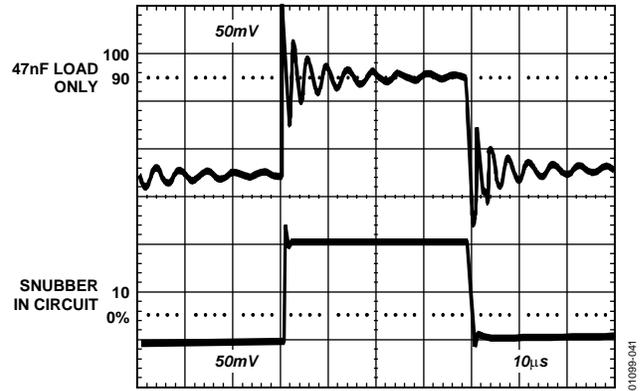


Figure 41. Overshoot and Ringing Are Reduced by Adding a Snubber Network In Parallel with the  $47\ \text{nF}$  Load

Table 5. Snubber Networks for Large Capacitive Loads

Load Capacitance ( $C_L$ )	Snubber Network ( $R_s$ , $C_s$ )
0.47 nF	$300\ \Omega$ , $0.1\ \mu\text{F}$
4.7 nF	$30\ \Omega$ , $1\ \mu\text{F}$
47 nF	$5\ \Omega$ , $1\ \mu\text{F}$



# AD8531/AD8532/AD8534

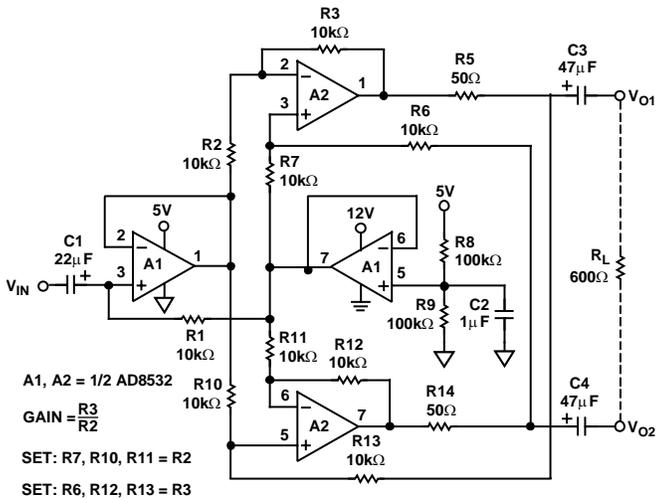


Figure 43. A Single-Supply, Balanced Line Driver for Multimedia and Automotive Applications

## SINGLE-SUPPLY HEADPHONE AMPLIFIER

Because of its speed and large output drive, the AD8531/AD8532/AD8534 make an excellent headphone driver, as illustrated in Figure 44. Its low supply operation and rail-to-rail inputs and outputs give a maximum signal swing on a single 5 V supply. To ensure maximum signal swing available to drive the headphone, the amplifier inputs are biased to  $V+/2$ , which in this case is 2.5 V. The 100 k $\Omega$  resistor to the positive supply is equally split into two 50 k $\Omega$  resistors, with their common point bypassed by 10  $\mu$ F to prevent power supply noise from contaminating the audio signal.

The audio signal is then ac-coupled to each input through a 10  $\mu$ F capacitor. A large value is needed to ensure that the 20 Hz audio information is not blocked. If the input already has the proper dc bias, the ac coupling and biasing resistors are not required. A 270  $\mu$ F capacitor is used at the output to couple the amplifier to the headphone. This value is much larger than that used for the input because of the low impedance of the headphones, which can range from 32  $\Omega$  to 600  $\Omega$ . An additional 16  $\Omega$  resistor is used in series with the output capacitor to protect the output stage of the op amp by limiting capacitor discharge current. When driving a 48  $\Omega$  load, the circuit exhibits less than 0.3% THD+N at output drive levels of 4 V p-p.

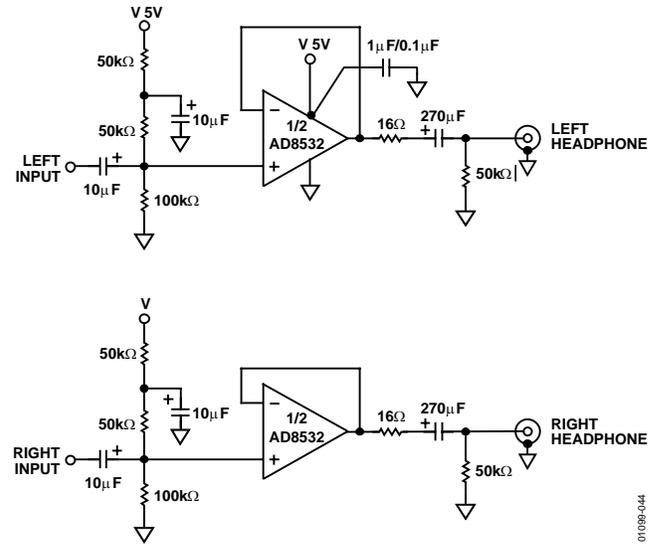


Figure 44. A Single-Supply, Stereo Headphone Driver

## SINGLE-SUPPLY, TWO-WAY LOUDSPEAKER CROSSOVER NETWORK

Active filters are useful in loudspeaker crossover networks for reasons of small size, relative freedom from parasitic effects, the ease of controlling low/high channel drive, and the controlled driver damping provided by a dedicated amplifier. Both Sallen-Key (SK) and multiple-feedback (MFB) filter architectures are useful in implementing active crossover networks. The circuit shown in Figure 45 is a single-supply, two-way active crossover that combines the advantages of both filter topologies. This active crossover exhibits less than 0.4% THD+N at output levels of 1.4 V rms using general purpose unity-gain HP/LP stages.

In this two-way example, the LO signal is a dc-500 Hz LP woofer output, and the HI signal is the HP (>500 Hz) tweeter output. U1B forms an LP section at 500 Hz, while U1A provides an HP section, covering frequencies  $\geq 500$  Hz.

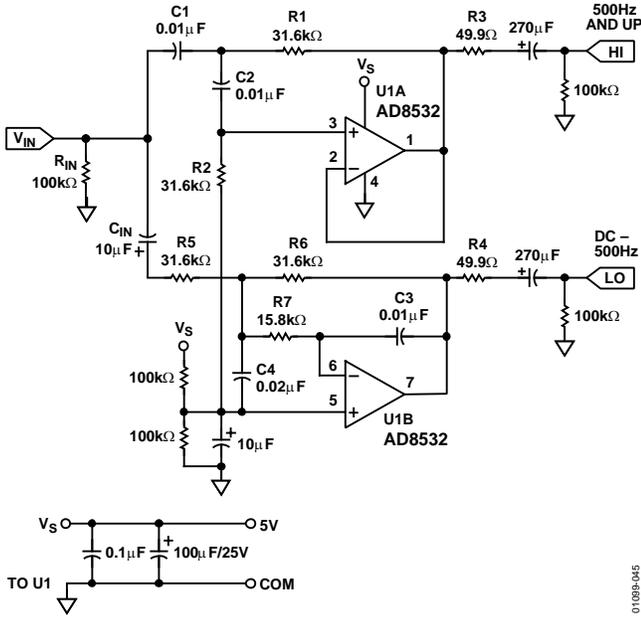


Figure 45. A Single-Supply, Two-Way Active Crossover

The crossover example frequency of 500 Hz can be shifted lower or higher by frequency scaling of either resistors or capacitors. In configuring the circuit for other frequencies, complementary LP/HP action must be maintained between sections, and component values within the sections must be in the same ratio. Table 6 provides a design aid to adaptation, with suggested standard component values for other frequencies.

For additional information on the active filters and active crossover networks, please consult the data sheet for the OP279, a dual rail-to-rail high output current operational amplifier.

Table 6. RC Component Selection for Various Crossover Frequencies<sup>1</sup>

Crossover Frequency (Hz)	R1/C1 (U1A) <sup>2</sup> R5/C3 (U1B) <sup>3</sup>
100	160 kΩ/0.01 µF
200	80.6 kΩ/0.01 µF
319	49.9 kΩ/0.01 µF
500	31.6 kΩ/0.01 µF
1 k	16 kΩ/0.01 µF
2 k	8.06 kΩ/0.01 µF
5 k	3.16 kΩ/0.01 µF
10 k	1.6 kΩ/0.01 µF

<sup>1</sup> Applicable for filter a = 2.

<sup>2</sup> For Sallen-Key stage U1A: R1 = R2, and C1 = C2, and so on.

<sup>3</sup> For multiple feedback stage U1B: R6 = R5, R7 = R5/2, and C4 = 2C3.

### DIRECT ACCESS ARRANGEMENT FOR TELEPHONE LINE INTERFACE

Figure 46 illustrates a 5 V only transmit/receive telephone line interface for 600 Ω transmission systems. It allows full duplex transmission of signals on a transformer coupled 600 Ω line in a differential manner. Amplifier A1 provides gain that can be adjusted to meet the modem output drive requirements. Both A1 and A2 are configured to apply the largest possible signal on a single supply to the transformer. Because of the high output current drive and low dropout voltage of the AD8531/AD8532/AD8534, the largest signal available on a single 5 V supply is approximately 4.5 V p-p into a 600 Ω transmission system. Amplifier A3 is configured as a difference amplifier for two reasons: (1) It prevents the transmit signal from interfering with the receive signal, and (2) it extracts the receive signal from the transmission line for amplification by A4. A4's gain can be adjusted in the same manner as that of A1 to meet the modem's input signal requirements. Standard resistor values permit the use of SIP (single in-line package) format resistor arrays.

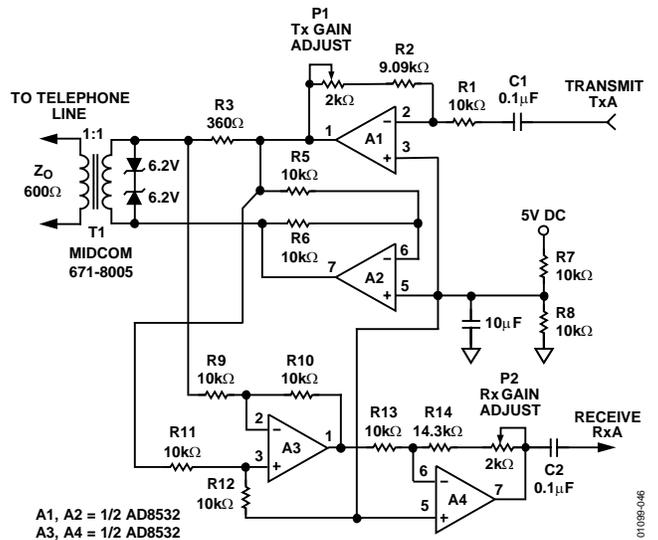


Figure 46. A Single-Supply Direct Access Arrangement for Modems

OUTLINE DIMENSIONS

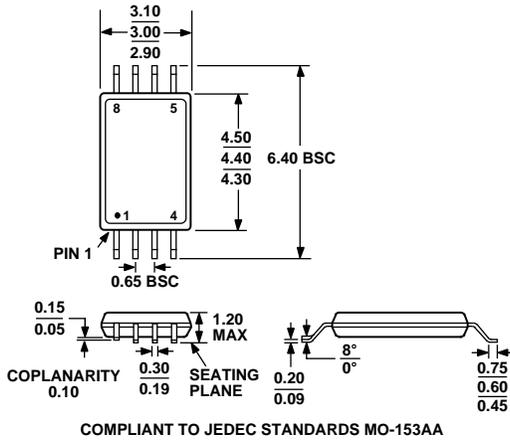


Figure 47. 8-Lead Thin Shrink Small Outline Package [TSSOP] (RU-8)  
Dimensions shown in millimeters

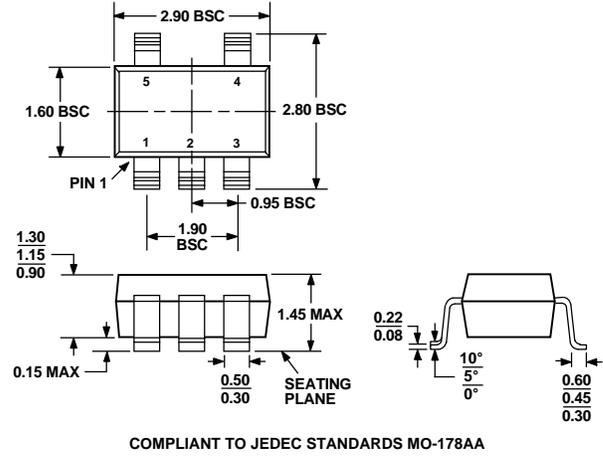


Figure 50. 5-Lead Small Outline Transistor Package [SOT-23] (RT-5)  
Dimensions shown in millimeters

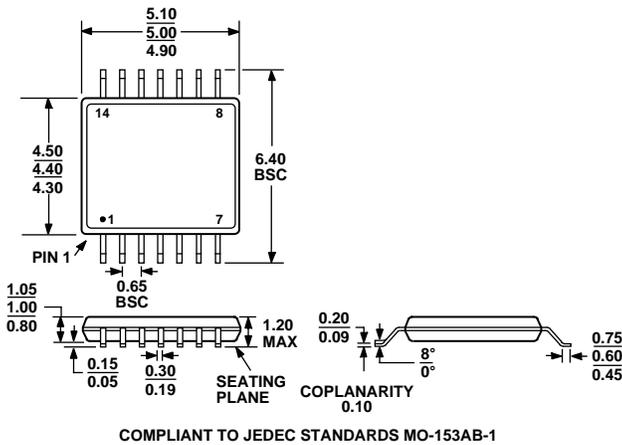


Figure 48. 14-Lead Thin Shrink Small Outline Package [TSSOP] (RU-14)  
Dimensions shown in millimeters

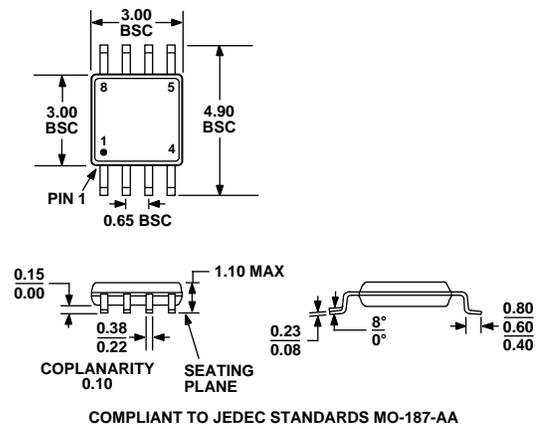


Figure 51. 8-Lead Mini Small Outline Package [MSOP] (RM-8)  
Dimensions shown in millimeters

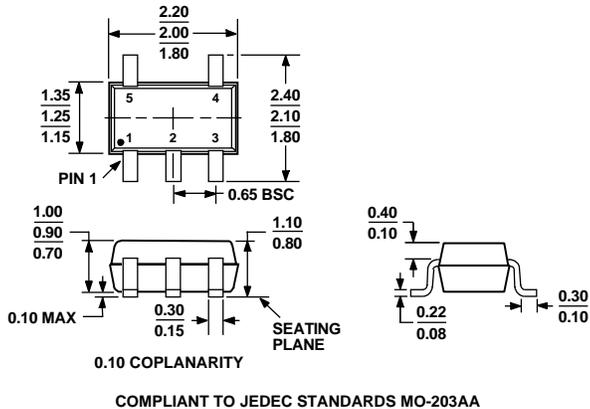


Figure 49. 5-Lead Thin Shrink Small Outline Transistor Package [KS-5]  
Dimensions shown in millimeters

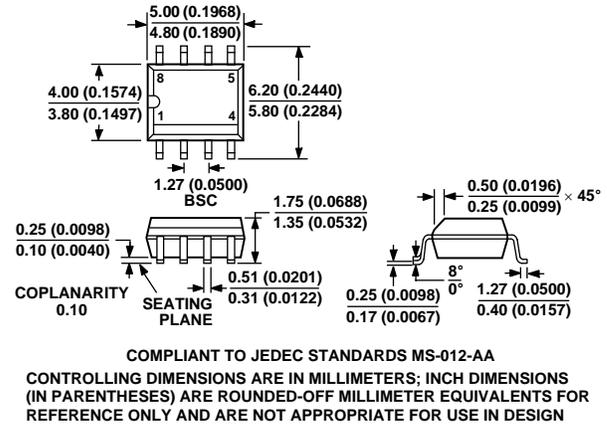
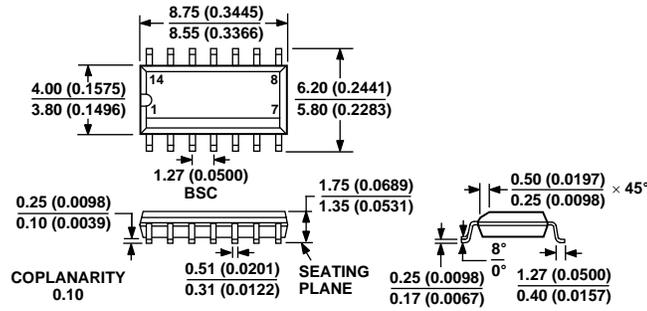


Figure 52. 8-Lead Standard Small Outline Package [SOIC-N] Narrow Body (R-8)  
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-012-AB  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 53. 14-Lead Standard Small Outline Package [SOIC\_N]  
 Narrow Body  
 (R-14)  
 Dimensions shown in millimeters and (inches)

**ORDERING GUIDE**

Model	Temperature Range	Package Description	Package Option	Branding Information
AD8531AKS-R2	-40°C to +85°C	5-Lead SC70	KS-5	A7B
AD8531AKS-REEL7	-40°C to +85°C	5-Lead SC70	KS-5	A7B
AD8531AKSZ-R2 <sup>1</sup>	-40°C to +85°C	5-Lead SC70	KS-5	A0Q
AD8531AKSZ-REEL7 <sup>1</sup>	-40°C to +85°C	5-Lead SC70	KS-5	A0Q
AD8531AR	-40°C to +85°C	8-Lead SOIC	R-8	
AD8531AR-REEL	-40°C to +85°C	8-Lead SOIC	R-8	
AD8531ARZ <sup>1</sup>	-40°C to +85°C	8-Lead SOIC	R-8	
AD8531ARZ-REEL <sup>1</sup>	-40°C to +85°C	8-Lead SOIC	R-8	
AD8531ART-REEL	-40°C to +85°C	5-Lead SOT-23	RT-5	A7A
AD8531ART-REEL7	-40°C to +85°C	5-Lead SOT-23	RT-5	A7A
AD8531ARTZ-REEL7 <sup>1</sup>	-40°C to +85°C	5-Lead SOT-23	RT-5	A0P
AD8532AR	-40°C to +85°C	8-Lead SOIC	R-8	
AD8532AR-REEL	-40°C to +85°C	8-Lead SOIC	R-8	
AD8532AR-REEL7	-40°C to +85°C	8-Lead SOIC	R-8	
AD8532ARZ <sup>1</sup>	-40°C to +85°C	8-Lead SOIC	R-8	
AD8532ARZ-REEL <sup>1</sup>	-40°C to +85°C	8-Lead SOIC	R-8	
AD8532ARZ-REEL7 <sup>1</sup>	-40°C to +85°C	8-Lead SOIC	R-8	
AD8532ARM-R2	-40°C to +85°C	8-Lead MSOP	RM-8	ARA
AD8532ARM-REEL	-40°C to +85°C	8-Lead MSOP	RM-8	ARA
AD8532ARMZ-R2 <sup>1</sup>	-40°C to +85°C	8-Lead MSOP	RM-8	A0R
AD8532ARMZ-REEL <sup>1</sup>	-40°C to +85°C	8-Lead MSOP	RM-8	A0R
AD8532ARU	-40°C to +85°C	8-Lead TSSOP	RU-8	
AD8532ARU-REEL	-40°C to +85°C	8-Lead TSSOP	RU-8	
AD8532ARUZ <sup>1</sup>	-40°C to +85°C	8-Lead TSSOP	RU-8	
AD8532ARUZ-REEL <sup>1</sup>	-40°C to +85°C	8-Lead TSSOP	RU-8	
AD8534AR	-40°C to +85°C	14-Lead SOIC	R-14	
AD8534AR-REEL	-40°C to +85°C	14-Lead SOIC	R-14	
AD8534ARZ <sup>1</sup>	-40°C to +85°C	14-Lead SOIC	R-14	
AD8534ARZ-REEL <sup>1</sup>	-40°C to +85°C	14-Lead SOIC	R-14	

# AD8531/AD8532/AD8534

Model	Temperature Range	Package Description	Package Option	Branding Information
AD8534ARU	-40°C to +85°C	14-Lead TSSOP	RU-14	
AD8534ARU-REEL	-40°C to +85°C	14-Lead TSSOP	RU-14	
AD8534ARUZ <sup>1</sup>	-40°C to +85°C	14-Lead TSSOP	RU-14	
AD8534ARUZ-REEL <sup>1</sup>	-40°C to +85°C	14-Lead TSSOP	RU-14	

<sup>1</sup> Z = Pb-free part.