Since April 1, 1999, Siemens Semiconductor is Infineon Technologies.
The next revision of this document will be updated accordingly.

ATTENTION

SIEMENS

ICs for Communications

ISDN Echocancellation Circuit
IEC-Q
PEB 2091 Version 4.3

User's Manual 02.95

PEB 2091 V4.3 Revision History:	Original Version: 09.94
Previous Releases:	02.95
Page	Subjects (changes since last revision)
	Update including appendix

Data Classification

Maximum Ratings

Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 ℃ and the given supply voltage.

Operating Range

In the operating range the functions given in the circuit description are fulfilled.

For detailed technical information about **"Processing Guidelines"** and **"Quality Assurance"** for ICs, see our **"Product Overview"**.

Table of Contents

- Vakat -

SIEMENS

ICs for Communications

ISDN Echocancellation Circuit

IEC-Q
PEB 2091

User's Manual 02.95

Vakat

Table of Contents

VAKAT

Contents **Page**

Contents (cont'd) **Page**

Contents (cont'd) **Page**

Contents (cont'd) **Page**

Contents (cont'd) **Page**

Contents (cont'd) **Page**

Contents (cont'd) **Page**

Contents (cont'd) **Page**

Contents (cont'd) **Page**

VAKAT

Introduction

The PEB 2091 Version 4.3 is a single-chip device which meets the newest American and European specifications.

This manual is divided into 6 major sections.

Section 1 gives the user an introduction to the PEB 2091 Vers. 4.3. It contains information about the functional blocks, features, and pinning of the IEC-Q.

Section 2 provides an overview of typical ISDN and non-ISDN-applications and demonstrates how these applications can be realized with the PEB 2091 Vers. 4.3.

Sections 3 and **4** are identical in structure. Both cover the major U-transceiver topics “Interfaces”, “Control Procedures” and “Maintenance Functions”. **Section 3** gives the user an overview on the discussed topics without going into technical details. It is intended as an application guide where the user can quickly look up how the registers of ICC, EPIC and IEC-Q Vers. 4.3 need to be programmed in order to initiate the desired action. Cross-references help to find further information on the discussed issue.

Section 4 is dedicated to detailed technical information. Status diagrams, state descriptions, algorithms, dynamic characteristics are to be found here. **Section 4** thus is intended for the user who seeks specific technical information.

Section 5 summarizes all electrical, **section 6** all environmental characteristics.

VAKAT

Technical Data

- Features
- System Integration
- Application Guide
- Technical Description
- Electrical Characteristics

VAKAT

Technical Data

Features

VAKAT

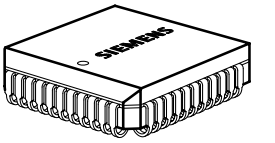
SIEMENS

ISDN Echocancellation Circuit (IEC-Q)

PEB 2091

CMOS IC

1 Features



P-LCC-44

Full duplex data transmission and reception at the U-reference point according to the following layer-1 specifications:

- Specification of the American National Standard Institute ANSI T1.601–1991
- CNET Specification Technique ST/LAA/ELR/DNP/822
- ETSI DTR/TM 3002
- Recommendation CCITT, G961
- 144 kbit/s user bit rate over a two-wire subscriber loop
- 2B1Q-block code (2 binary, 1 quaternary)
- 80-kHz symbol rate
- Activation and deactivation procedure
- Meets transmission requirements for loop #1 through loop #15 of ANSI's 15 telephone plant test loops
- Meets transmission requirements for loop #1 through #6 of CNET's 6 telephone plant test loops
- Meets transmission requirements for loop #1 through #8 of ETSI's 8 telephone plant test loops
- Built-in wake-up unit for activation from power-down state
- Adaptive echo cancellation
- Adaptive equalization
- Automatic polarity adaption
- Clock recovery (frame and bit synchronization) in all applications
- Automatic gain control
- Low power consumption:
  standby: max. 55/70 mW
  active: max. 350 mW
- P-LCC-44 package
- Extended temperature range (– 40 ... to 85 °C) available

Type	Version	Ordering Code	Package
PEB 2091	V 4.3	Q-67100-H6341	P-LCC-44 (SMD)
PEF 2091	V 4.3	Q-67106-H6380	P-LCC-44 (SMD)

IOM®-2-Interface

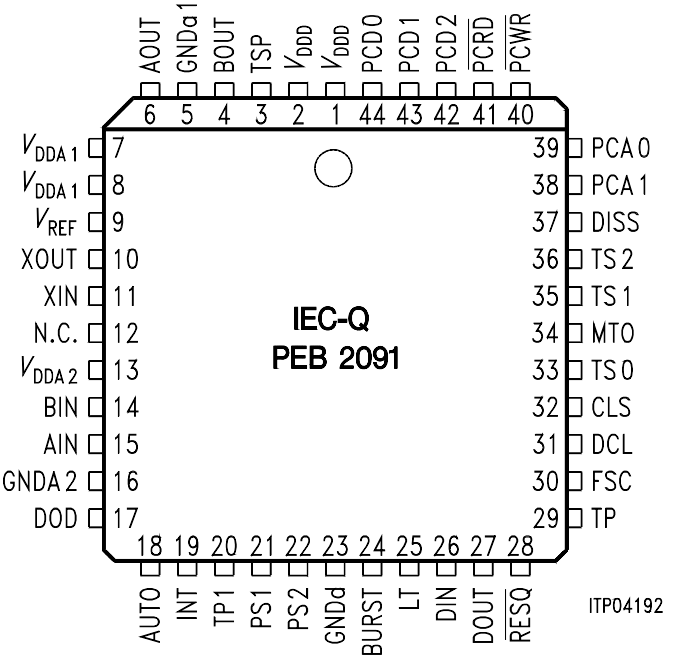
– Optimized for operation in conjunction with SBCX, ICC, EPIC®and IDEC® telecom ICs.
– Handling of commands and indications contained in the IOM®-2 C/I-channel for deactivation, activation, supervision of power supply unit and equipment for testing.
– Data available via MONITOR channel on:
  CRC-transmission errors
  Loop current
  Echo canceler coefficients and internal status
– Switching of test loops.
– Generation of synchronized 7.68-MHz clock for SBCX in NT-mode.
– Generation of all IOM®-clock signals in LT-mode for DAML-applications.

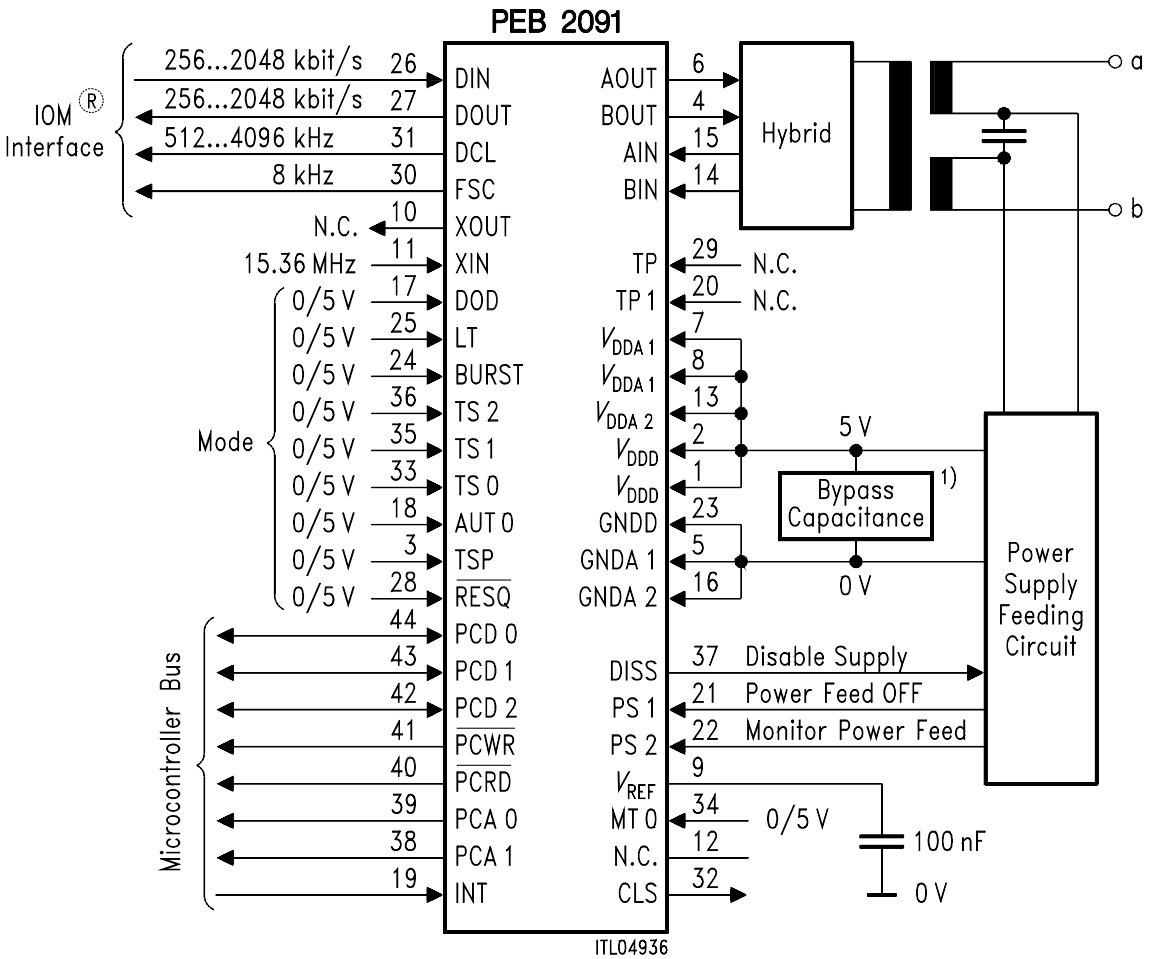
Modes

– Adaptation of internal interfaces by programmable modes of operation:

LT:	Line termination in public or private exchange
LT-RP:	Repeater connected to NT or TE
COT-512:	DAML-mode for central office terminal with 512 kHz DCL
COT-1536:	DAML-mode for central office terminal with 1.5 MHz DCL
TE:	Terminal mode
NT:	Network termination connected to SBCX
NT-Auto:	As NT but with automatic activation after “Reset”
NT-PBX:	Trunk module (TDM)
NT-RP:	Repeater connected to LT

Pin Configuration
(top view)





Logic Symbol

1.1 Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
Power Supply Pins			
1, 2	V_{DDD}	I	5 V ± 5 % digital supply voltage
5	GNDA1	I	0 V analog
7, 8	V_{DDA1}	I	5 V ± 5 % analog supply voltage
9	V_{REF}	O	V_{REF} pin to buffer internally generated voltage with capacitor 100 nF vs GND
13	V_{DDA2}	I	5 V ± 5 % analog supply voltage
16	GNDA2	I	0 V analog
23	GNDD	I	0 V digital
Mode Selection Pins			
3	TSP	I	Single pulse test mode. For activation refer to **table 2**. When active, alternating 2.5 V pulses are issued in 1.5 ms intervals. Clamp to GND if not used.
18	Auto	I	Selection between auto- and transparent mode for EOC channel processing. (Automode = (1))
24	Burst	I	Selection of burst modes (LT, NT-PBX) with (1) and non-burst modes (NT, TE, COT-512/1536, LT/NT-RP) with (0)
25	LT	I	Selection of LT-modes LT, COT-512/1536, LT-RP (1) and non LT-modes NT, TE, NT-PBX, NT-RP (0)
33	TS0	I	Time-slot. IOM-2 channel selection for burst mode. LSB active high
35	TS1	I	Time-slot. IOM-2 channel selection for burst mode. Active high
36	TS2	I	Time-slot. IOM-2 channel selection for burst mode. MSB active high
28	$\overline{\text{RESQ}}$	I	Power-on reset, active (0) (for activation-conditions refer to table 2), must be (0) at least for 10 ns. The RESET in the LT and NT-PBX mode will be applied only after the clock on the IOM is applied. Clamp to (1) if not used.

Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
Power Controller Pins			
44	PCD0	I/O	Data bus of power controller interface. LSB. Do not connect if not used. Internal pull-up.
43	PCD1	I/O	Data bus of power controller interface. Do not connect if not used. Internal pull-up.
42	PCD2	I/O	Data bus of power controller interface. MSB. Do not connect if not used. Internal pull-up.
39	PCA0	O	Address bus of power controller interface.
38	PCA1	O	Address bus of power controller interface.
41	$\overline{\text{PCRD}}$	O	Power controller interface read request. Active (0).
40	$\overline{\text{PCWR}}$	O	Power controller interface write request. Active (0).
19	INT	I	Interrupt. Change-sensitive. After a change of level has been detected the C/I code "INT" will be issued on IOM. Clamp to (0) during operation.
37	DISS	O	Disable power supply. Different function in LT and NT modes. LT: the DISS pin is set to (1) with the C/I command "LTD". NT: the DISS pin is set to (1) after receipt of MON-0 LBBD in auto-mode.
21	PS1	I	Power status (primary). Different function in LT- and NT-mode. LT: (1) indicates that the remote power is switched off. (1) on PS1 results in C/I message "HI". Clamp to low if not used. NT: (1) indicates that prim. power supply is ok. The pin value is identical to the overhead bit "PS1" value.
22	PS2	I	Power status (secondary). Different function in LT- and NT-mode. LT: the current feed value is transmitted (8 bit serially) from a power controller. Read the value with MON-8 "RPFC". NT: (1) indicates that secondary power supply is ok. The pin value is identical to the overhead bit "PS2" value.

Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
Miscellaneous Function Pins			
10	XOUT	O	Crystal OUT. 15.36-MHz crystal is connected with 30 pF in parallel.
11	XIN	I	Crystal IN. External. 15.36-MHz clock signal or 15.36-MHz crystal with 30 pF in parallel is connected.
17	DOD	I	Dout open drain. Select open drain with DOD = (1) (external pull-up resistor required) and tristate with DOD = (0).
29	TP	I	Test pin. Not available to user. Do not connect. Internal pull-down resistor.
20	TP1	I	Test pin. Not available to user. Do not connect. Internal pull-down resistor.
32	CLS	O	Clock Signal. In the LT-, COT-, and NTRP-modes the 15.36 MHz master clock is provided on this pin. In all other NT-Modes this clock is synchronized to U-Interface. Used to synchronize external PLL or to clock S-Interface devices. In the NT- and TE-modes a 7.68MHz clock is provided on this pin. In the PBX- and in the LT-RP-Modes a 512 KHz is provided.
12	N.C.	I/O	Not connected. Do not connect this pin externally in order to guarantee upward compatibility.
34	MTO	I	Monitor procedure timeout. Disables the internal 6 ms monitor timeout when set to (1). Internal pull-down resistor.
IOM®-Pins			
31	DCL	I/O	Data clock. Clock range 512 kHz to 4096 kHz.
30	FSC	I/O	Frame synchronization clock. The start of the B1-channel in time-slot 0 is marked. FSC = (1) for one DCL-period indicates a superframe marker. FSC = (1) for at least two DCL-periods marks a standard frame.
26	DIN	I	Data in. Input of IOM-data synchronous to DCL-clock. Corresponds to DD (data downstream) in LT and DU (data upstream) in NT-applications.
27	DOUT	O	Data out. Output of IOM-data synchronous to DCL-clock. Corresponds to DD (data downstream) in NT and DU (data upstream) in LT-applications.

Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
U-Interface Pins			
15	AIN	I	Differential U-Interface input. Connect to hybrid.
14	BIN	I	Differential U-Interface input. Connect to hybrid.
6	AOUT	O	Differential U-Interface output. Connect to hybrid.
4	BOUT	O	Differential U-Interface output. Connect to hybrid.

1.2 Functional Block Diagram

The IEC-Q can be subdivided into three main blocks:

SIU	System Interface Unit
REC	Receiver
LIU	Line Interface Unit

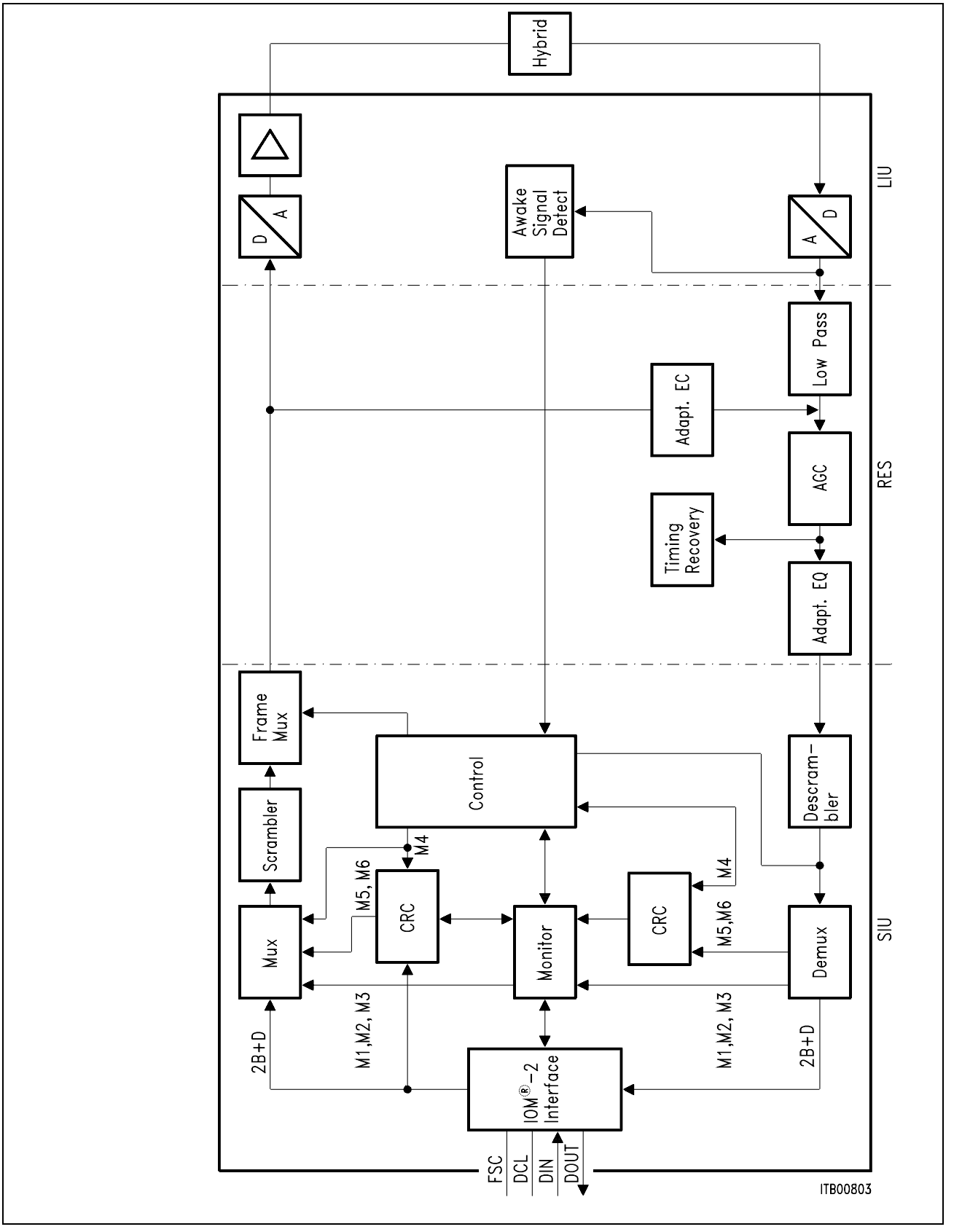


Figure 1
Block Diagram of IEC-Q

The Line Interface Unit (LIU) contains the crystal oscillator and all of the analog functions, such as the A/D-converter and the awake unit in the receive path, the pulse-shaping D/A-converter, and the line driver in the transmit path.

The System Interface Unit (SIU) provides the connection of the U- and the IOM-interfaces. After scrambling/descrambling and rate adaptation the data channels (2B + D) are transferred to the appropriate frame. Complete activation and deactivation procedures are implemented, which are controlled by activation and deactivation indications from U- or IOM-interfaces. State transition of the procedures depend on the actual status of the receiver (adaptation and synchronization) and timing functions to watch fault conditions. Two different modes can be selected for maintenance functions: In the auto-mode all EOC-procedure handling and executing as specified by ANSI is performed. In the transparent mode all bits are transferred transparent to the IOM-interface without any internal processing.

The Receiver block (REC) performs the filter algorithmic functions using digital signal processing techniques. Modules for echo cancellation, pre- and post-equalization, phase adaptation and frame detection are implemented in a modular multi-processor concept.

Technical Data

System Integration

VAKAT

2 System Integration and Applications

Different hardware configurations as well as different operating modes of the IEC-Q Vers. 4.3 are selectable to cope with different system requirements. The following is an overview of typical layer-1 applications. It shows how the IEC-Q is integrated in systems using other Siemens ISDN devices and how the PEB 2091 is electrically connected. The chapter concludes with a summary of the clock generation methods applied in the described systems.

2.1 Operational Modes and System Integration

2.1.1 LT-Application

An LT-configuration with up to 8 IEC-Q devices can be built with an EPIC and two IDECs. The EPIC controls the C/I-channel, the B-channel slot assignment and the MONITOR channel handling. The IDEC is a HDLC-controller for four independent D-channels.

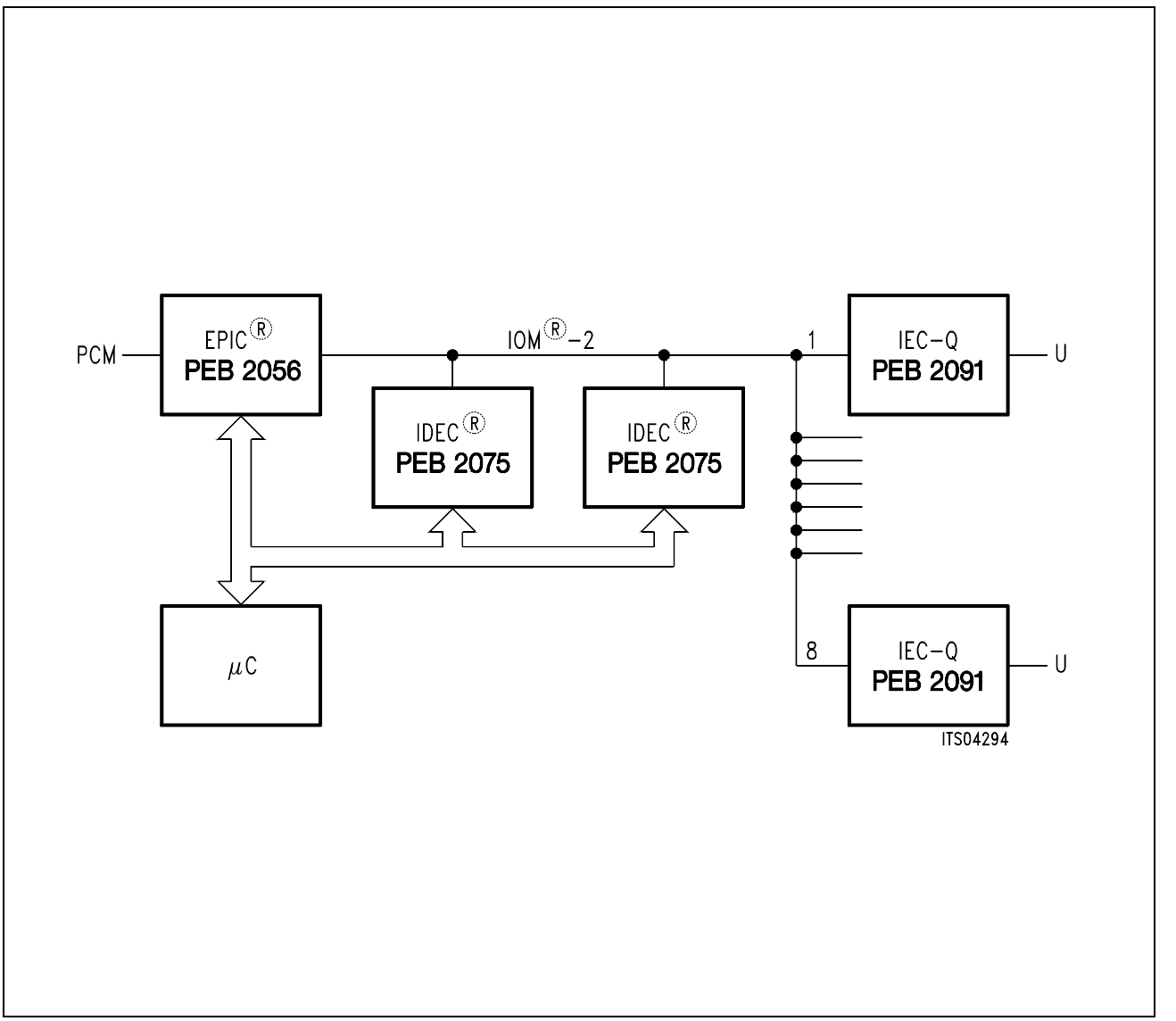
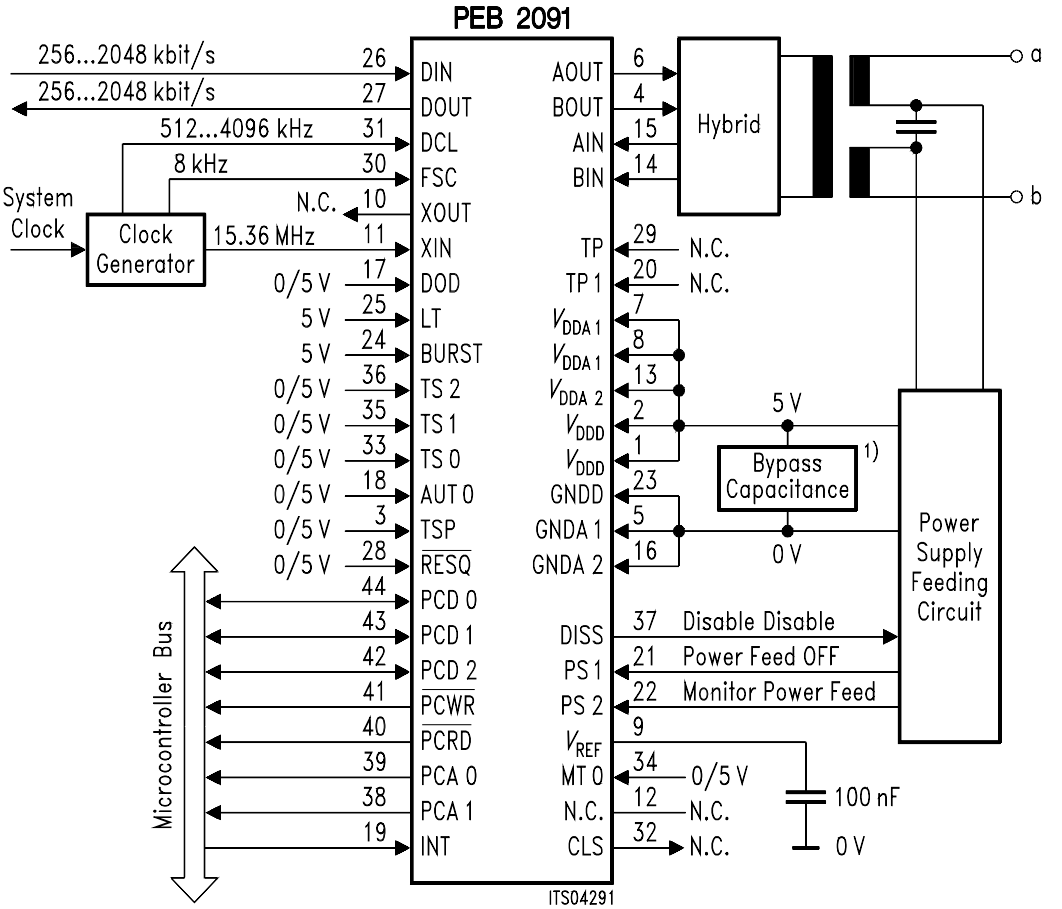
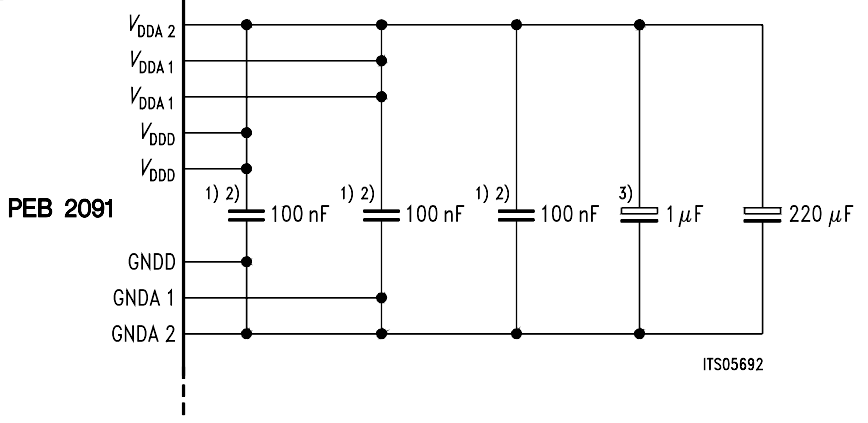


Figure 2
LT-Application



1) **Detail of Figure 3**
Bypass Capacitance



1) These capacitors should be located as near as possible to PEB 2091

2) MKT-stack film capacitors

3) Tantalum electrolytic capacitor

Figure 3
IEC-Q in LT-Mode

2.1.2 NT-Application

By using the SBCX (four-wire S/T-bus interface) a complete NT1 Network Termination can be built with only two devices. For a more complex and microcontrolled NT, the ICC is used to provide layer-1 maintenance functions.

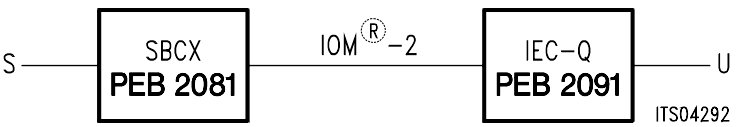


Figure 4
NT-Application

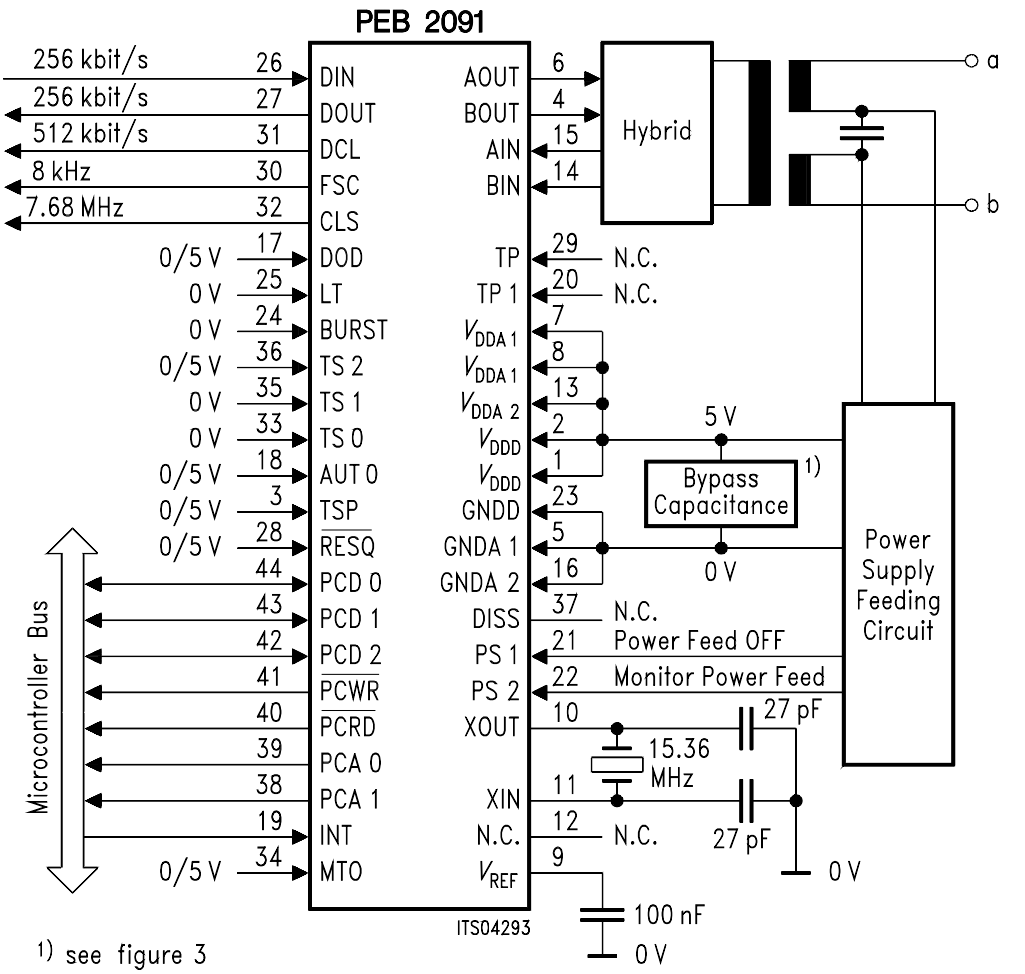


Figure 5
IEC-Q in NT-Mode

2.1.3 NT-PBX-Application

The basic timing is generated by the IEC-Q.

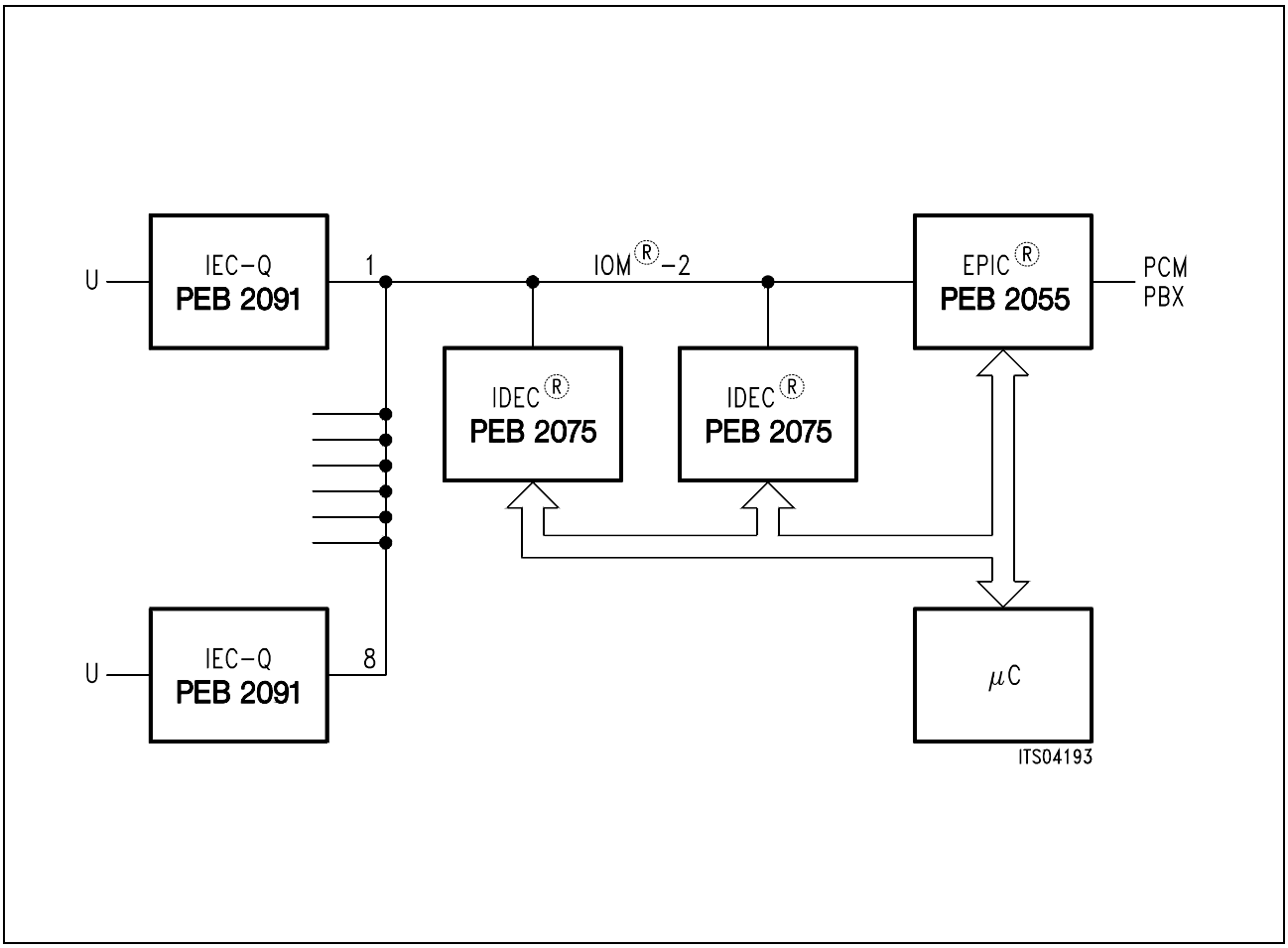


Figure 6
NT-PBX-Application

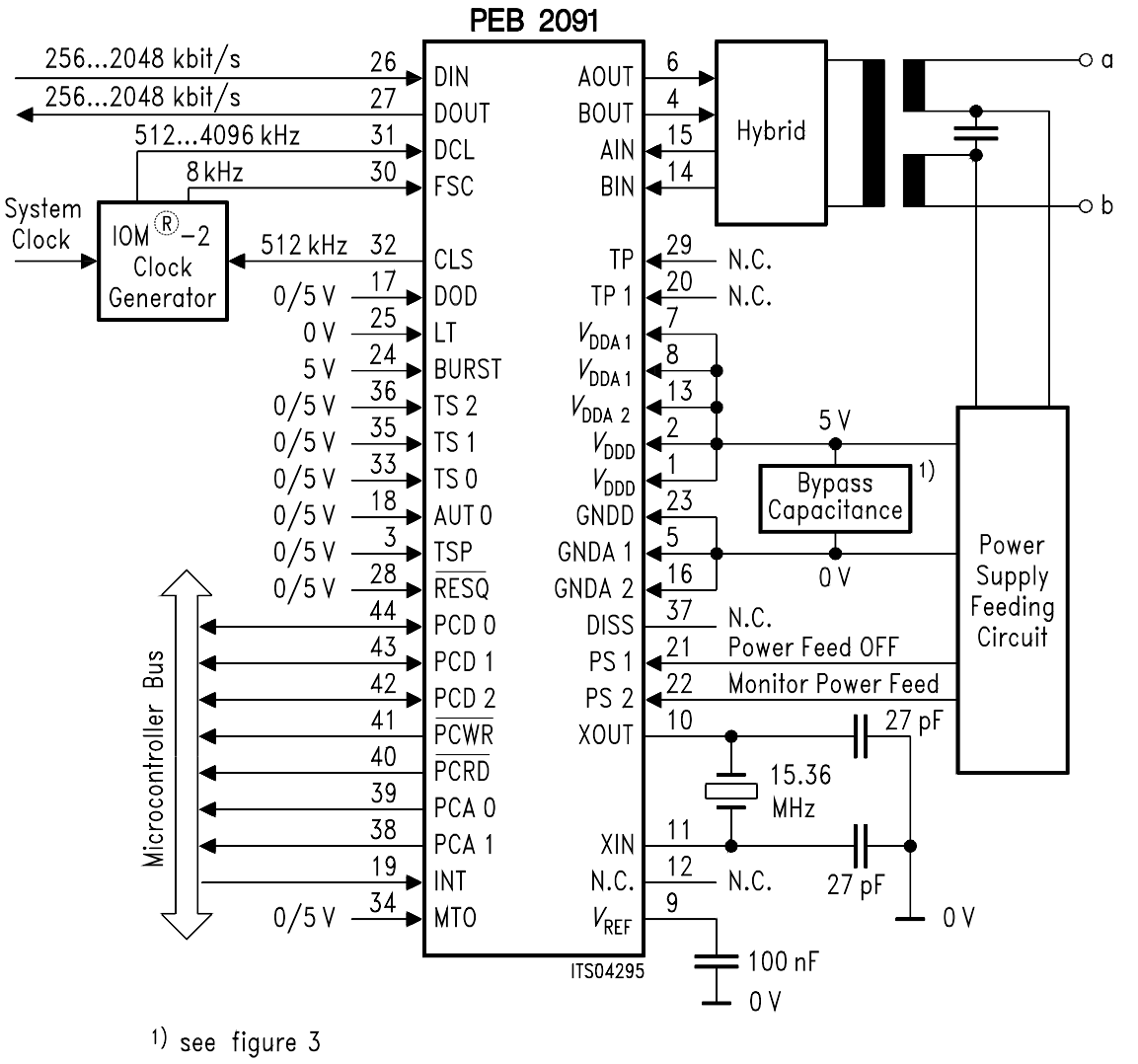


Figure 7
IEC-Q in NT-PBX-Mode

2.1.4 TE-Application

With voice/data modules such as ITAC® Terminal Adapter Circuit or ARCOFI® Audio Ringing Codec Filter, a complete TE-configuration can be built in a cost-effective manner. Three IOM-channels are used, the IOM-data clock is fixed at 1.536 MHz.

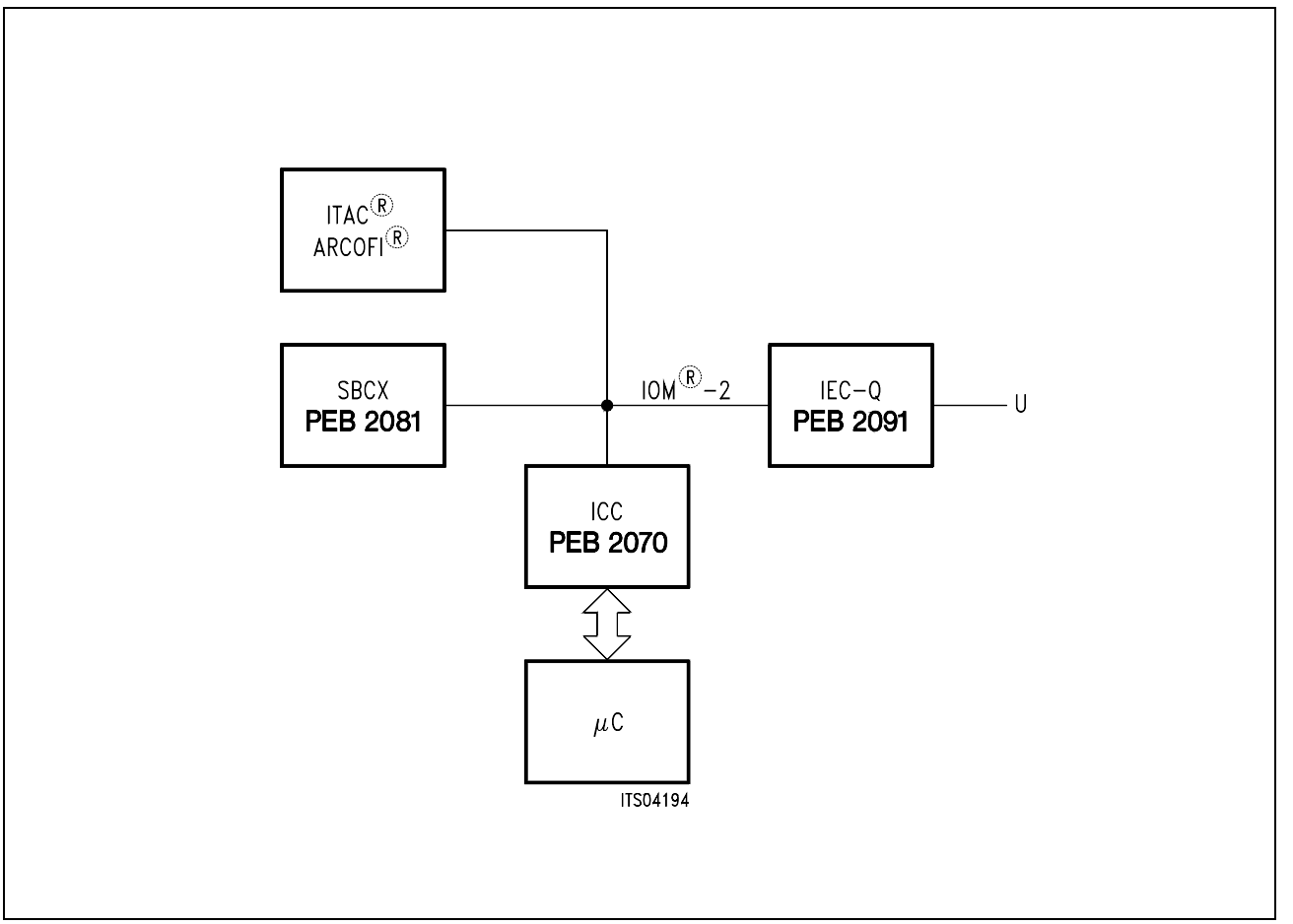


Figure 8
TE-Application

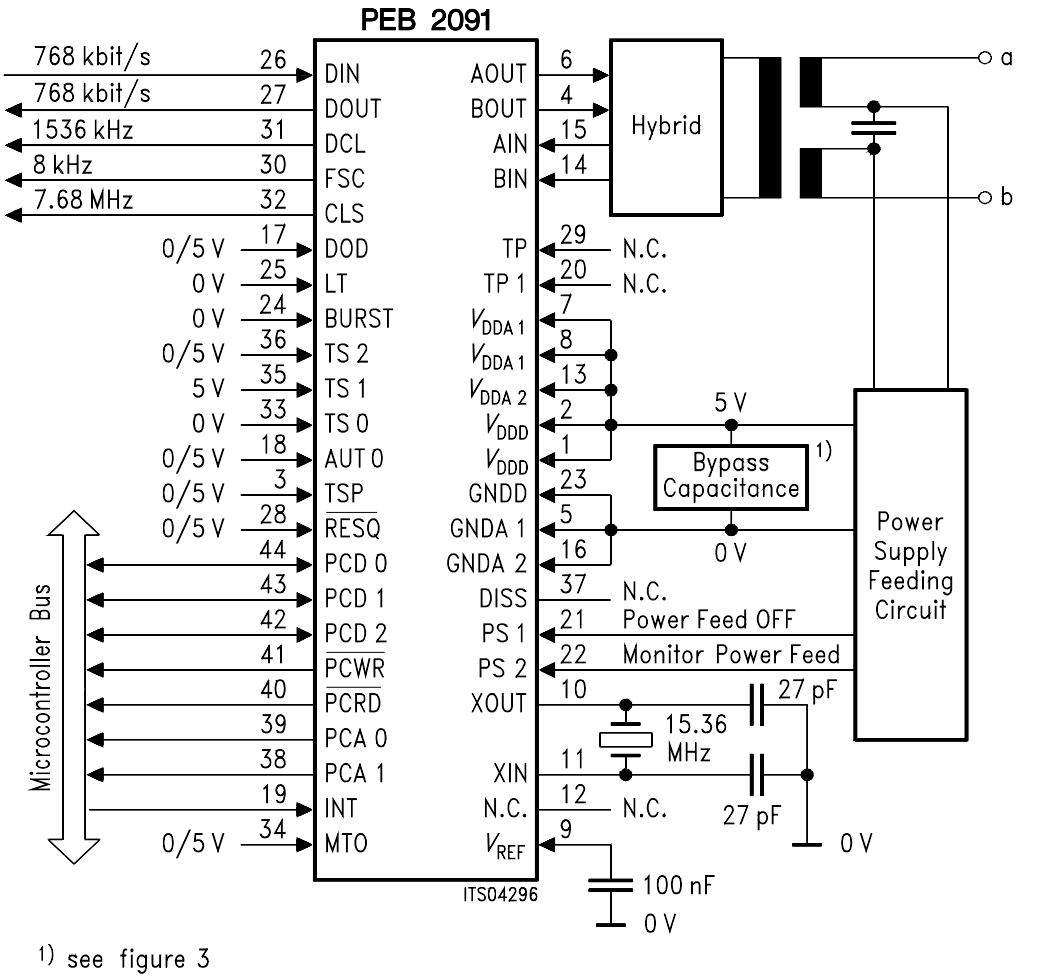


Figure 9
IEC-Q in TE-Mode

2.1.5 Repeater Application

With an additional repeater control unit, two IEC-Qs can easily build a U-repeater. Most of the additional repeater functions are performed within the repeater control unit. It has to be defined according to national standards.

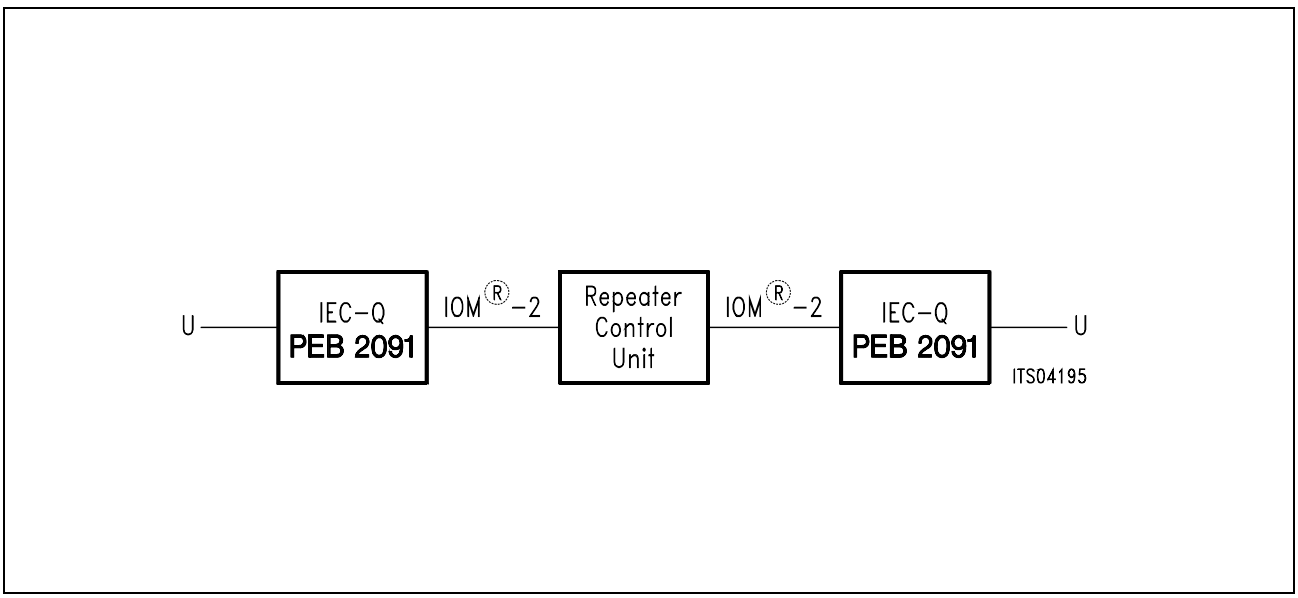


Figure 10
Repeater Application

A proposed connection is shown in **figure 11**.

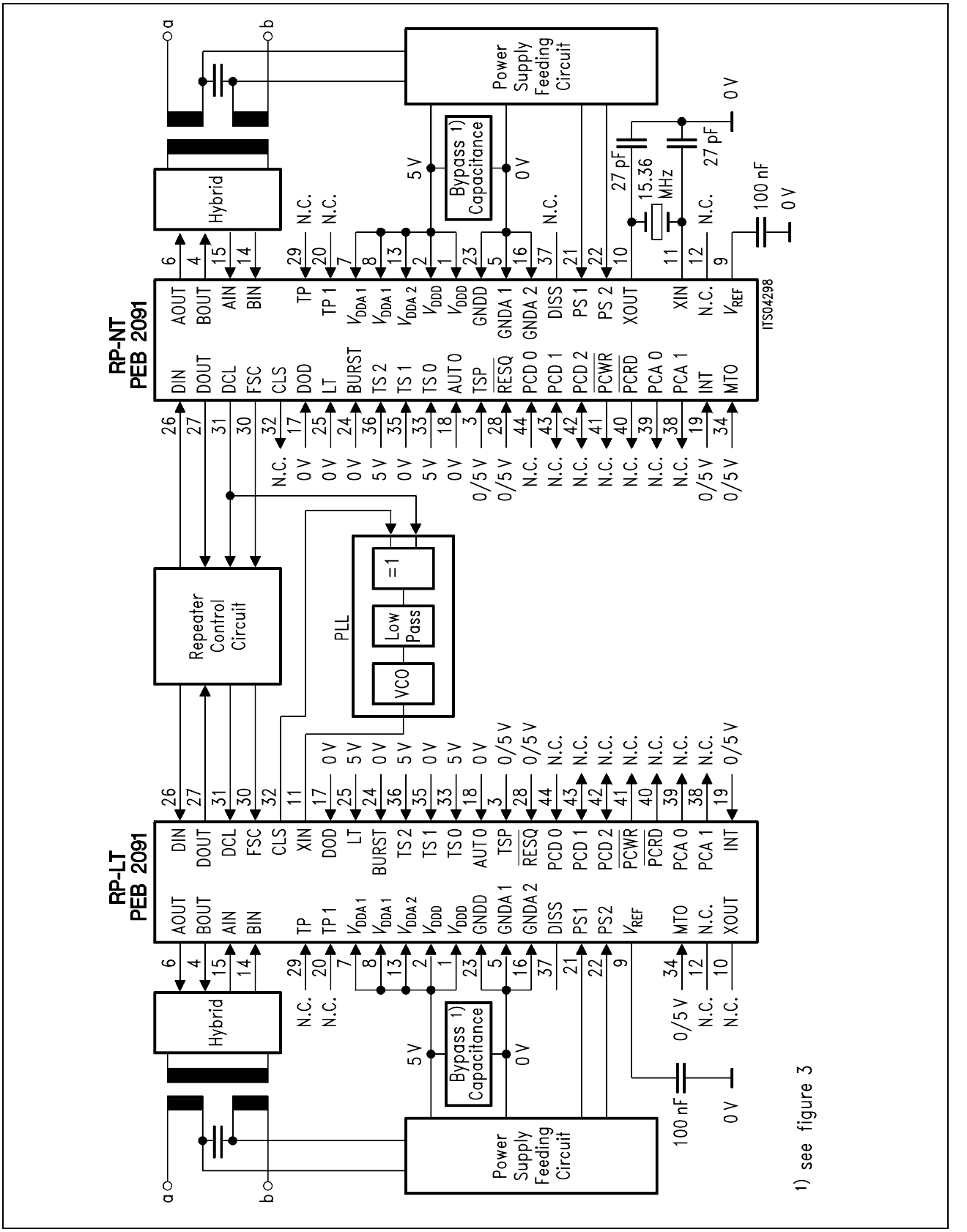


Figure 11
IEC-Q in Repeater Mode

2.1.6 Digital Added Main Line (Pair Gain)

The most common non-ISDN application the IEC-Q is used for is the Digital Added Main Line (DAML). With a DAML-system only one copper wire pair is required to transmit the data of two analog line pairs. The central office terminal (COT) transforms the two analog signals into a digital data stream by means of a SICOFI® -2. One B-channel is allocated for each analog line pair. The IEC-Q transmits the data to a remote terminal (RT) where it is reconverted into the original analog signals with a SICOFI-2 and two SLICs.

For the COT two solutions are proposed. The first concept is based on one COT-station for each line pair. This concept is supported with the COT-512/1536 mode of the IEC-Q.

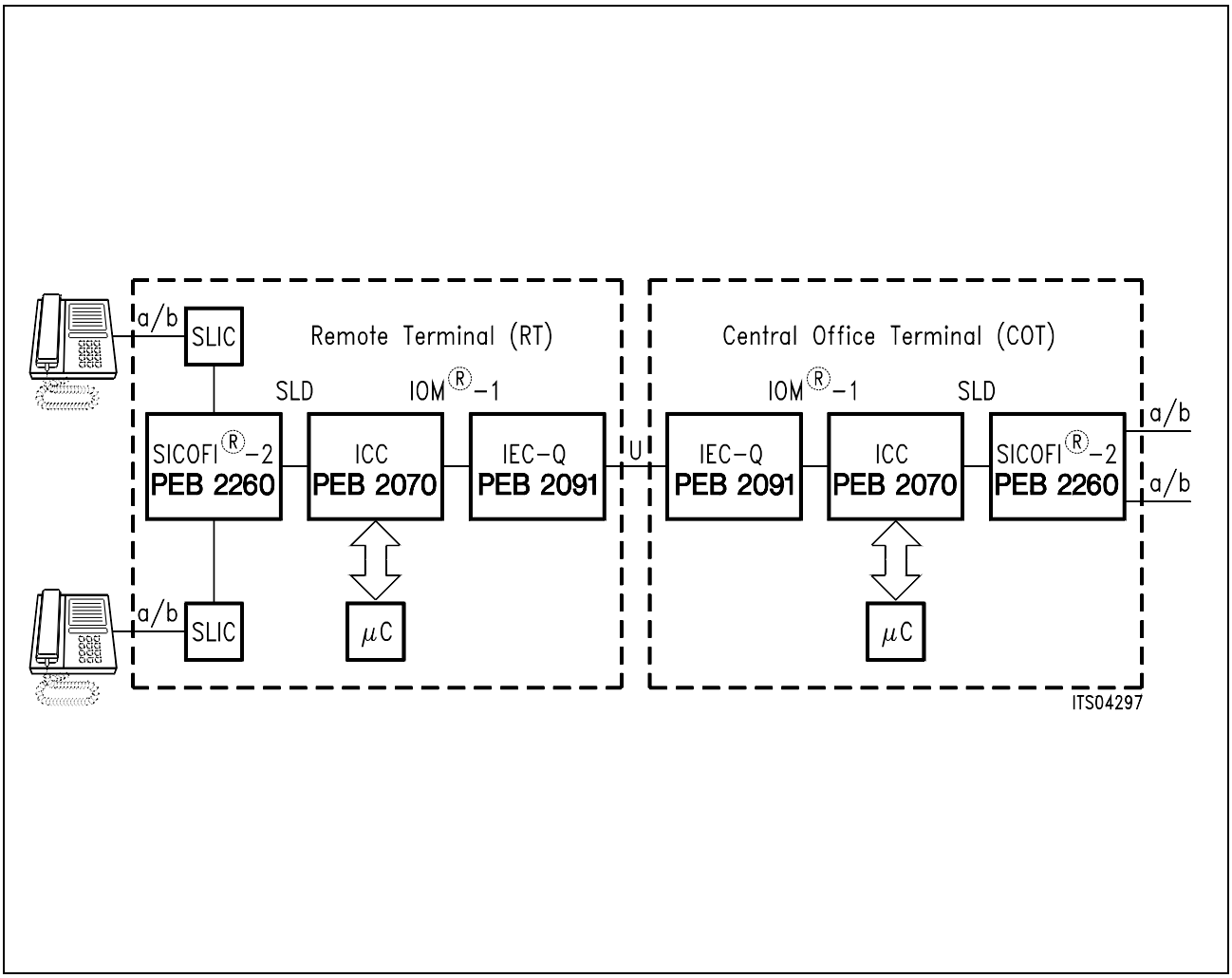


Figure 12
DAML-Concept 1

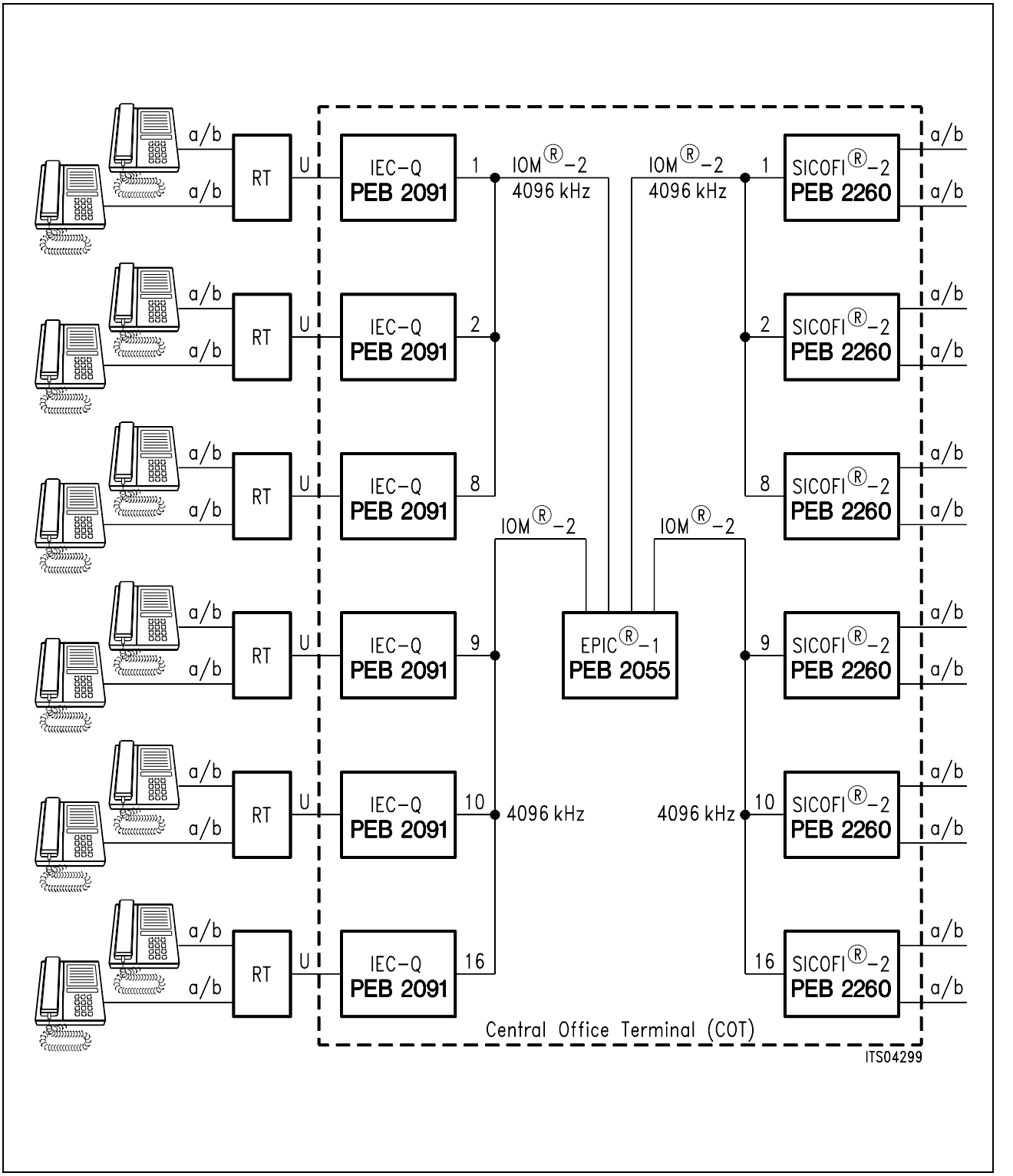


Figure 13
DAML-Concept 2

Figure 13 depicts a very economical approach utilizing one EPIC-1 to control 16 IEC-Qs and SICOFI-2s for 32 analog line pairs. The IEC-Q is operating in the standard LT-mode with 4096-kHz DCL-clock rate.

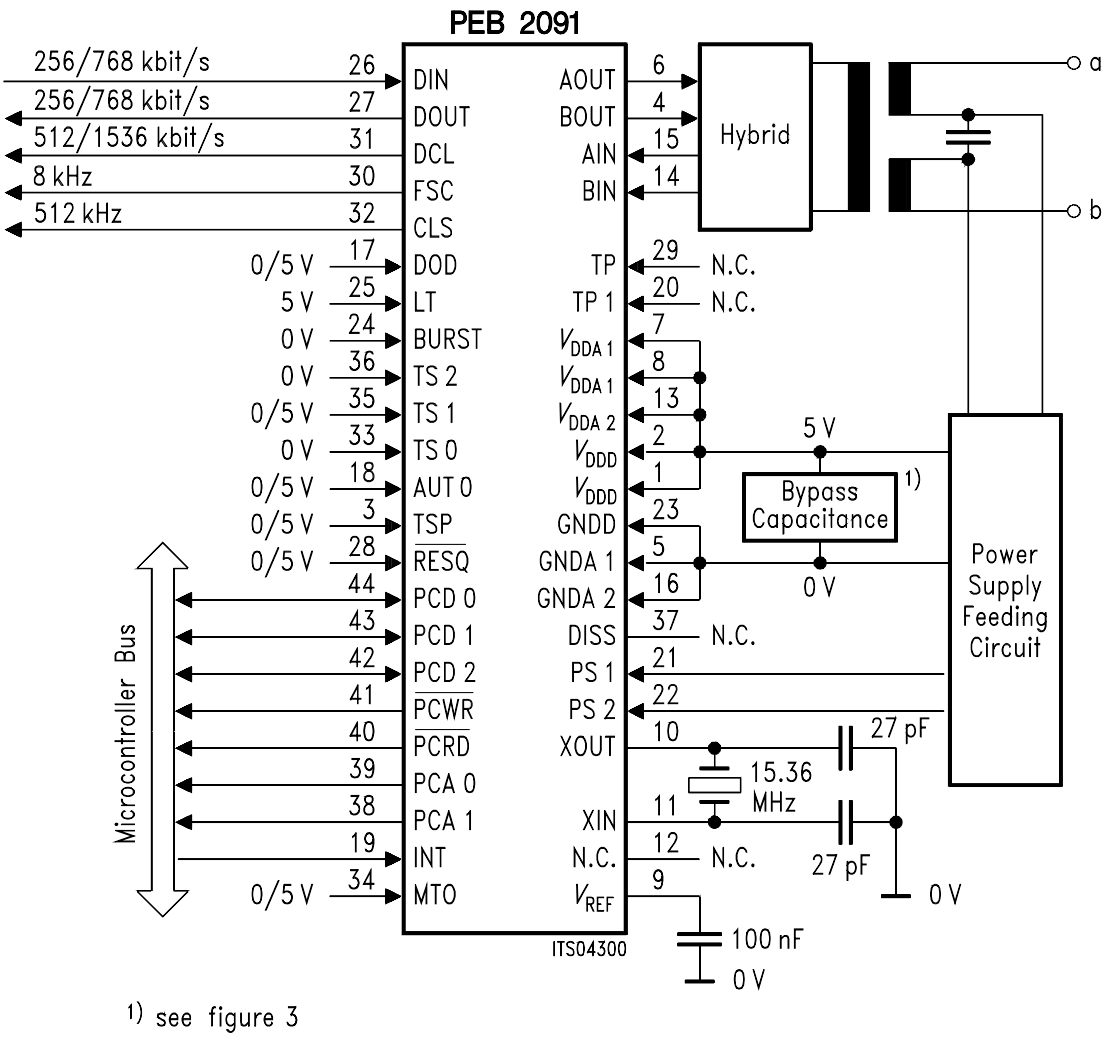


Figure 14
IEC-Q in COT-512/1536 Mode

2.2 Setting Operating Modes

Tables 1 to 5 illustrate what modes are supported by the PEB 2091 Vers. 4.3 and how they are configured by the user.

It is possible to change the mode of a device during operation (e.g. for test purposes) if the mode change is followed by a reset.

Table 1
Modes of Operation

	Input Pins						**Output Pins U Synchronized**		
Mode	**Burst**	**LT**	**TS2**	**TS1**	**TS0**	**DCL IN**	**DCL OUT**	**CLS OUT**	**Super-frame-marker**[1)]
NT	0	0	0	0	0	–	512	7680[2)]	no
NT	0	0	1	0	0	–	512	7680[2)]	yes
NT-AUTO	0	0	0	0	1	–	512	7680[2)]	no
TE	0	0	0	1	0	–	1536	7680[2)]	no
TE	0	0	1	1	0	–	1536	7680[2)]	yes
PBX	1	0	IOM-2 channel assignment (**table 4**)			512-4096	–	512[2)]	–
LT	1	1	IOM-2 channel assignment (**table 4**)			512-4096	–	512[3) 4)]	–
COT-512	0	1	0	0	0	–	512	512[3) 4)]	no
COT-1536	0	1	0	1	0	–	1536	512[3) 4)]	no
LT-RP	0	1	1	0	1	512	–	512[3)]	–
NT-RP	0	0	1	0	1	–	512	7680[2)]	yes

Notes: [1)] 1 DCL-period high-phase of FSC at superframe position
2 DCL-periods high-phase of FSC at normal position
[2)] CLS-clock signal not available while device is in power-down
[3)] CLS-clock signal available while device is in power-down
[4)] This clock may be changed in further versions of the IEC-Q

Table 2
Test Modes

Test-Mode	RESQ Pin	TSP Pin
Master-Reset	0	0
Send Single-Pulses	1	1
Data-Through	0	1

Table 3
EOC Mode

EOC-Mode	Input Pin AUTO
Transparent	0
Automatic	1

Table 4
IOM®-2 Channel Assignment *)

IOM®-2 Channel No.	TS2	TS1	TS0	Bit No.	Min. Frequency of DCL (kHz)
CH 0	0	0	0	0 … 31	512
CH 1	0	0	1	32 … 63	1024
CH 2	0	1	0	64 … 95	1536
CH 3	0	1	1	96 … 127	2048
CH 4	1	0	0	128 … 159	2560
CH 5	1	0	1	160 … 191	3071
CH 6	1	1	0	192 … 223	3584
CH 7	1	1	1	224 … 255	4096

Note: *) TS pins are read continuously (non-latching) after the supply voltage has reached its nominal value.

Table 5
DOUT-Modes

Mode	RESQ	TSP	DOD	DOUT	DOUT in Slot Position	DOUT not in Slot Position
Master Reset	0	0	x	0	low	int. pull-up
Master Reset	0	0	x	1	int. pull-up	int. pull-up
Tristate	1	0	0	0	low	high Z
Open Drain [1)]	1	0	1	0	low	floating
Tristate	1	0	0	1	high	high Z
Open Drain [1)]	1	0	1	1	floating	floating

Note: [1)] External pull-up resistors required (typ.1 kΩ)

2.3 Clock Generation

Clock generation varies with the application. The following diagrams show what timing signals need to be generated for each IEC-Q-mode and how system synchronization is obtained.

2.3.1 LT-Mode

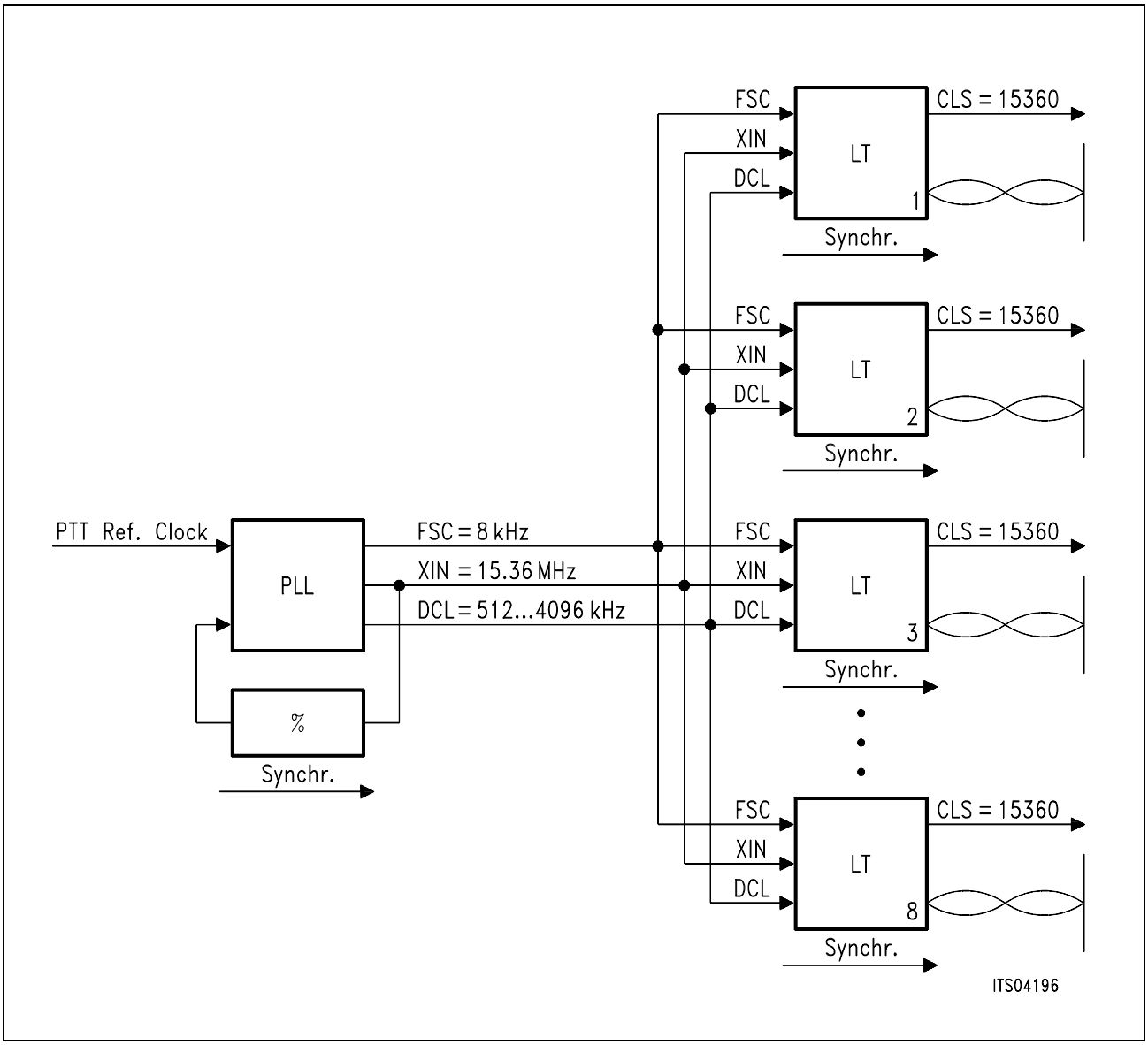


Figure 15
Clock Generation for LT-Mode

LT-mode is typically chosen in ISDN-line card applications. The U-transceiver has to synchronize onto an externally provided PTT-master clock. A phase locked loop (PLL) is required to generate the IOM-clock signals “FSC” (Frame Synchronization) and “DCL” (Data Clock) as well as the 15.36 MHz IEC-Q-system clock. A synchronized IEC-Q system clock guarantees that U-interface transmission will be synchronous to the PTT-master clock. Detailed information regarding delay and jitter requirements of the PLL are presented in **section 4.5**.

2.3.2 NT- and TE-Mode

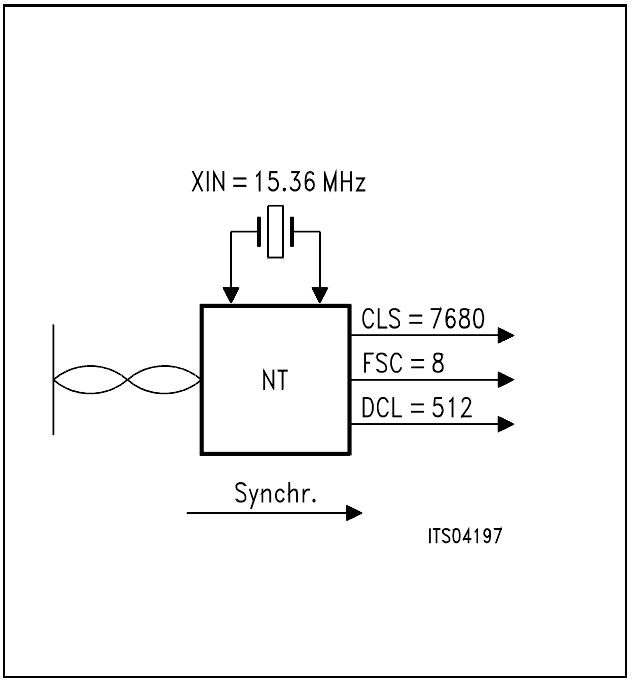


Figure 16
Clock Generation for NT-Mode

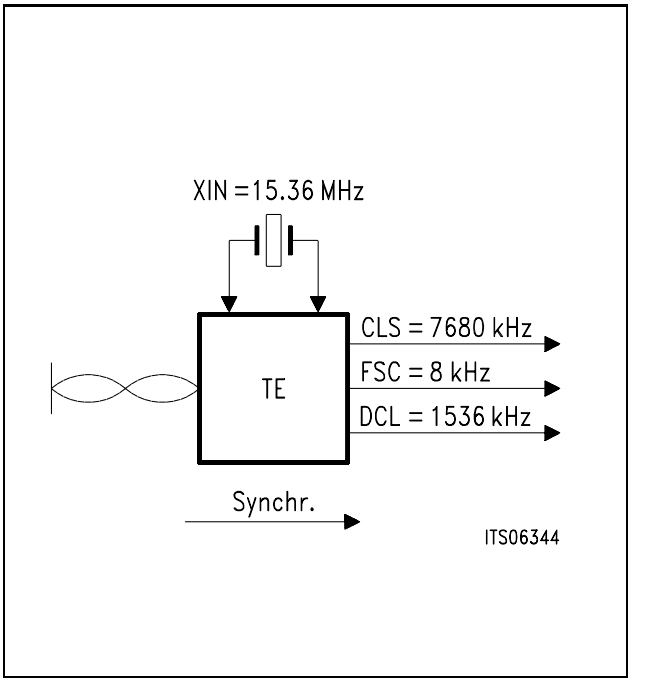


Figure 17
Clock Generation for TE-Mode

In NT- and TE-modes the PEB 2091 recovers the timing directly from the U-interface. A free running crystal or other clock source is to provide a 15.36-MHz base clock. The device synchronizes in both modes onto the U-interface by including correction steps in the divider of the 15.36-MHz base clock (**see section 4.5**). Thus the issued IOM-clock signals are synchronous to the PTT-master clock on LT-side. In NT-mode the DCL-rate is 512 kHz, in case of the TE-mode 1536 kHz.

2.3.3 NT-PBX

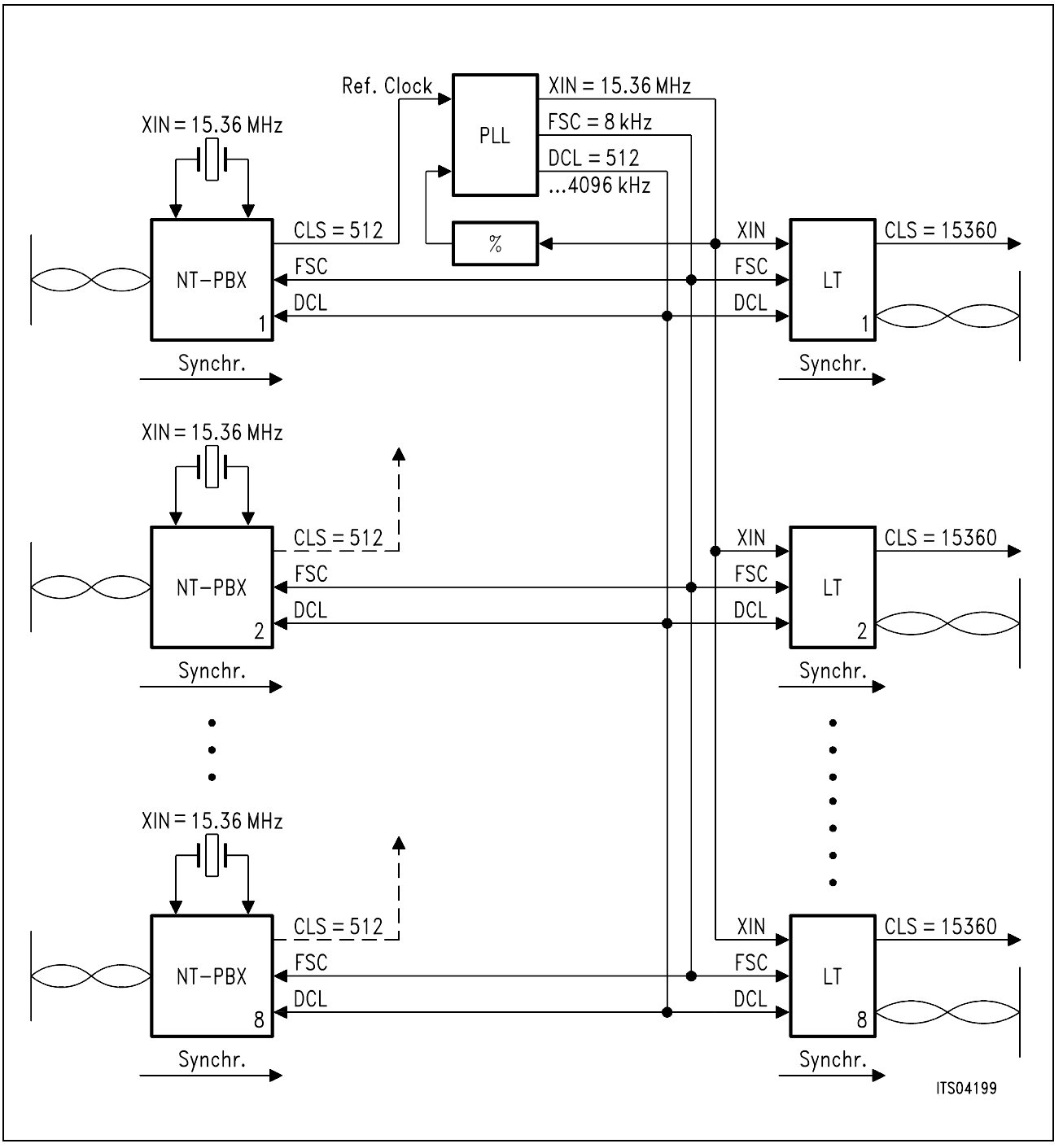


Figure 18
Clock Generation in NT-PBX-Mode

In NT-PBX-mode IOM-clock signals are not issued by the device but need to be generated externally. In order to ensure synchronous timing to the PTT-master clock, a PLL is used for generation of FSC and DCL (supplied to NT-PBX- and LT-devices) as well as of the 15.36-MHz system clock (LT only). Reference clock for the PLL is the PTT synchronous 512-kHz signal from pin CLS.

Note: It may be necessary to use a multiplexer for the PLL-reference clock because the CLS-signal is available only if the corresponding line is activated. Otherwise the PLL must be supplied by the CLS of another activated IEC-Q of the PBX.

2.3.4 Repeater Modes

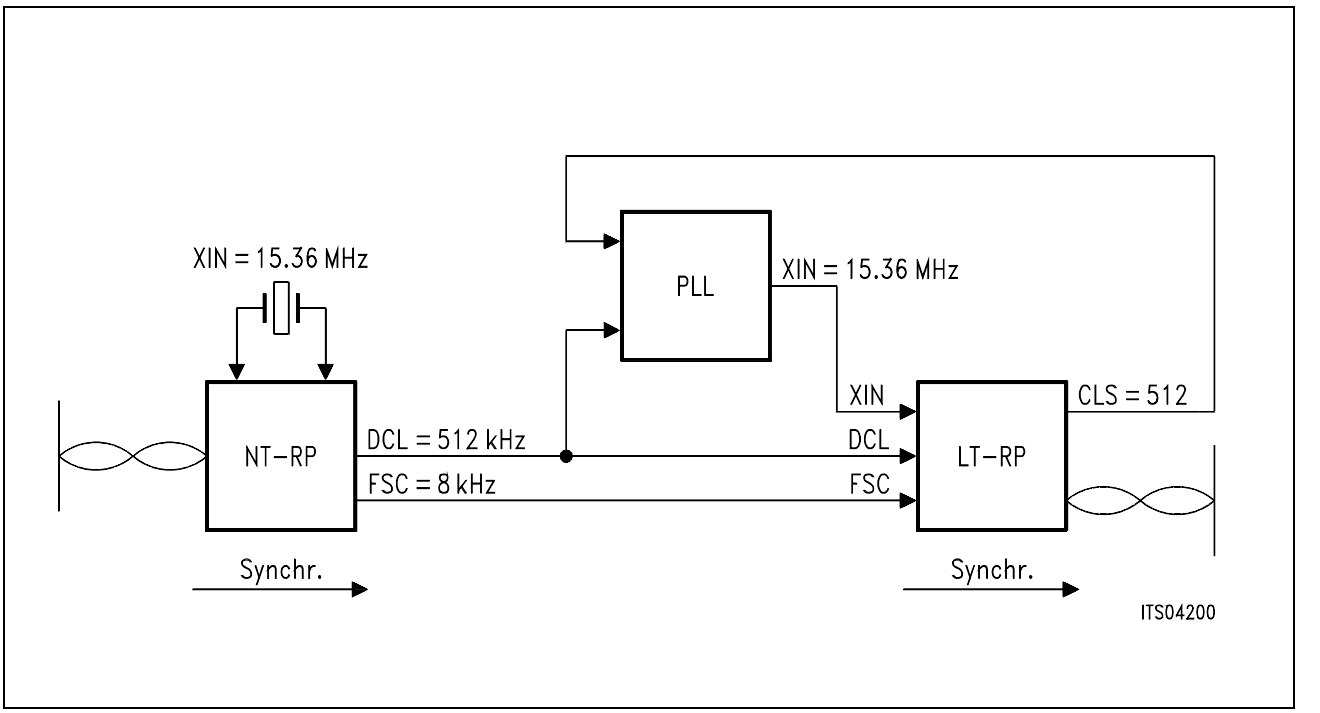


Figure 19
Clock Generation in Repeater Mode

The NT-RP issues IOM-clocks for direct use in the LT-RP. For generation of the 15.36-MHz LT-RP system clock, an external PLL is required as in NT-PBX-mode.

2.3.5 COT-512- and COT-1536-Mode

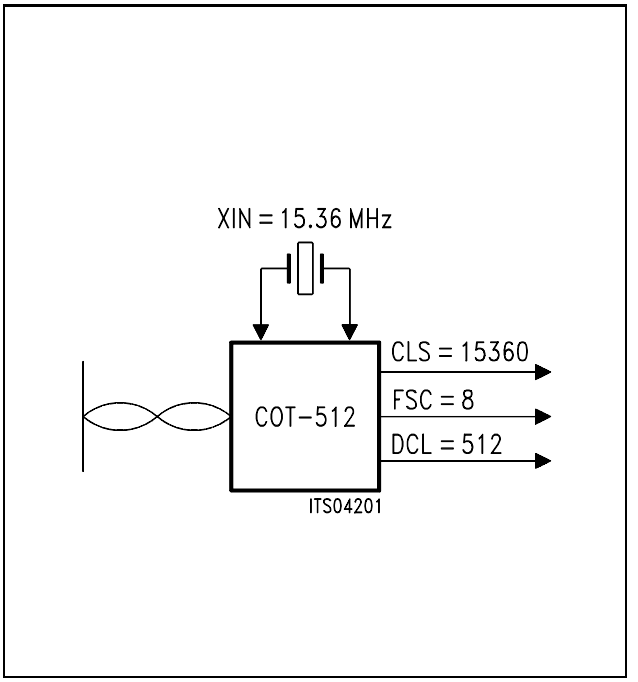


Figure 20
Clocks in COT-512-Mode

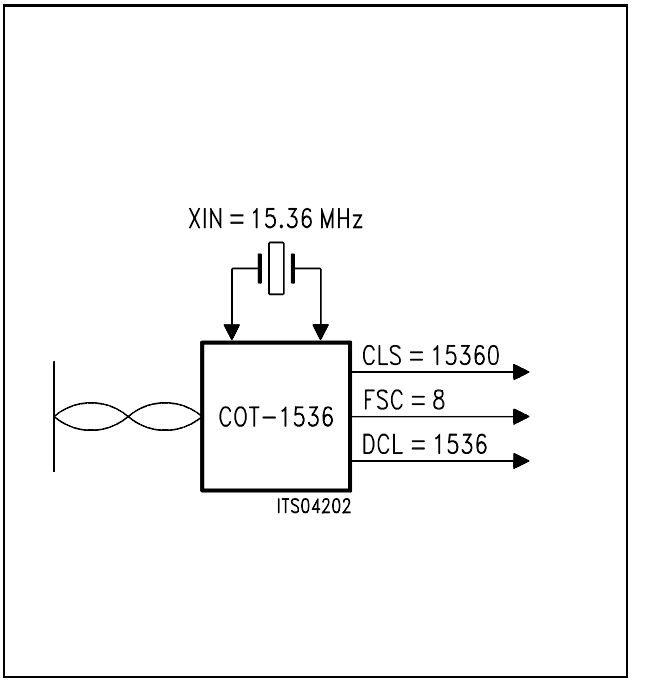


Figure 21
Clocks in COT-1536-Mode

In order to reduce the amount of external components required for pair gain applications, a COT-mode has been implemented in the IEC-Q Vers. 4.3. Because pair gain systems do not need to synchronize onto a PTT-master clock, at the exchange side a free running 15.36-MHz system clock may be used. In COT-mode the PEB 2091 issues all IOM-clocks, an external clock generation circuit is no longer necessary. Information on the U-interface is transmitted synchronous to the system clock.

Cross-reference: **4.5 Clock Generation (Technical Description)**

Technical Data

Application Guide

VAKAT

3 Application Guide

3.1 Interfaces

Section 3.1 describes the interfaces. Three interfaces are implemented in the IEC-Q:

– IOM-2 Interface
– U-Interface
– Power Controller Interface

3.1.1 IOM®-2 Interface

The IOM-2 interface is primarily used to interconnect telecommunication ICs. It provides a symmetrical full-duplex communication link, containing user data, control/programming and status channels. The IEC-Q communicates with other ISDN-devices to realize OSI layer-1 functions (such as a S-transceiver) or upper layer functions (e.g. together with ICC, EPIC, ARCOFI and ITAC).

The structure used follows the 2B + 1 D-channel structure of ISDN. The ISDN-user data rate of 144 kbit/s (B1 + B2 + D) on the U-interface is transmitted transparently in both directions (U <=> IOM) over the interface.

The IOM-2 interface is a generalization and enhancement of the IOM-1 interface.

3.1.1.1 IOM®-2 Frame Structure/Timing Modes

The IOM-2 interface comprises two clock lines for synchronization and two data lines.

The data is clocked by a Data Clock (DCL) which operates at twice the data rate. Frames are delimited by an 8-kHz Frame Synchronization Clock (FSC). Data is carried over Data Upstream (DU) and Data Downstream (DD) signals. The upstream and downstream directions are always defined with respect to the exchange: Downstream refers to information flowing from the exchange to the subscriber and vice versa.

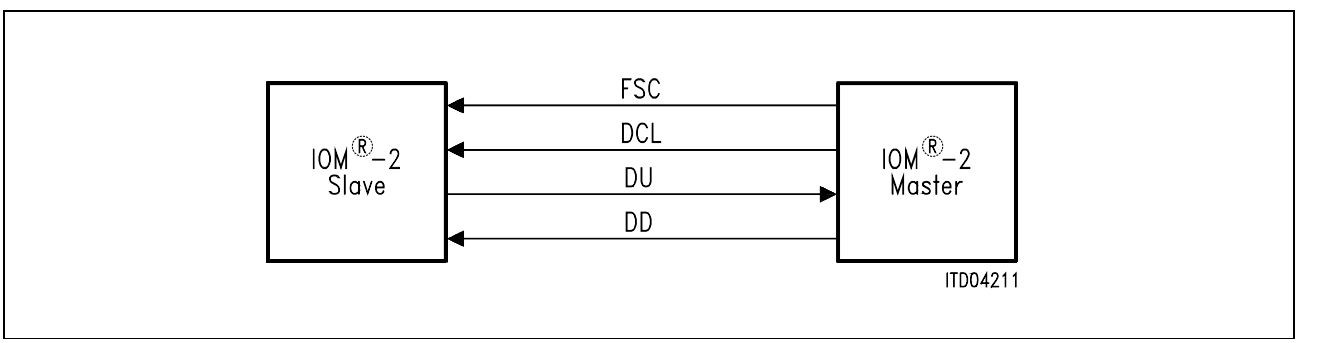


Figure 22
Clock Supply and Data Exchange between Master and Slave

Within one FSC-period, 32 bit up to 256 bit are transmitted, corresponding to DCL-frequencies ranging from 512 kHz up to 4096 kHz.

Two optimized IOM-2 timing modes exist for:

– Line Card Applications
– Terminal Applications

Both the line card and terminal applications utilize the same basic frame and clocking structure, but differ in the number and usage of the individual channels.

channel bits	B1	B2	Monitor	D	Command / Indicate	MR	MX
	8	8	8	2	4	1	1

Figure 23
Basic Channel Structure of IOM®-2

Each frame consists of

– Two 64-kbit/s channels B1 and B2
– The monitor channel for transferring maintenance information between the layer-1 functional blocks (SBCX, IEC-Q, etc.) and the layer-2 controller (ICC, EPIC)
– Two bits for the 16-kbit/s D-channel
– Four command / indication (C/I) bits for controlling of layer-1 functions (activation/deactivation and additional control functions) by the layer-2 controller (ICC, EPIC)
– Two bits MR and MX for handling the monitor channel

3.1.1.1.1 IOM®-2 Interface Line Card Frame Structure

In line card applications (LT-mode) the IEC-Q supports bit rates from 256 kbit/s up to 2048 kbit/s corresponding to DCL-frequencies from 512 kHz up to 4096 kHz.

The typical IOM-2 line card application comprises a DCL-frequency of 4096 kHz with a nominal bit rate of 2048 kbit/s. Therefore eight channels are available, each consisting of the basic frame with a nominal data rate of 256 kbit/s. The downstream data (DD) are transferred on pin DIN, the upstream data (DU) on pin DOUT. The IEC-Q is assigned to an individual channel by pin strapping.

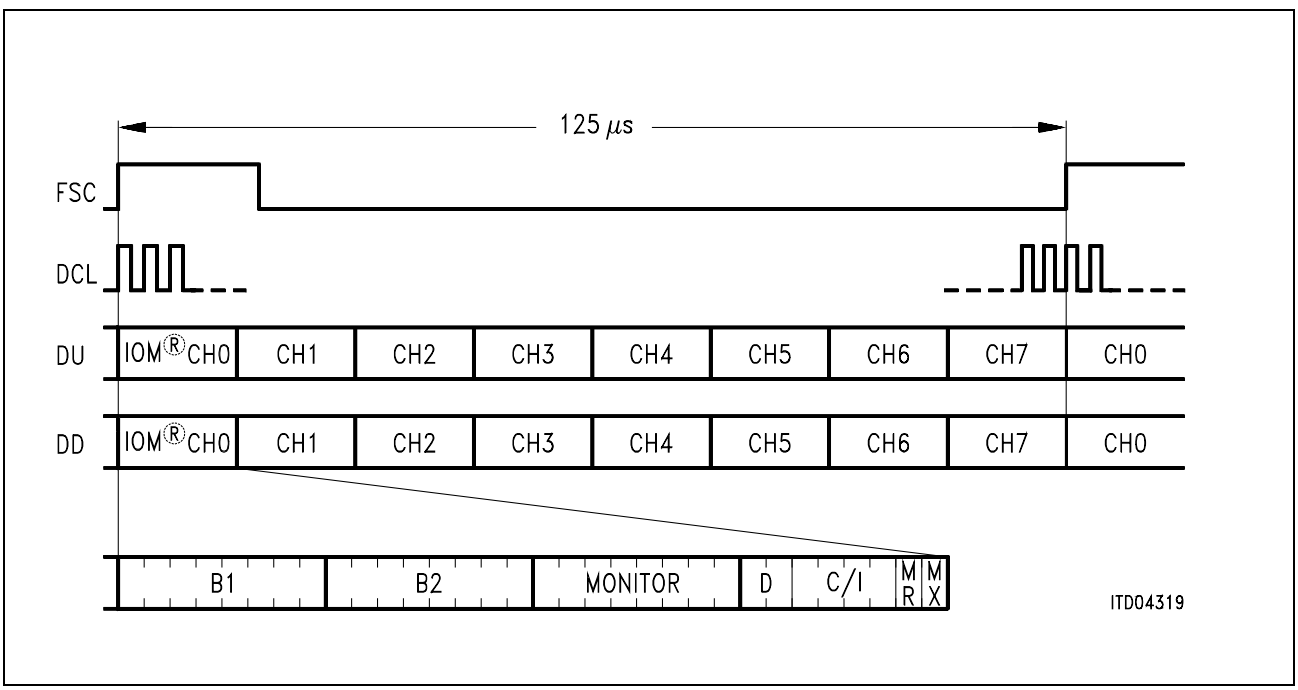


Figure 24
Multiplexed Frame Structure of the IOM®-2 Interface

3.1.1.1.2 IOM®-2 Interface Terminal Frame Structure

In TE mode the PEB 2091 IEC-Q provides a data clock DCL with a frequency of 1.536 MHz. As a consequence the IOM-2 interface provides three channels with a nominal data rate of 256 kbit/s each.

The IEC-Q only uses IOM-2 channel 0. The remaining two IOM-2 channels are for use by other devices (ARCOFI, ITAC) within the TE.

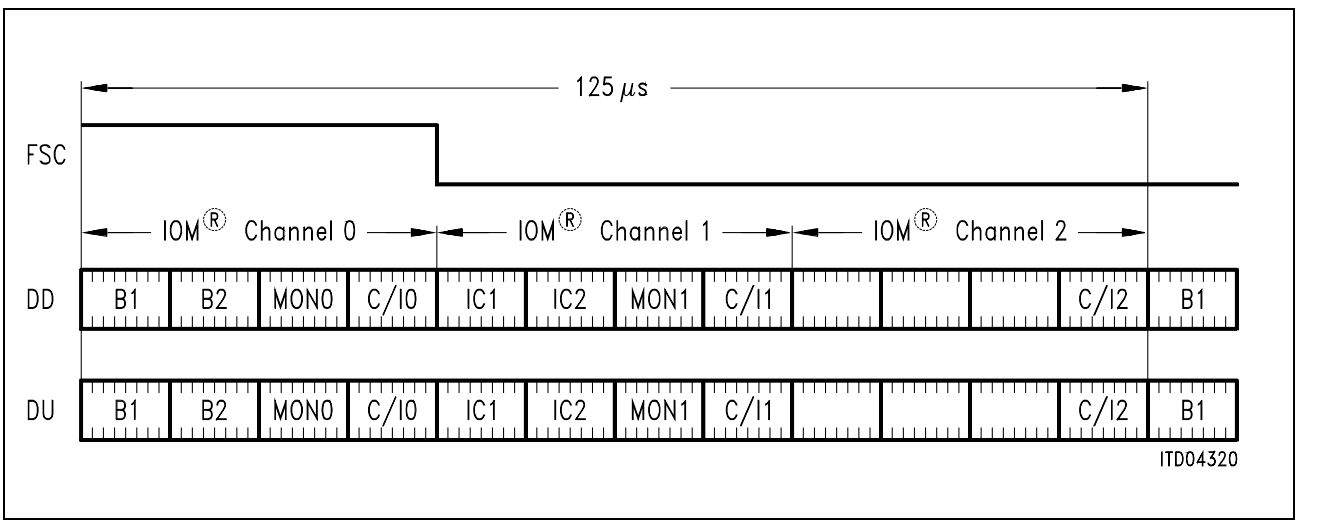


Figure 25
Definition of the IOM®-2 Channels in a Terminal

– C/I0 in IOM-channel 0:

DU/DD	D	D	C/I4	C/I3	C/I2	C/I1	MR	MX

MR: Monitor Read Handshake Bit

MX: Monitor Transmit Handshake Bit

The four command/indication (C/I) bits are used by the layer-2 controller (ICC, EPIC) for controlling the layer-1 functions (activation / deactivation and additional control functions).

– C/I1 in IOM-channel 1:

DU/DD	C/I6	C/I5	C/I4	C/I3	C/I2	C/I1	MR	MX

C/I1 to C/I6 are used to convey actual status information between a layer-2 device (ICC) and various non-layer-1 devices e.g. PSB 2160 ARCOFI.

– C/I2 in IOM-channel 2:

DU	1	1	BAC	TBA2	TBA1	TBA0	1	1
DD	E	E	S/G	A/B	1	1	1	1

BAC: TIC Bus Access Bit
TBA0-2: TIC Bus Address Bit 0 – Bit 2
E: D-Echo Bits
S/G: Stop / Go Bit
A/B: Available / Blocked

The user controls all functions of the IEC-Q with the command/indicate and the monitor channels. The following chapter describes the use of these channels.

Cross-references: **4.1.1 IOM®-2 Dynamic Characteristics (Technical Information)**

3.1.1.2 IOM®-2 Command/Indicate Channel

The Control/Indicate channel (C/I-channel) is used to control the operational status of the IEC-Q and to issue corresponding indications. C/I-channel codes serve as the main link between the IEC-Q and external intelligence. In **chapter 4.3** status diagrams for all selectable modes give information on the commands with which the current operational status may be left, and on indications issued in all states.

Commands have to be applied continuously on DIN until the command is validated by the IEC-Q and the desired action has been initiated. Afterwards the command may be changed.

An indication is issued permanently by the IEC-Q on DOUT until a new indication needs to be forwarded. Because a number of states issue identical indications it is not possible to identify every state individually.

The interpretation of C/I-codes depends on the mode selected. **Table 6** shows the abbreviations used for C/I-commands and indications.

Table 6
C/I-Abbreviations

Code	Description
AI	Activation Indication
AR	Activation Request
AR0	Activation Request with act bit = 0
ARL	Activation Request Local Loop
ARM	Activation Request Maintenance bits
DC	Deactivation Confirmation
DR	Deactivation Request
DEAC	Deactivation Accepted
DI	Deactivation Indication
DT	Data-Through test mode
DU	Deactivation Request Upstream
EI1	Error Indication1 (error on U)

Table 6
C/I-Abbreviations (cont'd)

Code	Description
EI2	Error Indication2 (error on S/T)
EI3	Error Indication3 (timeout T1 [15sec] error on U)
FJ	Frame Jump
HI	High Impedance (set by pin "PS1")
INT	Interrupt (set by pin "INT")
LTD	LT-Disable (control of pin "DISS")
LSL	Loss of Signal Level on U
UAI	U-Activation Indication
UAR	U-Activation Request
RES	Reset
RES1	Reset receiver
RSY	Loss of Synchronization
PU	Power-Up
SSP	Send-Single-Pulses test mode
TIM	Timing request

The following examples illustrate the use of the C/I-channel in combination with the PEB 2070 (ICC) and the PEB 2055 (EPIC). Both examples assume that the device has been initialized correctly prior to starting the C/I-code transfer.

PEB 2070 and C/I-Channel Programming:

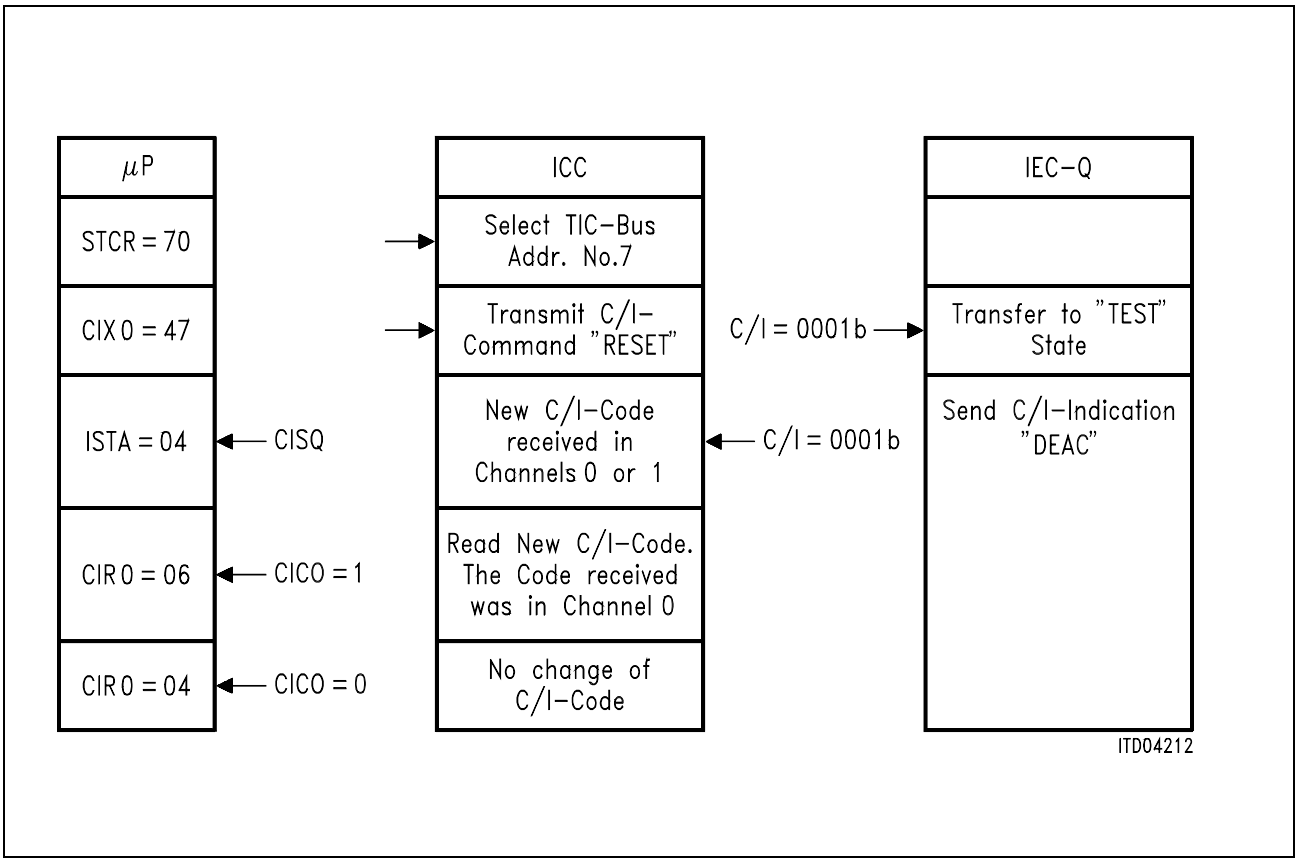


Figure 26
C/I-Channel Use with the ICC (all data values hexadecimal)

The STCR-register is programmed to allocate TIC-bus address 7 to the ICC. The C/I-command is transmitted with the CIX0-register (structure: 0 1 C/I C/I C/I C/I 1 1, bus access bit enabled). After the new C/I-command is loaded it is transmitted immediately.

A change in the C/I-channel is indicated by an ISTA-interrupt (CISQ-bit). The new C/I-message can be read from resister CIR0 (structure: 0 0 C/I C/I C/I C/I CIC0 1). Bit CIC0 indicates that the new C/I-message was received in channel 0 for at least two consecutive frames. It is reset after the read operation.

PEB 2055 and C/I-Channel Programming:

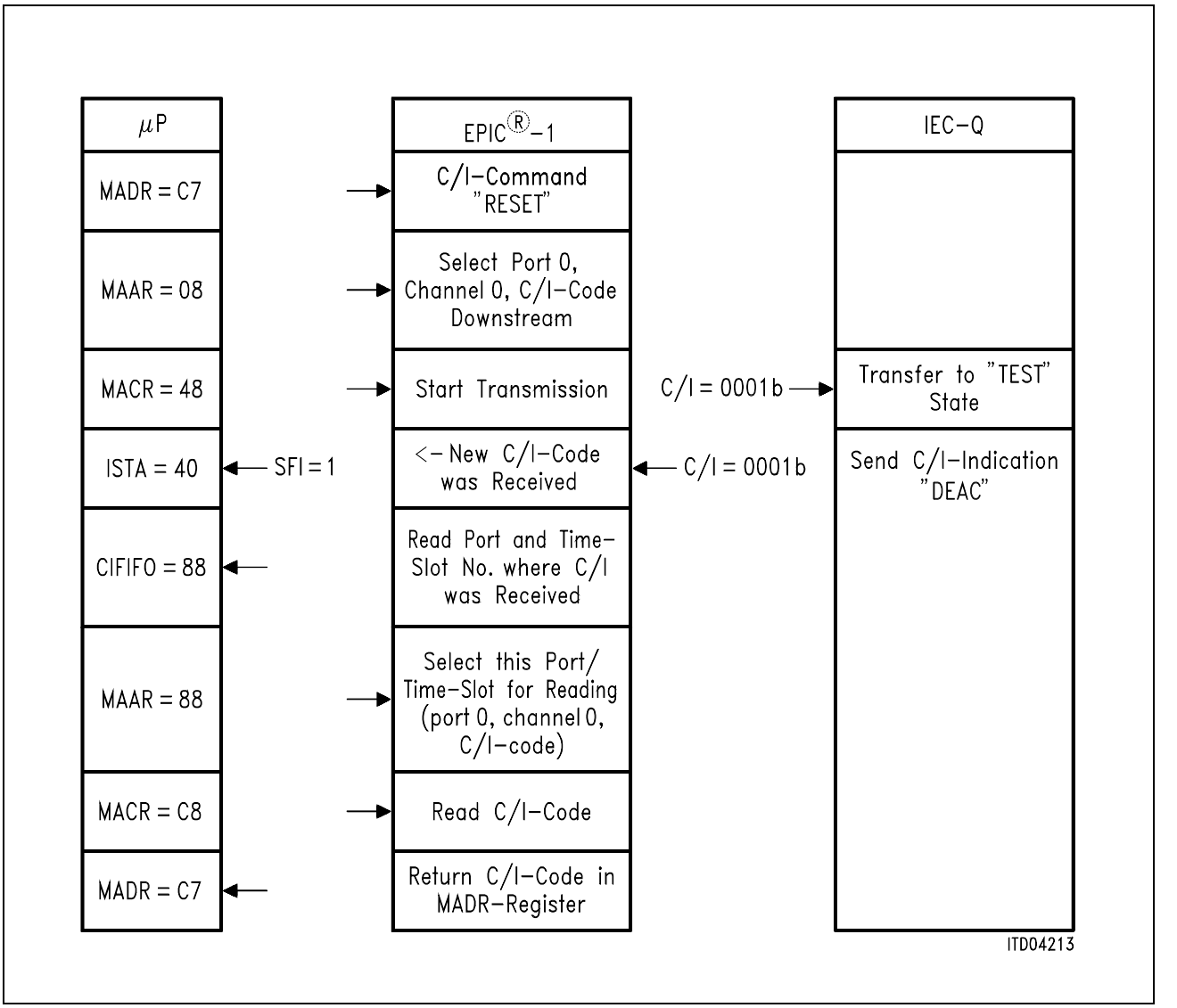


Figure 27
C/I-Channel Use with the EPIC® (all data values hexadecimal)

After the correct initialization of the EPIC, the C/I-code which is to be transmitted to the IEC-Q is written into the MADR-register (structure: 1 1 C/I C/I C/I C/I 1 1). With the MAAR-register the EPIC is informed where to send this C/I-code (transmission direction, port number and time-slot number). For a description of this register please refer to the EPIC-manual, the example above sends the C/I-command to port 0, time-slot 0. MACR = 48_H starts the transmission of the command.

If a change in one of the C/I-channels was observed, an ISTA-interrupt (bit SFI) is generated. Because the user does not know in which channel the change occurred, the location needs to be read from the CIFIFO-register. This address is copied via software into address register MAAR. After having started the read operation with MACR = $C8_H$ the C/I-message can be read from MADR (structure as described earlier).

Cross-references: **3.2 Control Procedures (Applications)**
4.1.1 C/I-Channel (Technical Information)
4.2 Control Procedures (Technical Information)

3.1.1.3 IOM®-2 Interface Monitor Channel

The monitor channel represents a second method of initiating and reading IEC-Q specific information. Features of the monitor channel are supplementary to the command/indicate channel. Unlike the command/indicate channel with an emphasis on status control, the monitor channel provides access to internal bits (maintenance, overhead) and test functions (EOC-commands, local loop-backs, block error counter and self-test).

Monitor functions of the IEC-Q can only be accessed by a control device (ICC, EPIC) in IOM-2 mode. The following chapters describe the principle of monitor handshake in IOM-2, internal safe guards against blocking of the monitor channel, and features (divided into 4 categories).

3.1.1.3.1 Handshake Procedure

IOM-2 provides a sophisticated handshake procedure for the transfer of monitor messages. For handshake control two bits are assigned to each IOM-frame (on DIN and DOUT).

The monitor transmit bit (MX) indicates when a new byte has been issued in the monitor channel (active low). The transmitter postpones transmitting the next information until the correct reception has been confirmed. A correct reception will be confirmed by setting the monitor read bit (MR) to low.

In order to send a monitor message from the control unit to the IEC-Q, the MX-bit on DIN and the MR-bit on DOUT are used. In the opposite direction the IEC-Q handles the MX-bit of the DOUT-pin and watches the MR-bit of the DIN-signal.

Figure 28 illustrates monitor channel handling with the PEB 2070 (ICC), **figure 29** demonstrates it with the PEB 2055 (EPIC-1). A two-byte message is sent from the control unit to the IEC-Q who acknowledges the receipt by returning a two-byte long message in the monitor channel.

PEB 2070 and Monitor Channel Programming:

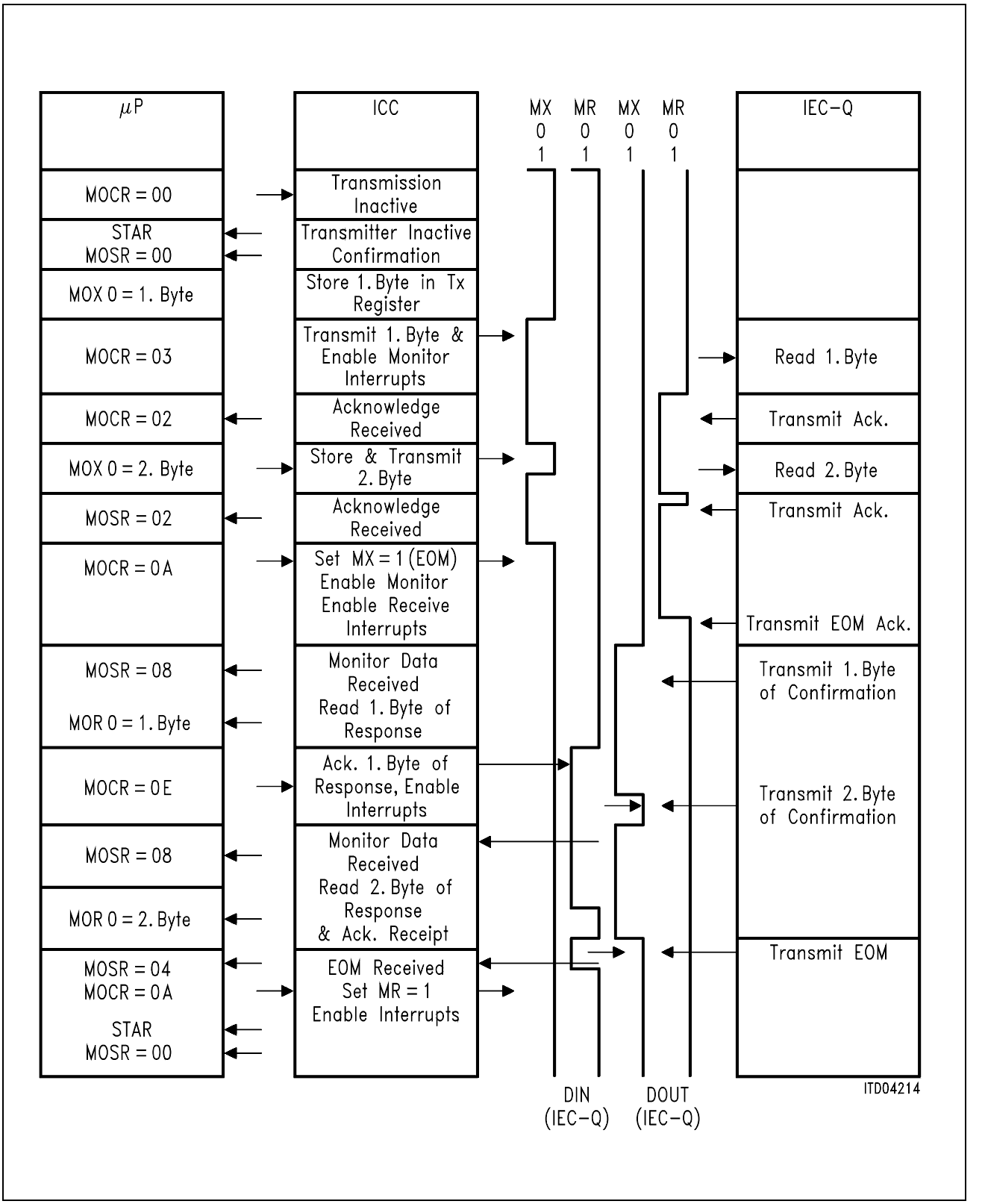


Figure 28
Monitor Channel Handling with ICC (all data values hexadecimal)

The µP starts the transfer procedure after having confirmed the monitor channel being inactive. The first byte of monitor data is loaded into the transmit register. Via the Monitor Control Register MOCR-monitor interrupts are enabled and control of the MX-bit is handed over to the ICC. Then transmission of the first byte begins. The IEC-Q reacts to a low level of the MX-bit on DIN by reading and acknowledging the monitor channel byte automatically. On detection of the confirmation, the ICC issues a monitor interrupt to inform the µP that the next byte may be sent. Loading the second byte into the transmit register results in an immediate transmission (timing is controlled by ICC). The IEC-Q receives the second byte in the same manner as before. When transmission is completed, the ICC sends “End of Message” (MX-bit high).

It is assumed that a monitor command was sent that needs to be confirmed by the IEC-Q (e.g. EOC commands). Therefore the PEB 2091 commences to issue a two-byte confirmation after an End-of-Message indication from the ICC has been detected. The handshake protocol is identical to that of the ICC. The ICC notifies the µP via interrupt when new monitor data has been received. The processor may then read and acknowledge the byte at a convenient instant. When confirmation has been completed, the IEC-Q sends “EOM”. This generates a corresponding interrupt in the ICC. By setting the MR-bit to high, the monitor channel is inactive, the transmission is finished.

PEB 2055 and Monitor Channel Programming

The EPIC-1/2 supports monitor transfers on a higher level than the ICC. Several modes are offered to support different types of monitor transfer. For communication with the IEC-Q, three are of special interest.

– Transmit Only. This mode is required when the EPIC sends monitor messages but no confirmation is returned by the IEC-Q (e.g. MON8 “CCRC”).
– Transmit and Receive. The EPIC transmits first and receives afterwards. Confirmations sent by the IEC-Q can be read (e.g. MON0 “EOC”-messages).
– Searching for Active Monitor Channels. Listens to the IOM-monitor channel and reads information issued by the IEC-Q autonomously (e.g. MON2-messages). Nothing is transmitted by the EPIC.

Unlike the ICC which had to respond to each change of the MR- and MX-bits individually (interrupt driven), the EPIC uses a FIFO for transmission and reception. The user therefore does not have to provide routines for the handshake protocol.

PEB 2055 and Monitor Channel Programming:

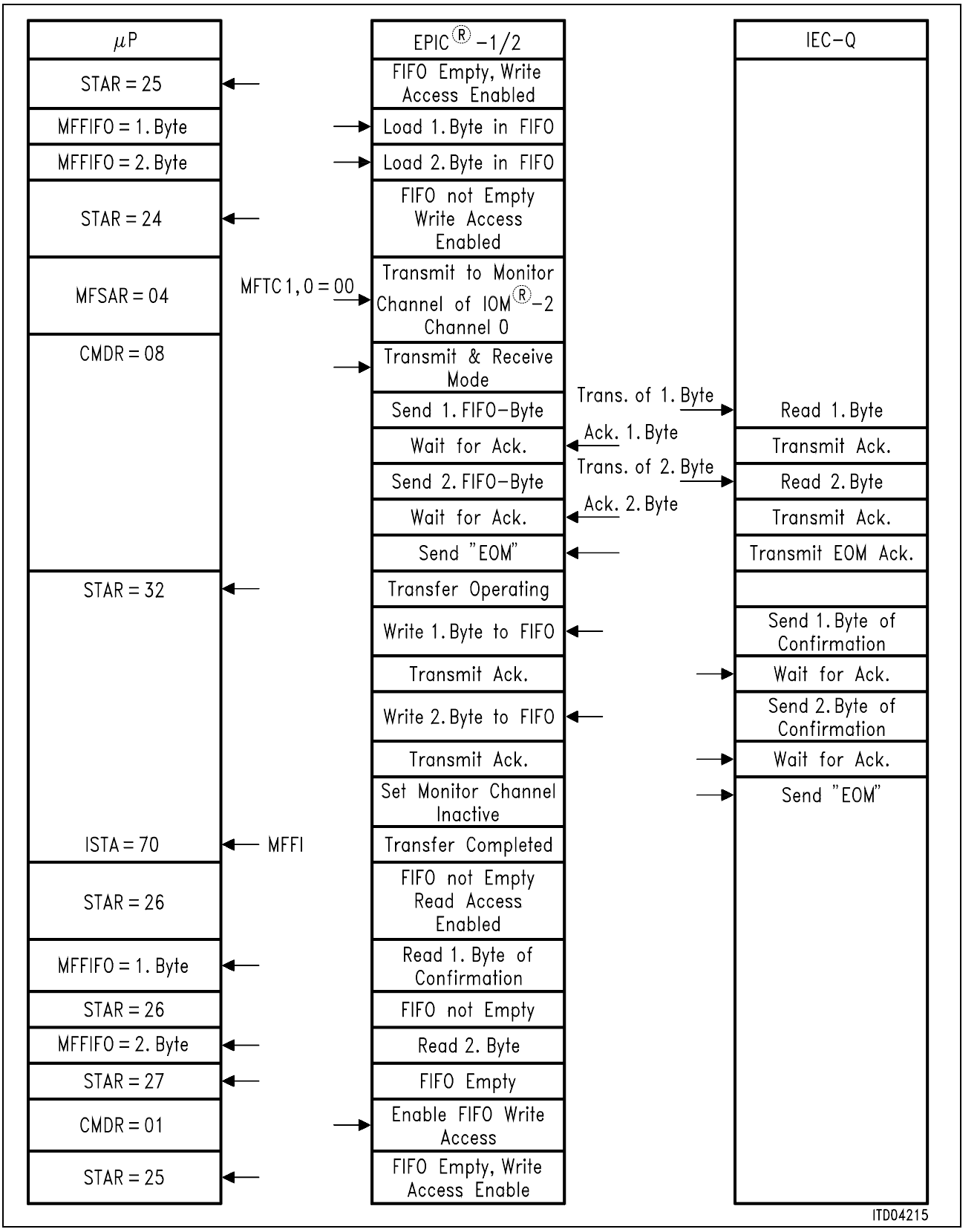


Figure 29
Monitor Channel Handling with EPIC®-1/2 (all data values hexadecimal)

The example of **figure 29** demonstrates the use of EPIC-1 or EPIC-2 in the transmit-and-receive mode. As for the ICC it is assumed that the transferred monitor message will be followed by a two byte confirmation issued by the IEC-Q.

Before programming the FIFO, it is verified that the FIFO is empty and write access is possible. All monitor data is loaded into the FIFO (two bytes), the transmission channel and mode are selected. Writing “CMDR = 08” starts transmission of the FIFO contents and enables monitor data reception. After both bytes have been transmitted, the confirmation from the IEC-Q is read into the FIFO. After completion of the transfer an interrupt is generated. If the operation was successful, “STAR = 26” will indicate that data is loaded and the read access is enabled (in addition it is indicated that the PCM-synchronization status is correct). Following the readout of the confirmation bytes, the FIFO is cleared and the write access is selected again with the CMDR-register (“CMDR = 01”).

The handshake timing for byte transfer is identical to that described for the ICC. Both devices (EPIC and IEC-Q) handle it automatically.

Cross-references: **3.1.1 Monitor Messages (Applications)**
4.1.1 Monitor Channel (Technical Information)

3.1.1.3.2 Monitor Procedure “Timeout” (MTO)

The IEC-Q offers an internal reset (monitor procedure “Timeout”) for the monitor routine. This reset function transfers the monitor channel into the idle state (MR and MX set to high) thereby resolving possible lock-up situations. It therefore is to be used in all systems where no µP is capable of detecting and solving hang-up situations in the monitor procedure (e.g. in a standard NT1).

The reset procedure is started in 6 ms intervals. In order to avoid the loss of transmitted or received data the IEC-Q commences a monitor transfer only when enough time is available before the next reset will be initiated. If this is not the case transmission is postponed until after the reset.

Once a message has been issued on IOM, its transfer needs to be completed before the next reset. If this is not accomplished, the message can be lost without notice. For this reason the control software should be able to transfer monitor messages as quickly as possible.

In applications where a µP controls the system this internal reset option should be disabled by setting the pin “MTO” (no. 34) to high. In this mode no restrictions regarding the time for completing a monitor transfer exist and hence the risk of loosing monitor message is reduced to a minimum.

Cross-references: **4.1.1 Monitor Timeout Procedure/MTO (Technical Information)**
4.1.1 MON Commands and their Priorities (Technical Information)

3.1.1.3.3 MON-0 Command (EOC Programming)

Monitor commands supported by the PEB 2091 divide into four categories. Each category derives its name from the first nibble (4 bits) of the two byte long message. All monitor messages representing similar functions are grouped together. Commands belonging into the first category, MON-0-commands, are described in more detail in this chapter. MON-1-, MON-2- and MON-8-commands are discussed in the following sections.

MON-0-messages are also referred to as EOC-messages (Embedded Operations Channel) because they are used to write and read the registers containing the information of the EOC-channel on the U-interface. Via the U-interface EOC-channel it is possible to exchange service of

signaling information between the exchange side and the terminal side. It is important to note that MON-0-messages provide only access to the device internal EOC-registers. The insertion and extraction of a message on the U-frame is handled automatically by the EOC-processor of the device. Usage of MON-0-monitor messages therefore differs not from other MON-commands.

Nine MON-0-commands are defined and can be interpreted by the PEB 2091. Commands (messages at DIN) are used in LT-mode only. MON-0-messages (at DOUT) are issued in both LT-(for confirmation) and NT-(for test purpose) modes. MON-0-messages are issued with the highest priority, i.e. if a MON-1,2,8-message should be sent simultaneously with a MON-0 message, it is the EOC-message that will be issued first.

The structure of a MON-0-message is shown in the table below.

Table 7
MON-0-Message Structure

1. Byte		2. Byte	
0 0 0 0	A A A | 1	E E E E	E E E E
MON-0	Addr. | d/m	EOC-Code	

The following table describes the commands and messages and gives information about their use. An example illustrating the use of EOC-commands is given in **sections 3.3.1 and 3.3.2**.

Table 8
MON-0-Functions (1. Priority)

NT		LT		Function
D	U	D	U	
LBBD		LBBD		Close complete loop-back (B1, B2, D). The NT does not close the complete loop-back immediately after receipt of this code. Instead it issues the C/I-command AIL (in “Transparent” state and auto-mode) or ARL in the states “Error S/T” and “Synchronized”. This allows the downstream device to close the loop-back if desired (e.g. SBCX). If the downstream device does not close the loop a MON-8 command (LBBD) must be returned and the loop-back is closed within the PEB 2091. In addition the DISS-pin is set to (1) after reception of LBBD. This provides a possibility to perform remote power supply control.
LB1		LB1		Closes B1 loop-back in NT. All B1-channel data will be looped back within the IEC-Q.
LB2		LB2		Closes B2 loop-back in NT. All B2-channel data will be looped back within the IEC-Q.
NCC		NCC		Notify of corrupt CRC. Upon receipt of NCC the NT-block error counters (near-end only) are disabled and error indications are retained. This prevents wrong error counts while corrupted CRCs are sent (MON-8 CCRC).

Table 8
MON-0-Functions (1. Priority) (cont'd)

NT		LT		Function
D	**U**	**D**	**U**	
RCC		RCC		Request corrupt CRC. Upon receipt the NT transmits corrupted (= inverted) CRCs upstream. This allows to test the near end block error counter on the LT-side. The far end block error counter at the NT-side is stopped and NT-error indications (MON-1) are retained.
RTN		RTN		Return to normal. With this command all previously sent EOC-commands will be released. The EOC-processor is reset to its initial state (FF_H). The DISS-pin will be set to (0).
		H	H	Hold. Provokes no change. It may be used as a preliminary message in configurations where the acknowledgment is delayed. E.g. in a repeater configuration the NT-RP could answer with H while the EOC-acknowledgment is passed upstream. Thereby it can be avoided that the LT-control unit misinterprets the delayed ACK as a malfunction. The device issues Hold if no NT or broadcast address is used or if the d/m indicator is set to (0).
			UTC	Unable to comply. Message sent instead of an acknowledgment if an undefined EOC-command was received by the NT.
			ACK	Acknowledge. If a defined and correctly addressed EOC-command was received by the NT, the NT replies by echoing back the received command.

Auto-Mode/Transparent Mode

The use of the EOC-channel depends upon the operational mode of the IEC-Q and the EOC-processing mode. The user may choose between auto- and transparent mode in LT- and NT-modes.

Special processing is required for repeater applications. Therefore it is recommended to use the transparent mode in repeater applications.

In auto-mode all received commands will be acknowledged (NT only). If addressed correctly (000_B = NT or 111_B = broadcast) the NT will initiate the requested action automatically. Only EOC-messages that differ from the previously received message will be passed on to the IOM-2 interface (see corresponding section in **chapter 4** for details).

In transparent mode no acknowledge and execution of requested actions is performed. A monitor message containing the most recently received command will be issued twice per superframe (every 6 ms) independently of whether the command has changed or not.

Because in both transparent and auto-mode all received EOC-commands are passed on to the IOM-2 interface via MON-0 messages, the EOC-channel may be used to transmit signaling information with user defined commands. Refer to section 4.1.2 and ANSI for restrictions on user defined codes.

Repeater Transparent Mode

LT-RP and NT-RP are operated in transparent mode. In order to address each repeater individually, the EOC-addresses (001_B) to (110_B) are used. This allows a maximum of 6 repeater stations to be addressed.

The repeater address is 001_B. If a repeater control unit detects an EOC-message with this address, the EOC-command will be executed according to the national repeater specification. In case an EOC-message with the NT (000_B) or broadcast (111_B) address is received by the repeater, the message needs to be passed on without modifications. If any other address is received (i.e. (010_B) to (110_B)) the repeater control unit (µ.P. system or ASIC) decrements the address before passing the EOC-message downstream. **Figure 30** illustrates this procedure with a repeater and a NT EOC-address.

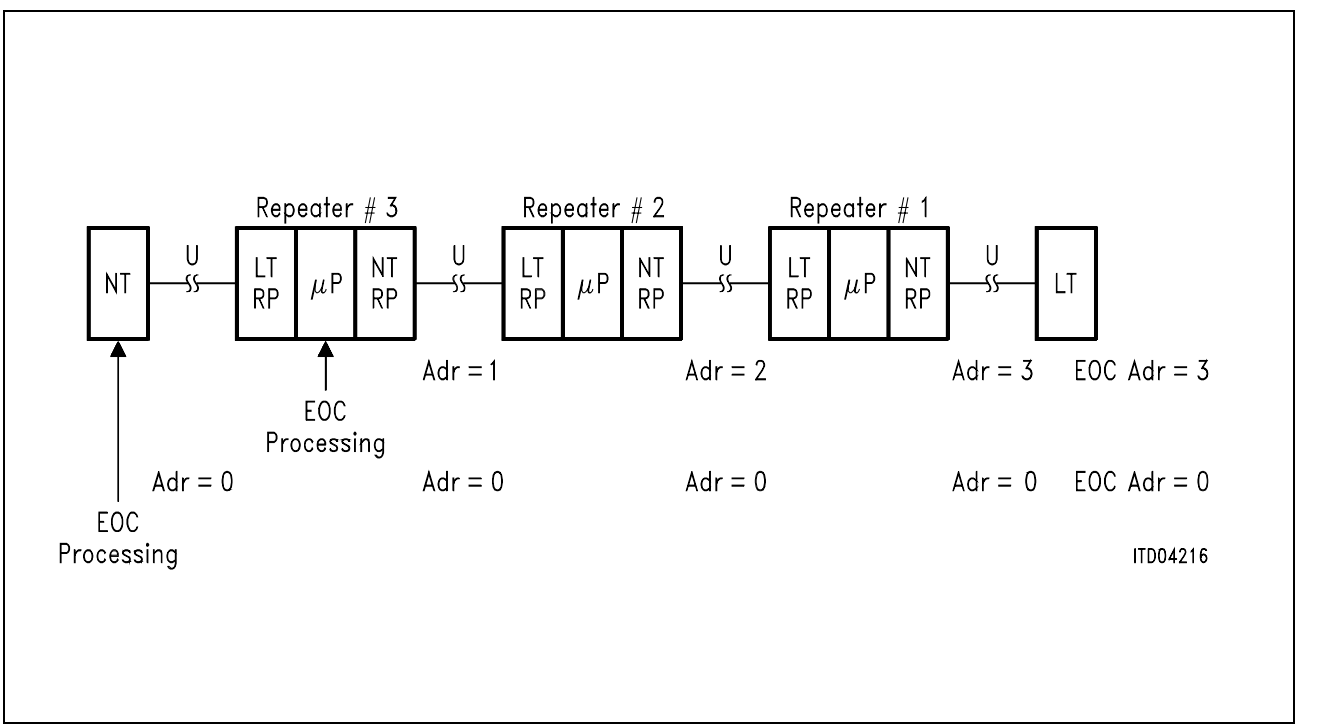


Figure 30
EOC-Handling in Repeater Applications

Cross-references:

3.1.1	**Commands in Different MON-Categories (Application)**
3.3.1	**Example of EOC Use in Error Counter Test (Application)**
4.1.1	**MON-0-Codes (Technical Description)**
4.1.2	**EOC-Channel on U-Interface (Technical Description)**

3.1.1.3.4 MON-1 Commands (Maintenance bits-S/Q-channel)

This category comprises commands and messages relating to bits in the maintenance channel on the U-interface as well as S/Q-channel indications.

The S/Q-channel of the S-interface corresponds to the EOC-channel of the U-interface and provides a method to exchange service information between terminal and network termination. The SBCX transfers all indications transparently between IOM-2 (NT) and S-interface. This allows the terminal to be informed about transmission errors that occurred on the U-interface (NEBE, FEBE, FNBE) or request the IEC-Q to perform a self-test (ST).

The maintenance bit channel is used to inform the exchange side that local tests are preventing a standard transmission.

MON-1 messages are two bytes long. The first nibble of the second byte contains S/Q-indications, the second nibble contains maintenance bit related commands. The following table gives an overview of indications available in the MON-1 category.

Table 9
Available Indications in MON-1-Commands

1. Byte		2. Byte	
0 0 0 1	0 0 0 0	S S S S	M M M M
MON-1		S/Q Code	M Bits

Table 10
Mon-1-Functions in S/Q-Channel (2. Priority)

NT		LT-RP		Function
D	U	D	U	S/Q-Channel
	ST			Self-test request. This command is issued by the terminal to inquire whether layer 1 is present. No test is performed within the IEC-Q. Upon reception the PEB 2091 replies with MON-1 “STP”.
STP				Self-test pass. Indicates to the terminal that the IEC-Q has received the command “ST” correctly.
FEBE			FEBE	Far-end block error. Via the FEBE bit set to (0) on the U-interface it is indicated to the NT that transmission errors occurred in the direction NT –> LT or NT –> LT-RP.
NEBE			NEBE	Near-end block error. Transmission errors occurred in the direction LT –> NT or LT –> NT-RP.
FNBE			FNBE	Far- and near-end block error. Transmission errors were observed in both LT –> NT and NT –> LT-direction.
	NORM			Normal. Return to normal (idle) state. This command initiates no IEC-Q action.

Table 11
MON-1-Functions Maintenance Bits (2. Priority)

NT		LT-RP		Function
D	U	D	U	Maintenance Bits
	NTM			NT-test mode. After reception of this command the NTM-bit of the U-interface is set active (= 0) in order to inform the exchange that the NT is involved in testing and not available for transparent transmission. This message needs to be sent out by the downstream device if the terminal requests tests which prevent transparent transmission (e.g. loops B1, B2, D).
	NORM			Normal Sets back the NTM-bit to 1. No other action taken.

Cross-references:
3.1.1 Commands in Different MON-Categories (Application)
4.1.1 MON-1-Codes (Technical Description)
4.1.2 Maintenance Bits at U-Interface (Technical Description)

3.1.1.3.5 MON-2 Commands (Overhead Bits)

MON-2-indications are used to transfer all overhead bits except those representing EOC- and CRC-bits. Starting with the ACT-bit, the order is identical to the position of the bits at the U-interface.

The first MON-2-message is issued immediately after reaching the “Synchronized” state in NT-modes or the “Line Active” state in LT-modes. Thereby the control system is informed about the initial U-interface status after a successful activation.

Later MON-2-messages will only be sent if a change of system status has occurred. No MON-2-messages are issued while CRC-violations are detected (refer to **section 4.2.3** for verification algorithm). This prevents the system of being overloaded by faulty monitor indications.

Table 12
MON-2 Command Structure

1. Byte		2. Byte
0 0 1 0	M41 M51 M61 M42	M52 M62 M43 M44 M45 M46 M47 M48
MON-2	Overhead Bits	Overhead Bits

The meaning of bits M41-M48 depends upon the transmission direction (LT –> NT or NT –> LT) and the mode. **Section 4.1.1** includes a table listing the bit positions within the MON-2 message in different modes and directions. The description in this chapter concentrates on the use of the overhead bits. They are grouped by the three control mechanisms responsible for setting and resetting the bits.

Control via IEC-Q:

– ACT (Activation bit)
  The ACT-bit is part of the start-up sequence and is used to indicate layer 2 to be ready for communication. In this case it is set to (1).
– DEA (Deactivation bit)
  The DEA-bit is used by the network side during deactivation. By setting DEA to (0), the network informs the NT of its intention to turn-off.
– CSO (Cold Start Only)
  The CSO-bit signals the network side whether the NT is only capable of being started via cold start. If the NT may be activated with a cold start procedure only, the CSO-bit is set to (1).
– UOA (Partial Activation)
  The UOA-bit is used by the network side to inform the NT that only the U-interface shall be activated (S-interface remains deactivated according to CNET-specification). If the UOA-bit is set to (0), only the U-interface will be activated.
– SAI (S Activity Indicator)
  The SAI-bit informs the LT-side about the state of the S-interface. With the S-interface deactivated (i.e. C/I-commands TIM or DI received), the SAI-bit is set to (0). Additionally the SAI-bit is used (with SAI = (1)) in a terminal initiated activation (when before only U was activated) to request complete NT-activation.
– FEBE (Far-End Block Error)
  The FEBE-bit is used to inform the opposite U-interface station that the transmitted data could not be received free of errors. The device sets the FEBE-bit to (0) if errors were observed. Each time a FEBE = (0) is detected, the count of the internal far-end block error counter will be incremented. Additionally it is possible to control the FEBE-bit with the MON-8-message “SFB”.

Control via Pins:

– PS1 (Power Status Primary Source)
  The PS1-bit is used to indicate the status of the primary NT-power supply. It is set to (1) if the level at pin PS1 is high. PS1 = (1) indicates that the primary power supply is normal.
– PS2 (Power Status Secondary Source)
  The PS2 bit is used to indicate the status of the secondary NT-power supply. It is set to (1) if the level at pin PS2 is high. PS2 = (1) indicates that the secondary power supply is normal.

Control via MON-Commands:

– FEBE (Far-End Block Error)
  IEC-Q controlled commands. Additionally it is possible to set the FEBE bit to (0) for one single U-superframe with the MON-8 message “SFB”.
– NTM (NT-Test Mode)
  This bit informs the network side that the NT is involved in terminal initiated tests and therefore is not available for transparent transmission. The NTM-bit set to (0) indicates that the NT is in a test-mode. The NTM-bit is set to (0) with the MON-1 command “NTM” and is reset to (1) by “NORM”.
– REPEATER Modes
  If the IEC-Q operates in LT-RP or NT-RP-RE-mode, all bits need to be controlled via MON-2-messages. This permits to implement national repeater specifications for overhead bit treatment. **Figure 31** shows an example for typical maintenance bit handling in repeater applications via MON-2.

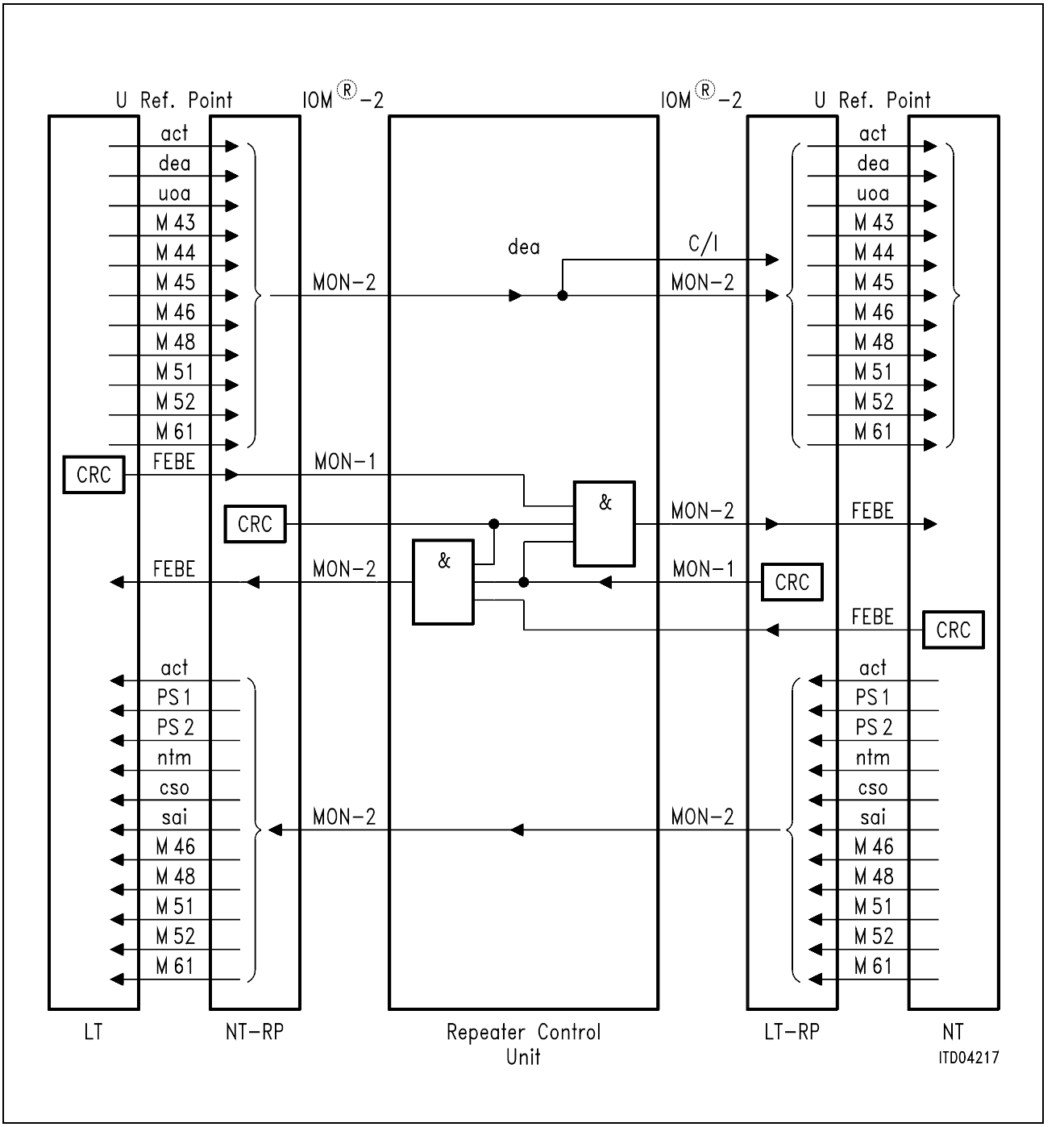


Figure 31
Maintenance Bit Handling in Repeaters (Example)

Cross-references:

3.1.1	**Commands in Different MON-Categories (Application)**
4.1.1	**MON-2-Codes (Technical Description)**
4.1.2	**Overhead Bits on U-Interface (Technical Description)**
4.2	**Control Procedures Involving UOA/SAI (Technical Description)**

3.1.1.3.6 MON-8 Commands (Local Functions)

Local functions are controlled via MON-8-commands. MON-8-commands have the lowest priority. The following tables give an overview of structure and features of commands belonging to this category.

Table 13
MON-8 Command Structure

1. Byte		2. Byte
1 0 0 0	r | 0 0 0	D7 D6 D5 D4 D3 D2 D1 D0
MON-8	Register Addr.	Local Command (Msg./Data)

Table 14
MON-8-Functions (4. Priority)

NT		LT		Function
D	U	D	U	Local Commands
	PACE	PACE		Partial Activation Control External. With the PACE-command issued at the NT-side, the IEC-Q will ignore the actual status of the received UOA-bit and behave as if the UOA-bit is set to (1). If issued at LT-side, the actual status of the SAI-bit is ignored and the device works as if SAI = (1) is received. After issuing PACE the IEC-Q Vers. 4.3 is compatible to IEC-Q Vers. 3.3 and the UOA/ SAI-bits can be controlled by MON-2-commands.
	PACA	PACA		Partial Activation Control Automatic. PACA enables the device to interpret and control the UOA- and SAI-bits automatically (NT- and LT-side respectively). Partial activation and deactivation in NT-modes is therefore possible. The IEC-Q is automatically reset into this mode in the states “Test”, “Receive Reset” and “Tear Down”.
	CCRC	CCRC		Corrupt CRC. In LT-mode this command causes the device to send inverted (i.e. corrupted) CRCs. Corrupted CRCs are used to test block error counters (see **section 3.3.2**). In NT-mode this command is only recognized if the device is set to transparent mode. The system controller (e.g. ICC) should issue the command in case the MON-0-command RCC was received before. CCRC then causes corrupt CRCs to be transmitted upstream.

Table 14
MON-8-Functions (4. Priority) (cont'd)

NT		LT		Function
D	**U**	**D**	**U**	**Local Commands**
	LB1			Loop-back B1. The command is only recognized in NT-transparent mode. The system controller (e.g. ICC) should issue the command in case the MON-0-command LB1 was received before. LB1 loops back the B1 channel. The loop is closed near the IOM-interface.
	LB2			Loop-back B2. The command is only recognized in NT-transparent mode. The system controller (e.g. ICC) should issue the command in case the MON-0-command LB2 was received before. LB2 loops back the B2 channel. The loop is closed near the IOM-interface.
	LBBD			Loop-back B1 + B2 + D. The command is used in the transparent and auto-mode. LBBD loops back both B-channels and the D-channel. The loops are closed near the IOM-interface. In transparent mode the loop is closed unconditionally. In auto-mode the loop is closed only if LBBD was received in the EOC-channel before (see also **section 3.1.1.3.3** "LBBD"). See **section 3.3.1** on test functions for details.
	NORM	NORM		Return to Normal. The NORM-command resets the device into its default mode, i.e. loops are resolved and corrupted CRCs are stopped. In NT-mode it is only used in transparent mode.
	RBEN	RBEN		Read Near-End Block Error Counter. The value of the near-end block error counter is returned and the counter is reset to zero. The maximum value is FF_H.
	RBEF	RBEF		Read Far-End Block Error Counter. The value of the far-end block error counter is returned and the counter is reset to zero. The maximum value is FF_H.
ABEC			ABEC	Answer Block Error Counter. The value of the requested block error counter is returned (8 bit).
		RPFC		Read Power Feed Current. The value of the feed current is returned. This value is transferred serially (8 bit) via the power controller to pin PS2. This feature is only available in conjunction with power controllers that support this function (e.g. SEL). For details please refer to **section 3.1.3, 4.1.3**.

Table 14
MON-8-Functions (4. Priority) (cont'd)

NT		LT		Function
D	**U**	**D**	**U**	**Local Commands**
	WCI	WCI		Write Controller Interface. Three bit wide data is transferred to one of four addresses of the power controller. The command is designed to work in combination with the power controller PEB 2025 (IEPC) but may also be used to address a general purpose interface. Please see **section 4.1.3 and 5.1.3** for details.
	RCI	RCI		Read Controller Interface. A two bit wide address is used to select the power controller register to be read. Like the write operation the RCI-command may also be used in conjunction with a general purpose interface.
ACI			ACI	Answer Controller Interface. Contains the three bits of data returned after a read request (RCI).
	RID	RID		Read Identification. Request for device identification.
AID			AID	Answer identification. The IEC-Q Vers. 4.3 will reply with the ID 8001_H.
	SFB	SFB		Set FEBE Bit to 0

Cross-references:

3.1.1 **Commands in Different MON-Categories (Application)**
3.1.3 **Power Controller Interface (Application)**
3.3.1 **Test Loops (Application)**
3.3.2 **Block Error Counters (Application)**
4.1.1 **MON-8-Codes (Technical Description)**
4.1.3 **Power Controller Interface (Technical Description)**
4.2.5 **Control Procedures Involving UOA/SAI (Technical Description)**

3.1.2 U-Interface

The U-interface establishes the direct link between the exchange and the terminal side. It consists of two copper wires. The PEB 2091 provides two differential outputs and two differential inputs which are coupled via an external “hybrid” network and a transformer onto the copper pair.

Direct access to the U-interface is not possible. 2B + D user data can be inserted and extracted via the IOM-2 interface. Control of maintenance bits is partly possible with IOM-2 monitor messages and power controller interface pins. The remaining maintenance bits are fully controlled by the IEC-Q itself and allow no external influence (e.g. CRC-checksum).

Because **chapter 3** is application oriented and the user has no direct access possibility to the U-interface, the following sections give only an overview. For details please refer to the technical description in **chapter 4**.

3.1.2.1 Frame Structure/Timing

Transmission on over the U-interface is performed at a rate of 80 kBaud. The code used is reducing two binary informations to one quaternary symbol (2B1Q).

Data is grouped together into U-superframes of 12 ms each. The beginning of a new superframe is marked with an inverted synchronization word (ISW). Each superframe consists of eight basic frames which begin with a standard synchronization word (SW) and contain 222 bits of information. The structure of one U-superframe is illustrated in **figure 32**.

ISW	**1. Basic Frame**	**SW**	**2. Basic Frame**	**. . .**	**SW**	**8. Basic Frame**
<---			12 ms			--->

Figure 32a
U-Superframe Structure

(I) SW **(Inverted) Synch Word** **18 Bit (9 Quat)**	**12 × 2B + D** **User Data** **216 Bits (108 Quat)**	**M1 – M6** **Maintenance Data** **6 Bits (3 Quat)**
<---	1,5 ms	--->

Figure 32b
U-Basic Frame Structure

Out of the 222 information bits 216 contain 2B + D data from 12 IOM-frames, the remaining 6 bits are used to transmit maintenance bits. Thus 48 maintenance bits are available per U-superframe. They are used to transmit two EOC-messages (24 bit), 12 overhead bits and one checksum (12 bit).

The function of EOC and overhead bits has already been discussed in connection with monitor messages. The next two sections describe how these bits are transmitted on the U-interface. Section “Cyclic Redundancy Check” describes the third group of maintenance bits, the cyclic redundancy checksum.

3.1.2.2 Embedded Operations Channel (EOC)

The embedded operations channel is used to transfer data from the exchange to the terminal side and vice versa without occupying B- or D-channels. It is used to transmit diagnostic functions and signaling information.

EOC-data is inserted into the U-frame at the positions M1, M2 and M3 thereby permitting the transmission of two complete EOC-messages within one U-superframe.

Access to the embedded operations channel is only possible via the EOC-processor and the monitor channel in IOM-2. With a MON-0-command a complete EOC-message (address field, data/ message indicator and information field) can be passed to the PEB 2091. All application relevant issues are discussed in the MON-0-section.

Cross-references:
3.1.1 MON-0-Commands (Application)
4.1.1 MON-0-Commands (Technical Description)
4.1.2 Embedded Operations Channel (Technical Description)

3.1.2.3 Overhead Bits

The positions M4 and M6 in the U-superframe is reserved for overhead bits. These bits are used to communicate status and maintenance functions between the transceivers. The meaning of a bit position is dependent upon the direction of transmission (upstream/downstream) and the operation mode (repeater or NT/LT).

For details regarding single bits please refer to the cross-references listed below.

Cross-references:
3.1.1 MON-1/2-Commands (Application)
3.1.3 Power Status Bits (Application)
4.1.1 MON-1/2-Commands (Technical Description)
4.1.2 U-Frame Structure (Technical Description)
4.1.3 Power Status Bits (Technical Description)

3.1.2.4 Cyclic Redundancy Check

The cyclic redundancy check provides a possibility to verify the correct transmission of data. The checksum of the currently transmitted U-superframe is calculated according to the CRC algorithm. This 12-bit value is transmitted at position M5 and M6 in the following superframe. At the receiving side this value is compared with the value calculated from the received superframe. In case both values are not identical, the FEBE bit is set to (0) in order to indicate that transmission errors had occurred. **Figure 33** shows this relationship.

LT –> NT Superframe				
… Z	A	B	C	D
…	1 2 3 4 5 6 7 8	1 2 3 4 5 6 7 8	1 2 3 4 5 6 7 8	1 2 3 4 5 6 7 8
…	CRC(Z), FEBE(– 1)	CRC(A), FEBE(0)	CRC(B), FEBE(1)	CRC(C), FEBE(2)

NT –> LT Superframe				
… 0	1	2	3	4
…	1 2 3 4 5 6 7 8	1 2 3 4 5 6 7 8	1 2 3 4 5 6 7 8	1 2 3 4 5 6 7 8
…	CRC(0), FEBE(Y)	CRC(1), FEBE(Z)	CRC(2), FEBE(A)	CRC(3), FEBE(B)

----------> Time

Figure 33
CRC in Superframes

It is not possible to access the CRC-checksum. Hence the user cannot read or write the checksum values.

Cross-references: **4.1.2 Cyclic Redundancy Check (Technical Description)**

3.1.2.5 Scrambler/Descrambler

The bit stream needs to be scrambled before transmission in order to avoid long sequences of continuous (1) or (0). The scrambling algorithm is defined by ANSI. In the receiver the scrambled signal is reconstructed with a descrambling algorithm. The scrambling/descrambling process is controlled fully by the IEC-Q. No influence can be taken by the user.

Cross-references: **4.1.2 Scrambler/Descrambler (Technical Description)**

3.1.3 Power Controller Interface

A special controller interface is implemented in the PEB 2091 to provide comfortable access to peripheral circuits which do not have an own microprocessor interface. Because this interface was specifically designed to support the ISDN Exchange Power Controller IEPC (PEB 2025) with a minimum of external effort, this interface is also referred to as “Power Controller Interface”. Despite this dedication to the IEPC, the controller interface is just as suited for many general-purpose applications.

3.1.3.1 Power Controller Structure

The power controller interface consists of four sections. It provides:

– 3 bit data bus
– 2 bit address bus
– 3 control signals
– power controller maintenance bits

Figures 34 and 35 illustrate how the user generally accessed both interface and maintenance bits in NT mode and LT mode applications.

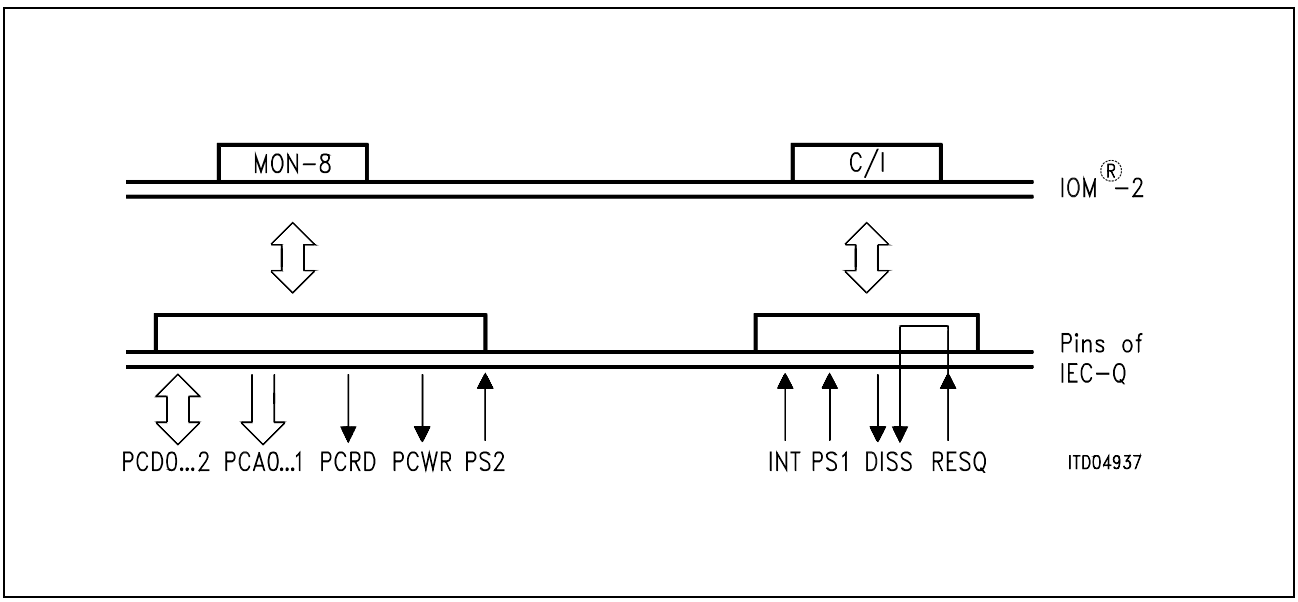


Figure 34
Power Controller Access in LT Mode

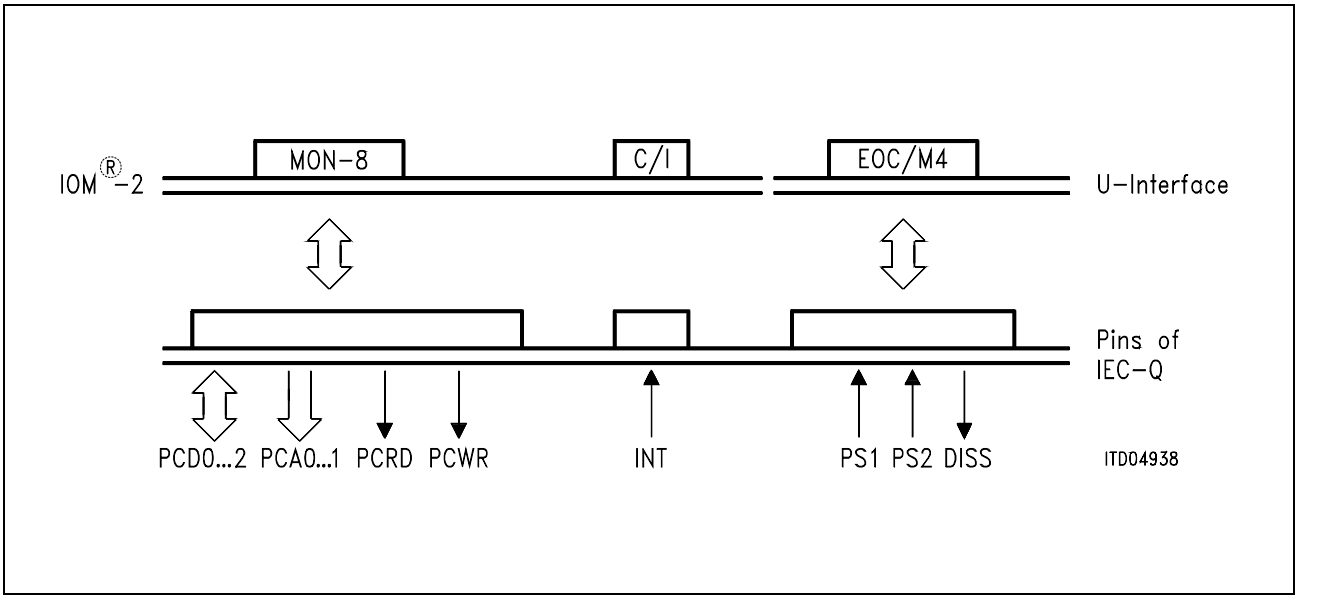


Figure 35
Power Controller Access in NT Mode

The following two sections describe the power controller interface and maintenance bits as well as their use in detail.

3.1.3.2 Interface Bits (PCD, PCA, PCRD, PCWR, INT)

The interface structure is adapted to the register structure of the IEPC. It consists of three data bits PCD0 ... 2, two address bits PCA0,1, read and write signals PCRD and PCWR respectively as well as an interrupt facility INT.

The address bits are latched, they may therefore in general interface applications be used as output lines. For general interface inputs each of the three data bits is suitable. Read and write operations are performed via MON-8 commands. Three inputs and two outputs are thus available to connect external circuitry.

The interrupt pin is edge sensitive. Each change of level at the pin INT will initiate a C/I-code “INT” (0110_B) lasting for four IOM-frames. Interpretation of the interrupt cause and resultant actions need to be performed by the control unit.

Table 15 lists all MON-8- and C/I-commands relevant to the power controller interface. With regard to the interface section of the power controller interface no differences between operation in LT- or NT-modes exist. In **sections 3.1.1** (MON-8, Local Functions, Application) and **4.1.1** (MON-8, Local Functions, Technical Description) the user finds more information about these commands. Refer to the example below for a sample application.

Table 15
MON-8- and C/I-Commands

LT- and NT-Modes		
Channel	**Code**	**Function**
MON-8	WCI	Write to interface. Address and data is contained in the MON-command. The address is latched, data is not latched.
MON-8	RCI	Read from interface at specified address. Address is latched and the current value of the data port is read. The result is returned to the user with MON-8 “ACI”.
MON-8	ACI	Answer from interface. After a RCI-request the value of three data bits at the specified address is returned.
C/I	INT	Interrupt. After a change of level has been observed, the C/I-code “INT” is issued for 4 IOM-frames. Note the special timing of the interrupt signals described in **section 4.1.3**.

Applications:

For transfer of the monitor commands with ICC or EPIC proceed as described in **section 3.3.1**. For an interpretation of the codes used in these examples please refer to **section 4.1.1**. The following examples represent the results when no power controller is connected. The address lines are not connected, the data lines are clamped to the values given in the application.

1) Write to controller interface:

IOM-2	IEC-Q	
a) MON-8 WCI (80 7C) ——>	Pin PCA0 = (0)	; Write data 7_H to address
	Pin PCA1 = (0)	; 0_H
	Pin PCD0 … 2 = (1)	; Data not latched
b) MON-8 WCI (80 62) ——>	Pin PCA0 = (0)	; Write data 0_H to address
	Pin PCA1 = (1); 1_H	
	Pin PCD0 … 2 = (0)	; Data not latched

2) Read from controller interface:

IOM-2	IEC-Q	
a)	Pin PCD0 = (0)	; Values stable on data port
	Pin PCD1 = (0)	
	Pin PCD2 = (0)	
MON-8 RCI (80 40) ——>	Pin PCA0 = (0)	; Read from address 0_H
	Pin PCA1 = (0)	; Address is latched
MON-8 ACI (80 00) <——		; PCD0 … 2 = (0)
b)	Pin PCD0 = (0)	; Values stable on data port
	Pin PCD1 = (0)	
	Pin PCD2 = (0)	
MON-8 RCI (80 42) ——>	Pin PCA0 = (1)	; Read from address 1_H
	Pin PCA1 = (0)	; Address is latched
MON-8 ACI (80 00) <——		; PCD0 … 2 = (0)
c)	Pin PCD0 = (1)	; Values stable on data port
	Pin PCD1 = (0)	
	Pin PCD2 = (1)	
MON-8 RCI (80 41) ——>	Pin PCA0 = (0)	; Read from address 2_H
	Pin PCA1 = (1)	; Address is latched
MON-8 ACI (80 A0) <——		; PCD0 … 2 = (101)

3) Interrupt

IOM-2	IEC-Q	
C/I AI (1100) <——		; Initial C/I-code
	Pin INT (0) <-> (1)	; Level change on INT-pin
C/I INT (0110) <——		; C/I-code INT issued for
C/I AI (1100) <——		; 4 IOM-frames

Cross-references:

3.3.1	**Handshake Procedure with ICC and EPIC (Application)**
3.3.1	**MON-8 Commands (Application)**
4.1.1	**MON-8 Commands (Technical Description)**
4.1.3	**Interface (Technical Description)**

3.1.3.3 Power Controller Maintenance Bits (PS1, PS2, DISS)

In addition to the general interface, three signals are available for comfortably surveying and controlling the power status. Their meanings depend on the mode selected.

In NT-mode, power status bits 1 and 2 (PS1/2) are used to monitor both primary and secondary NT-power supply. This information is transferred via the overhead bit channel to the exchange side. A pin level of (1) results in the corresponding overhead bit to be set to (1) and indicates that the power supply is working correctly.

The output pin disable (DISS) is set to (1) if the EOC-command “close complete loop” (LBBD) has been detected by the NT. This function is only available in auto-mode. It may be used to test a secondary power source (e.g. battery check). The DISS-pin is set back to (0) with the EOC-command “RTN” or a reset.

In LT-mode the first power status bit (PS1) is used to monitor the remote power feed circuit of the subscriber line. A high level (1) indicates that the remote power has been turned off. In order to notify the processing unit of this condition, the C/I-code “HI” (0011_B) will be issued and the device is reset into the “TEST” state. An existing communication link will be broken down.

The pin PS2 provides a serial interface in order to read in the value of the current fed to the subscriber line by the power controller. This function is available only in combination with a power controller which supports this feature (the IEPC does not). The power controller is to send the eight-bit “current feed value” synchronous to the B1-channel on IOM-2 (in the first time-slot if operated at a higher rate than 512 kHz). The value can be read out by the processing unit with a MON-8-message.

The DISS-pin is used for switching off the remote power supply of the subscriber line. It is set to (1) by the C/I-command “LTD” (0011_B). A software reset with C/I = “RES” does not affect the DISS-pin. While the DISS-pin is set to (1), the device is in the “TEST” state.

The following table summarizes the commands and messages used in conjunction with pins PS1, PS2 and DISS. In LT-modes the IOM-2-interface is used for access, in NT-modes access is achieved by U-interface bits.

Table 16
Power Controller Maintenance Bits (PS1, PS2, DISS)

LT-Modes		
Channel (IOM-Interface)	**Code**	**Function**
C/I	HI (out)	High level at pin PS1. A high level (1) at pin PS1 causes the device to be reset, to move into the “TEST” state and to issue the C/I-code “HI”
MON-8	RPFC (in)	Read power feed current. Requests the IEC-Q to return the current feed value which has been read from pin PS2. The answer MON-8 “APFC” will be returned in the next IOM-2 frame available. For timing requirements of serial data transfer between power controller and PS2 please see **section 4.1.3**
MON-8	APFC (out)	Answer power feed current. Contains the latest value of the power feeding current as read at pin PS2
C/I	LTD (in)	LT disable. After receipt of “LTD” the DISS-pin is set to (1) and the device is transferred into the “TEST” state.
NT-Modes		
Channel (U-Interface)	**Code**	**Function**
Overhead	M42 (PS1 bit)	Primary power supply status bit. The overhead bit is level sensitive. With pin PS1 set to (1) the overhead bit is set to (1). With pin PS1 set to (0) overhead bit M42 is set to (0)
Overhead	M43 (PS2 bit)	Secondary power status bit. The overhead bit is level sensitive. With pin P2 set to (1) the overhead bit is set to (1). With pin PS2 set to (0) overhead bit M43 is also set to (0)
EOC	LBBD	Close complete loop. In auto-mode this command causes also the DISS-pin being set to (1). The DISS pin is a reset to (0) with EOC “RTN” or reset

Applications:

For transferring C/I-commands to/from the ICC or EPIC proceed as described in **section 3.3.1.**

1) Switch-off remote power supply (initiated by LT):

IOM-2		IEC-Q	
C/I DC (1111_B)			; IEC-Q in “Deactivated” state
C/I LTD (0011_B)	———>	Pin DISS = (1)	; Request remote power supply ; to be switched-off ; IEC-Q is in “TEST” state
C/I HI (0011_B)	<———	Din PS1 = (1)	; Peripheral circuit confirms by ; setting pin PS1 to (1)

Cross-references:

3.1.1	**C/I-Channel Use with ICC and EPIC (Application)**
3.1.1	**Handshake Procedure with ICC and EPIC (Application)**
3.1.1	**MON-8-Commands (Application)**
4.1.1	**MON-8-Commands (Technical Description)**
4.1.3	**Interface (Technical Description)**

3.2 Control Procedures

Control procedures describe the commands and messages required to control the PEB 2091 in different modes and situations. This chapter shows the user how to activate and deactivate the device under various circumstances. In order to keep this chapter as application orientated as possible only actions and reactions the user needs to initiate or may observe are mentioned. Technical details on transmitted status bits and signals are described in **chapter 4.2 and 4.3** of this manual.

For transfer of the C/I-commands to and from the ICC or EPIC proceed as described in **section 3.1.1.**

Two types of start-up procedures are supported by the IEC-Q: cold starts and warm starts.

Cold starts are performed after a reset and require all echo and equalizer coefficients to be recalculated. This procedure typically is completed after 1-7 seconds depending on the line characteristic. Cold starts are recommended for activations where the line characteristic has changed considerably since the last deactivation.

A warm start procedure uses the coefficient set saved during the last deactivation. It is therefore completed much faster (maximum 300 ms). Warm starts are however restricted to activations where the line characteristic has not changed significantly since the last deactivation.

Both start-up procedures differ only in the fact that the device has been transferred into the TEST state prior to activation. Activation initialization and procedure is in both cases identical. The following sections thus apply to both warm and cold start-ups.

3.2.1 Complete Activation Initiated by LT

	NT IOM-2		LT IOM-2			
<———	C/I DC	(1111_B)	CI/DC	(1111_B)	<———	; Initial state is “Deactivated”
———>	C/I DI	(1111_B)	C/IDI	(1111_B)	———>	;
<———	C/I PU	(0111_B)	**C/I AR**	**(1000_B)**	**<–––––**	; Start activation
<———	C/I DC	(1111_B)	C/I AR	(1000_B)	———>	; Activation proceeds
			C/I ARM	(1001_B)	———>	; :
<———	C/I AR	(1000_B)	C/I UAI	(0111_B)	———>	; :
–––––>	**C/I AI**	**(1100_B)**				; Confirm that terminal is ; active
<———	C/I AI	(1100_B)	C/I AI	(1100_B)	———>	; Activation complete

3.2.2 Activation with ACT-Bit Status Ignored by Exchange Side

The LT ignores the ACT-bit transmitted upstream from the NT if the LT-activation has been initiated with AR0 instead of AR. Because the activation with AR0 is performed with the UOA-bit set to “0”, initially only a partial activation is started. By setting UOA = 1 via a MON2 message the S-interface is activated as well.

	NT IOM-2		LT IOM-2			
<———	C/I DC	(1111_B)	C/I DC	(1111_B)	<———	; Initial state is “Deactivated”
———>	C/I DI	(1111_B)	C/I DI	(1111_B)	———>	;
			C/I AR0	**(1101_B)**	**<–––––**	; Start activation
<———	C/I PU	(0111_B)	C/I AR	(1000_B)	———>	;
<———	C/I DC	(1111_B)	C/I ARM	(1001_B)	———>	;
			C/I UAI	(0111_B)	———>	;
			MON8 PACE	**(80 BE_H)**	**<––––**	; Enable control of UOA-bit
			MON2 UOA	**(2F FF_H)**	**<–––––**	; and set UOA = 1
<———	C/I AR	(1000_B)				
–––––>	**C/I AI**	**(1100_B)**				: Confirm that terminal is ; active
<———	C/I AR	(1000_B)	C/I UAI	(1100_B)	———>	; ACT-bit status ignored
			C/I AR	**(1000_B)**	**<–––––**	; Enable ACT-bit evaluation
<———	C/I AI	(1100_B)	C/I AI	(1100_B)	———>	; Activation complete
			C/I AR0	**(1101_B)**	**<–––––**	: Disable ACT-bit evaluation
<———	C/I AR	(1000_B)	C/I UAI	(0111_B)	———>	: ACT-bit status ignored

3.2.3 Complete Activation Initiated by TE

When initiating an activation from the terminal side, the LT must be in the “DEACTIVATED” state. For a TE initiated activation to be successful the downstream LT C/I-code must be DC. This is not the case if the “DEACTIVATED” state has been entered from the “TEST” state (the last code is DR in this case).

	NT IOM-2		LT IOM-2			
<———	C/I DC	(1111_B)	C/I DC	(1111_B)	<———	; Initial state is “Deactivated”
———>	C/I DI	(1111_B)	C/I DI	(1111_B)	———>	
–––––>	**C/I TIM**[1]	**(0000_B)**				; Start IOM-clocks
<———	C/I PU	(0111_B)				; IEC-Q is in power-up
–––––>	**C/I AR**	**(1000_B)**				
–––––>	**TIM release**[2]					; Start activation
<———	C/I DC	(1111_B)	C/I AR	(1000_B)	———>	; Activation proceeds
			C/I ARM	(1001_B)	———>	; :
<———	C/I AR	(1000_B)	C/I UAI	(0111_B)	———>	; :
–––––>	**C/I AI**	**(1100_B)**				; Confirm that terminal is
						; active
<———	C/I AI	(1100_B)	C/I AI	(1100_B)	———>	; Activation complete

Notes: [1] For the PEB 2070 TIM is requested with register SPCR = 80_H
[2] For the PEB 2070 TIM release is requested with register SPCR = 00_H

3.2.4 Activation Attempt Initiated by NT in NT-Auto-Mode

In IEC-Q Version 4.3 the NT-auto-mode has been additionally implemented. In this mode the NT IEC-Q will start one single activation attempt after leaving the “TEST” state, i.e. after being resetted. In case the LT is in the condition where it can be activated, activation proceeds as described in the previous section.

The example below illustrates the procedure if the LT refuses to acknowledge the activation attempt.

	NT IOM-2		LT IOM-2			
<———	C/I DR	(0000_B)	C/I DEAC	(0001_B)	———>	; Both side in “TEST” state
–––––>	**C/I RES**	**(0001_B)**	**C/I RES**	**(0001_B)**	**<–––––**	;
–––––>	**C/I DI**	**(1111_B)**				“TEST” state left for 1. time
<———	C/I DC	(1111_B)				NT activation attempt
<———	C/I EI1	(0100_B)				failes, because LT in
<———	C/I DR	(0000_B)				“TEST” state.
<———	C/I DC	(1111_B)				

3.2.5 Complete Deactivation

Deactivating the U-interface can be initiated only by the exchange. A deactivation can be started when the device is in the states “LINE ACTIVE”, “PEND. TRANSPARENT” of “TRANSPARENT”.

	NT IOM-2		LT IOM-2			
			C/I DR	(0000_B)	<———	; Start deactivation
<———	C/I DR	(0000_B)	C/I DEAC	(0001_B)	———>	; Deactivation proceeds
			C/I DI	(1111_B)	———>	; Deactivation complete on ; LT
———>	C/I DI	(1111_B)				; Power down NT
<———	C/I DC	(1111_B)				; Deactivation complete on ; NT

3.2.6 Partial Activation (U Only)

Activating the U-interface only partially is a requirement specified by the CNET. The S-interface remains deactivated.

When activating partially from the LT-side, the exchange has two options:

First, in case the C/I-command DC is not issued after the partial activation is complete, the exchange has to issue AR (see **section 3.2.8** case 1) before a terminal initiated complete activation request is accepted. This allows the exchange to retain full control, even in case of terminal initiated activation requests.

Secondly the exchange can issue DC after UAI has been received. This allows the terminal to activate the S-interface independently of the exchange (see **section 3.2.8** case 2). In this case the exchange has no control of the S-interface activation procedure.

	NT IOM-2		LT IOM-2			
<———	C/I DC	(1111_B)	C/I DC	(1111_B)	<———	; Initial state is “Deactivated”
———>	C/I DI	(1111_B)	C/I DI	(1111_B)	———>	
			C/I UAR	**(0111_B)**	**<–––––**	; Start partial activation
<———	C/I PU	(0111_B)	C/I AR	(1000_B)	———>	; Activation proceeds
<———	C/I DC	(1111_B)	C/I ARM	(1001_B)	———>	; :
			C/I UAI	(0111_B)	———>	; Partial activation complete
			[C/I DC	(1111_B)]	<———	; Exchange retains no con- ; trol of S-interface activation

3.2.7 Complete Activation Initiated by LT with U Active

When U is already active, the S-interface can be activated either by the exchange or the terminal. The first case is described here, the second in the next section.

	NT IOM-2		LT IOM-2			
<———	C/I DC	(1111_B)	C/I UAR [DC]		<———	; U only is activated
———>	C/I DI	(1111_B)	C/I UAI	(0111_B)	———>	; [exchange retains no control]
			C/I AR	**(1000_B)**	**<–––––**	; Start complete activation
<———	C/I AR	(1000_B)				
–––––>	**C/I AR**	**(1100_B)**				
			C/I AR	(1000_B)	———>	; Activation proceeds
–––––>	**C/I AI**	**(1100_B)**				; Confirm that terminal is active
			C/I UAI	(0111_B)	———>	
<———	C/I AI	(1100_B)	C/I AI	(1100_B)	———>	; Activation complete

3.2.8 Complete Activation Initiated by TE with U Active

When the terminal requests to activate the S-interface (U-interface already active) two cases can occur:

In the first case the exchange has retained control over the S-interface activation. Then S-activation can proceed only after the explicit permission by the exchange with AR. This situation is discussed in this section under “case 1”.

In the second case the exchange is not requested to send AR in order to continue activation. This situation is described in “case 2” of this section.

The terminal recognizes no difference between the two types, the procedure on NT-side consequently is identical in both cases.

Case 1 (controlled by exchange)

	NT IOM-2		LT IOM-2			
<———	C/I DC	(1111_B)	C/I UAR	(0111_B)	<———	; U only is activated
———>	C/I DI	(1111_B)	C/I UAI	(0111_B)	———>	
–––––>	**C/I AR**	**(1000_B)**				; Terminal requests activation
			C/I AR	(1000_B)	———>	; Exchange is notified of request
			C/I AR	**(1000_B)**	**<–––––**	; Exchange permits S-activation
<———	C/I AR	(1000_B)				
–––––>	**C/I AI**	**(1100_B)**				; Confirm that terminal is active
			C/I UAI	(0111_B)	———>	
<———	C/I AI	(1100_B)	C/I AI	(1100_B)	———>	; Activation complete

Case 2 (no control by exchange)

	NT IOM-2		LT IOM-2			
<———	C/I DC	(1111_B)	C/I DC		<———	; U only is activated
———>	C/I DI	(0011_B)	C/I UAI	(0111_B)	———>	
–––––>	**C/I AR**	**(1000_B)**				; Terminal requests activation
			C/I AR	(1000_B)	———>	; Exchange is notified of
<———	C/I AR	(1000_B)				; proceeding S-activation
–––––>	**C/I AI**	**(1100_B)**				; Confirm that terminal is active
			C/I UAI	(0111_B)	———>	
<———	C/I AI	(1100_B)	C/I AI	(1100_B)	———>	; Activation complete

3.2.9 Deactivating S/T-Interface Only

The following shows the procedure for deactivating the S-interface only while leaving the U-interface active.

	NT IOM-2		LT IOM-2			
<———	C/I AI	(1100_B)	C/I AI	(1100_B)	———>	; Initial state: layer 1 activated
———>	C/I AI	(1100_B)	C/I AR	(1000_B)	<———	
<———	C/I DR	(0000_B)	**C/I UAR**	**(0111_B)**	**<–––––**	; Deactivate S-interface only
–––––>	**C/I DI**	**(1111_B)**	C/I UAI	(0111_B)	———>	; S-interface is deactivated
<———	C/I DC	(1111_B)	[C/I DC	(1111_B)]	<———	; Exchange retains no control

3.2.10 Activation Initiated by LT with Repeater

For LT and NT the activation procedure with a repeater between exchange and network is identical to that described at the beginning of this chapter. The repeater transforms the received U-signals into C/I-codes and monitor messages. These codes and messages pass the repeater control unit (e.g. ASIC). In this control unit a number of adaptations are made to comply with a specific national specification.

In this section only C/I-codes are considered which need to be transformed by the control unit such that the repeater counterpart will operate correctly. In addition overhead bits and the specified 2B + D data needs to be transferred for a correct repeater activation/deactivation.

In order to recognize the dependence of LT-RP- and NT-RP-signals more easily, the arrows point towards the middle.
When activating the repeater unit from the exchange side, the UAI-code issued by the LT-RP needs to be converted into AI for the NT-RP.

LT-RP IOM-2				NT-RP IOM-2		
C/I DC	(1111_B)	<———	<——— C/I PU	(0111_B)	;	Initial state “Power Up” to provide timing
C/I DI	(1111_B)	———>	———> C/I TIM	(0000_B)		
C/I AR	(1000_B)	<———	<——— C/I DC	(1111_B)	;	Activation started by LT
C/I AR	(1000_B)	———>	<——— C/I AR	(1000_B)		
C/I ARM	(1001_B)	———>			;	Activation proceeds
C/I UAI	(0111_B)	———>	———> C/I AI	(1100_B)		
C/I AI	(1100_B)	———>	<——— C/I AI	(1100_B)	;	Activation complete

3.2.11 Activation Initiated by TE with Repeater

In order to recognize a terminal initiated activation successfully the NT-RP must be in “Power Up” condition to provide clocks for the LT-RP. During the activation procedure the LT-RP-signal “UAI” needs to be changed into “AI” by the control unit.

LT-RP IOM-2				NT-RP IOM-2		
C/I DC	(1111_B)	<———	<——— C/I PU	(0111_B)	;	Initial state “Power Up” to provide timing
C/I DI	(1111_B)	———>	———> C/I TIM	(0000_B)		
C/I AR	(1000_B)	———>	———> C/I AR	(1000_B)	;	Terminal requests activation
C/I AR	(1000_B)	<———	<——— C/I AR	(1000_B)	;	Activation proceeds
C/I ARM	(1001_B)	———>				
C/I UAI	(0111_B)	———>	———> C/I AI	(1100_B)		
C/I AI	(1100_B)	———>	<——— C/I AI	(1100_B)	;	Activation complete

3.2.12 Deactivation by Repeater

The start of a deactivation procedure is passed from the LT- to the NT-side via overhead bits in the U-frame. These are interpreted by the LT-RP. Thereafter the deactivation process in LT-RP and NT-RP is running mostly independent of each other as illustrated below. No C/I-codes need to be converted by the control unit. The NT-RP, upon reception of DC should however be forced to stay in “Power Up” in order to retain the clocks. Thereby a TE initiated repeater activation will be enabled.

LT-RP IOM-2				NT-RP IOM-2		
C/I AR	(1000_B)	<———	<——— C/I AI	(1100_B)	;	Layer 1 is activated
C/I AI	(1100_B)	———>	———> C/I AI	(1100_B)		
C/I DR	(0000_B)	<———	<——— C/I AR	(1000_B)	;	Deactivation started by LT
C/I DEAC	(0001_B)	———>	<——— C/I DR	(0000_B)	;	Deactivation proceeds
C/I DI	(1111_B)	———>	———> C/I DI	(1111_B)		
C/I DC	(1111_B)	<———	<——— C/I DC	(1111_B)	;	Deactivation complete
			———> C/I TIM	(0000_B)	;	Stay in “Power Up” to keep clocks
			<——— C/I PU	(0111_B)	;	turned on.

3.3 Maintenance Functions

This chapter summarizes all features provided by the IEC-Q Vers. 4.3 to support maintenance functions and system measurements. Three main groups may be distinguished:

– maintenance functions to close and open test loop-backs
– features facilitating the recognition of transmission errors
– test modes required for system measurements

A fourth group yields information about the access to internal chip data. As a use of this feature requires very detailed knowledge about the internals of the IEC-Q, only in few cases these informations will be of practical relevance to the user.

The next four sections describe how these maintenance functions are used in applications.

3.3.1 Test Loop-Backs

Test loop-backs are specified by the national PTTs in order to facilitate the location of defect systems. Four different loop-backs are defined. The position of each loop-back is illustrated in **figure 36**.

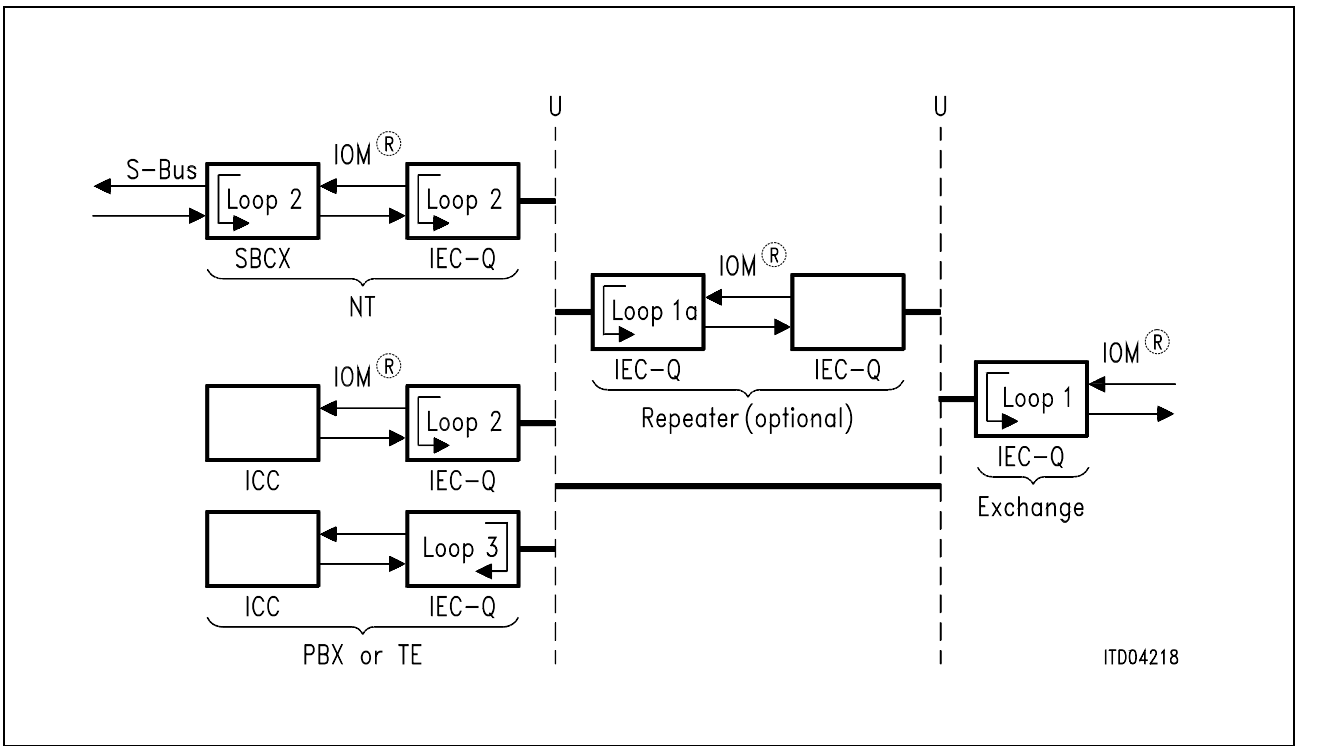


Figure 36
Test Loop-Backs Supported by the PEB 2091

Loop-backs #1, #1A and #2 are controlled by the exchange. Loop-back #3 is controlled by the terminal. All four loop-back types are transparent. This means all bits that are looped back will also be passed onwards in the normal manner.

The next sections describe how these loop-backs are closed and opened using the C/I- and MON-commands available to the IEC-Q.

3.3.1.1 Analog Loop-Back (No. 1/No. 3)

Both loop-back #1 and loop-back #3 are closed by the IEC-Q as near to the U-interface as possible. For this reason they are also called analog loop-backs. All analog signals will still be passed on to the U-interface. This results in the opposite station (NT in case of #1, LT in case of #3) to be activated as well.

Before an analog loop-back is closed with the C/I-command ARL (activation request loop-back), the device should have been reset.

In order to open an analog loop-back correctly, reset the device into the TEST state with the C/I-command RES (or by pin reset). This ensures that the echo coefficients and equalizer coefficients will converge correctly when activating the following time.

Although loop-back #1 and loop-back #3 are closed with the same command and perform the same function, they cannot be started from the same state: Loop-back #1 is closed when in the state “Deactivated” (LT-side); loop-back #3 can only be closed in the state “Test” (NT side).

The examples below demonstrate the use of loop-backs #1 and #3.

Loop-back #1 (LT-side)

	NT IOM-2		LT IOM-2			
<———	C/I DC	(1111_B)	C/I DI	(1111_B)	———>	
			C/I ARL	**(1010_B)**	**<–––––**	; Close loop-back #1
<———	C/I AR	(1000_B)	C/I AR	(1000_B)	———>	; Activation proceeds in NT
			C/I ARM	(1001_B)	———>	; and LT
			C/I UAI	(0111_B)	———>	; Activation complete, ; #1 closed
			C/I RES	**(0001_B)**	**<–––––**	; Open loop-back #1, ; reset the IEC-Q

Loop-back #3 (NT-side)

For correct operation of this example it is assumed that IOM-clock signals (FSC and DCL) are present. If not, use the timing command first.

	NT IOM-2		LT IOM-2			
–––––>	**C/I RES**	**(0001_B)**	C/I DI	(1111_B)	———>	; NT in “Test” state
<———	C/I DR	(0000_B)				
–––––>	**C/I ARL**	**(1010_B)**				; Close loop-back #3
<———	C/I DC	(1111_B)				
<———	C/I AR	(1000_B)				; NT act. complete, #3 closed
–––––>	**C/I RES**	**(0001_B)**				; Open #3 and reset NT

3.3.1.2 Partial and Complete Loop-Back (No. 2)

For loop-back #2 several alternatives exist. Both the type of loop-back and the location may vary. Three loop-back types belong to the loop-back-#2 category:

– Complete loop-back
– B1-channel loop-back
– B2-channel loop-back

The complete loop-back comprises both B-channels and the D-channel. It may be closed either in the IEC-Q itself or in a downstream device. Single-channel loop-backs are always performed within the IEC-Q. In this case the digital data of DOUT will be directly fed back into DIN. This also applies if the complete loop-back is closed in the IEC-Q.

Normally loop-back #2 is controlled from the exchange. The EOC monitor commands LBBD, LB1 and LB2 are used. They will be recognized and executed automatically in the NT IEC-Q if the auto-mode is selected. Alternatively (e.g. when NT operates in transparent mode) MON-8-commands are available.

All loop-back functions are latched. This allows channel B1 and channel B2 to be looped back simultaneously. All loop-backs are opened when the EOC command RTN or the MON-8-command NORM is sent.

3.3.1.2.1 Complete Loop-Back

When receiving the EOC-command LBBD in auto-mode, the NT IEC-Q does not close the loop-back immediately. Because the intention of this loop-back is to test the complete NT, the IEC-Q passes the complete loop-back request on to the next downstream device (e.g. SBCX). This is achieved by issuing the C/I-code AIL in the “Transparent” state or C/I = ARL in states different than “Transparent”. If the downstream device is not able to close the complete loop-back, a MON-8-message LBBD may be returned to the NT IEC-Q. This then will close the complete loop-back within the IEC-Q itself (B1 + B2 + D-channels). All remaining IOM-information (monitor, C/I-channel as well as the bits MR and MX) are still read from the IOM-2-interface. For this reason it is still possible for a layer-2 device to deactivate the NT despite the fact that the loop-backs are controlled by the exchange.

Figure 37 illustrates these two options.

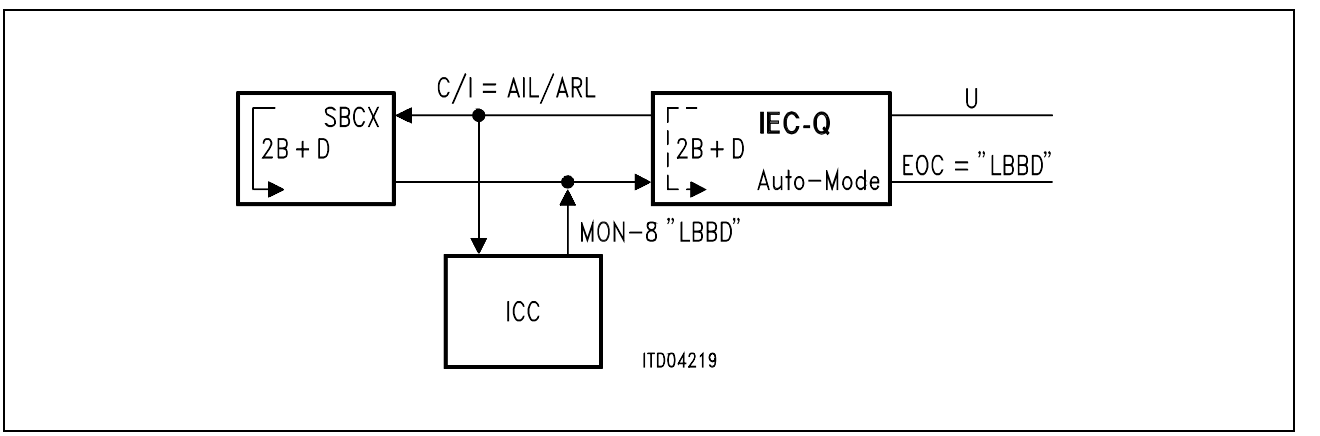


Figure 37
Complete Loop-Back Options in NT-Modes

Note: If operated in auto-mode, the complete loop-back can only be closed in the IEC-Q if previously the EOC-command LBBD was received. Without this EOC-message the MON-8-command LBBD will be ignored.
If operated in transparent mode, a complete loop-back may be closed at any time with MON-8 LBBD.

Complete Loop-Back in NT-Auto-Mode:

In auto-mode the complete loop-back is reset after RTN has been received in the EOC-channel. In transparent mode MON-8 NORM is used for this purpose. No reset as for loop-backs #1 or #3 is required for loop-back #2. The line is active and ready for data transmission.

The typical procedure for closing and opening a complete loop-back is demonstrated in the examples below.

	NT IOM-2		LT IOM-2			
			C/I AR	(1000_B)	<———	; U-interface is activated
<———	C/I AR	(1000_B)	C/I UAI	(0111_B)	———>	; without terminal
						; confirmation
(———>	C/I AI	(1100_B)				; or with
<———	C/I AI	(1100_B)	C/I AI	(1100_B)	———>	; terminal confirmation)
			MON-0 LBBD	**(50_H)**	**<–––––**	; Close complete loop (EOC)
<———	C/I AIL	(1110_B)				; Request for downstream
<———	MON-0 LBBD	(50_H)				; device to close complete ; loop-back
			MON-0 LBBD	(50_H)	———>	; Receive acknowledgment
–––––>	**MON-8 LBBD**	**($F1_H$)**				; If downstream device can't ; close, loop is closed in IEC
			MON-0 RTN	**(FF_H)**	**<–––––**	; Open all loop-backs
<———	MON-0 RTN	(FF_H)				; All loop-backs opened
			MON-0 RTN	(FF_H)	———>	; Receive acknowledgment

In the above example the LT is operated in auto-mode.

Complete Loop-Back in Transparent NT-Mode:

	NT IOM-2		LT IOM-2			
———>	C/I AI	(1100_B)	C/I AR	(1000_B)	<———	; U-interface is activated
<———	C/I AI	(1100_B)	C/I AI	(1100_B)	———>	
			MON-0 LBBD	**(50_H)**	<———	; Close complete loop (EOC)
<———	MON-0 LBBD	(50_H)				; Request passes IEC ; transparent
–––––>	**MON-0 LBBD**	**(50_H)**	MON-0 LBBD	(50_H)	———>	; Transmit acknowledgment
–––––>	**MON-8 LBBD**	**($F1_H$)**				; Close complete loop in IEC
			MON-0 RTN	**(FF_H)**	<———	; Request to open all loops
–––––>	**MON-0 RTN**	**(FF_H)**	MON-0 RTN	(FF_H)	———>	; Receive acknowledgment
–––––>	**MON-8 NORM**	**(FF_H)**				; Open all loop-backs

In the above example the LT is operated in auto-mode.

3.3.1.2.2 Single-Channel Loop-Backs

Single-channel loop-backs are always performed directly in the IEC-Q. No difference between the B1-channel and the B2-channel loop-back control procedure exists. They are therefore discussed together.

In auto-mode the B1-channel is closed with the EOC-command LB1. LB2 causes the channel B2 to loop-back. Because these functions are latched, both channels may be looped back simultaneously by sending first the command to close one channel followed by the command for the remaining channel.

In transparent mode, single channels are closed with the corresponding MON-8-commands.

Single-channel loop-backs are resolved in the same manner as described for the complete loop-back. The NT may be deactivated with layer 2 while single loop-backs are closed.

Single-Channel Loop-Back in NT-Auto-Mode:

	NT IOM-2		LT IOM-2			
———>	C/I AI	(1100_B)	C/I AR	(1000_B)	<———	; U-interface is activated
<———	C/I AI	(1100_B)	C/I AI	(1100_B)	———>	
			MON-0 LB1	**(51_H)**	<———	; Close B1 loop (EOC)
<———	MON-0 LB1	(51_H)				; Loop B1 closed
			MON-0 LB1	(51_H)	———>	; Receive acknowledgment
			MON-0 LB2	**(52_H)**	<———	; Close B2 loop-back (EOC)
<———	MON-0 LB2	(52_H)				; Loop-back B1 and B2 ; closed

	NT IOM-2		LT IOM-2			
			MON-0 LB2	(52_H)	———>	; Receive acknowledgment
			MON-0 RTN	**(FF_H)**	<———	; Open all loop-backs
<———	MON-0 RTN	(FF_H)				; All loop-backs opened
			MON-0 RTN	(FF_H)	———>	; Receive acknowledgment

In the above example the LT is operated in auto-mode.

Single-Channel Loop-Back in NT-Transparent Mode:

	NT IOM-2		LT IOM-2			
———>	C/I AI	(1100_B)	C/I AR	(1000_B)	<———	; U-interface is activated
<———	C/I AI	(1100_B)	C/I AI	(1100_B)	———>	
			MON-0 LBBD	**(51_H)**	<———	; Close B1 loop (EOC)
<———	MON-0 LB1	(51_H)				; Request passes IEC ; transparent
–––––>	**MON-0 LB1**	**(51_H)**	MON-0 LBBD	(51_H)	———>	; Transmit acknowledgment
–––––>	**MON-8 LB1**	**($F4_H$)**				; Close B1 loop in IEC
			MON-0 LBBD	**(52_H)**	<———	; Close B2 loop (EOC)
<———	MON-0 LB2	(52_H)				; Request passes IEC ; trabsparent
–––––>	**MON-0 LB2**	**(52_H)**	MON-0 LB2	(52_H)	———>	; Transmit acknowledgment
–––––>	**MON-8 LB2**	**($F2_H$)**				; Close B2 loop in IEC ; B1 and B2 closed
			MON-0 RTN	**(FF_H)**	<———	; Request to open all loops
–––––>	**MON-0 RTN**	**(FF_H)**	MON-0 RTN	(FF_H)	———>	; Receive acknowledgment
–––––>	**MON-8 NORM**	**(FF_H)**				; Open all loop-backs

In the above example the LT is operated in auto-mode.

3.3.1.3 Repeater Loop-Back (No. 1A)

Loop-back #1A is always closed in the repeater. Functionally it corresponds to loop-backs #1 and #3 on the exchange and on the network side. If a line contains more than one repeater unit, it is possible to address each unit individually in order to close loop-back #1A in the specified unit only.

For loop-back #1A everything described in **section 3.3.1** (Analog Loop-Back) applies: The loop-back is opened with the C/I-command RES, closed with the C/I-command ARL, and it is closed as near to the U-interface as possible. The difference results from the fact that the command ARL needs to be generated by the repeater control unit (µP system or ASIC) according to national repeater specifications.

This specification defines an EOC-command which will activate loop-back #1A if received in conjunction with the repeater address (001_B). The NT-RP is operating in transparent mode. The repeater control unit watches for MON-0-commands with address (001_B). If the predefined loop-back #1A command is received, the repeater control unit sends the C/I-code ARL to the LT-RP and loop-back #1A will be closed.

In case the address (000_B) or (111_B) (NT and broadcast address) is received, the control unit ignores all MON-0-commands and leaves the address unchanged.

Should the address read (010_B) to (110_B), the MON-0-command will be ignored but the address will be decremented. This procedure is described in **section 3.3.1** (EOC-Programming) and allows individual repeater addressing.

Figure 38 illustrates this in a system with two repeater units where the second unit is requested to close loop-back #1A.

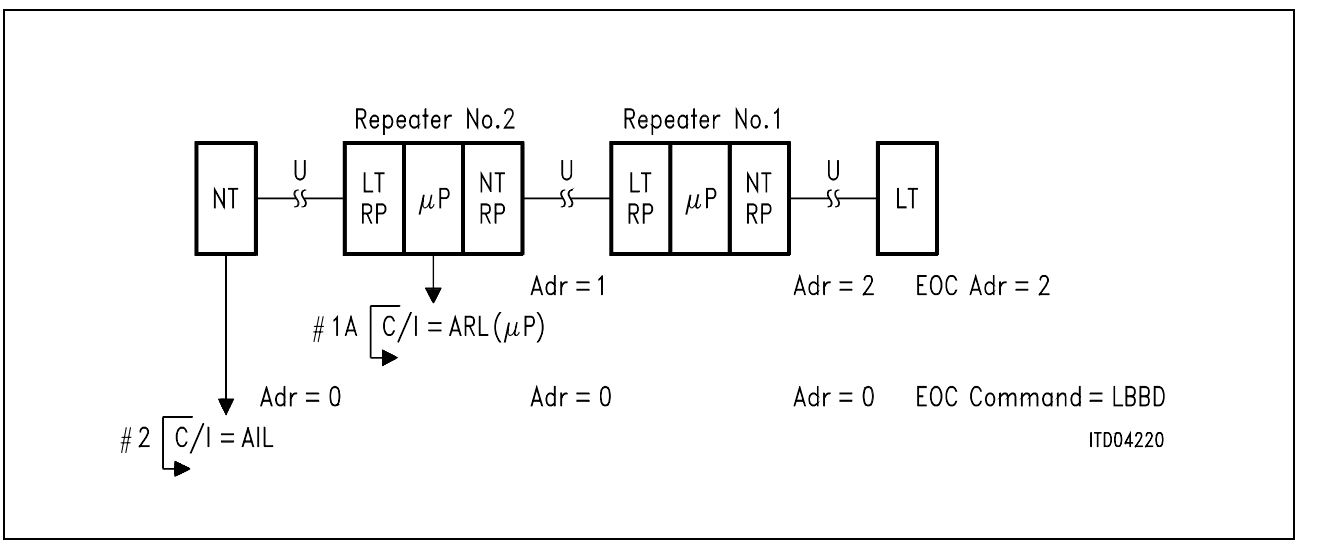


Figure 38
Closing Loop-Back #1A in a Multi-Repeater System

3.3.2 Block Error Counters

The IEC-Q provides internal counters for far-end and near-end block errors. This allows a comfortable surveillance of the transmission quality at the U-interface. In addition, MON-messages indicate the occurrence of near-end errors, far-end errors, and the simultaneous occurrence of both errors.

A block error is detected each time when the calculated checksum of the received data does not correspond to the control checksum transmitted in the successive superframe. One block error thus indicates that one U-superframe has not been transmitted correctly. No conclusion with respect to the number of bit errors is therefore possible.

The following two sections describe the operation of near and far-end block error counters as well as the commands available to test them.

3.3.2.1 Near-End and Far-End Block Error Counter

A near-end block error (NEBE) indicates that the error has been detected in the receive direction (i.e. NEBE in the NT = LT => NT error). This will be indicated with a MON-1-message NEBE in all NT-modes as well as the LT-RP-mode. Each detected NEBE-error increments the 8-bit NEBE-counter. When reaching the maximum count, counting is stopped and the counter value reads (FF_H).

The current value of the NEBE counter is read in both LT- and NT-modes with the MON-8-command RBEN. The response comprises two bytes: the first byte always indicates that a MON-8-message is replied to (80_H), the second represents the counter value (00_H) … (FF_H). Each read operation resets the counter to (00_H).

A far-end block error identifies errors in transmission direction (i.e. FEBE in the NT = NT => LT-error). FEBE errors are processed in the same manner as NEBE-errors. A far-end block error will be indicated with a MON-1-message FEBE (NT-modes and LT-RP). The FEBE counter is read and reset with the MON-8-command RBEF.

In case both, far-end and near-end block errors occur simultaneously, the MON-1-message FNBE will be issued in all NT-modes and the LT-RP-mode.

The following section illustrates how block error counters can be tested.

3.3.2.2 Testing Block Error Counters

Figure 39 illustrates how near- and far-end block error counters can be tested. Transmission errors are simulated with artificially corrupted CRCs. With two commands the cyclic redundancy checksum can be inverted. A third command offers to invert single FEBE-bits.

MON-8 CCRC causes the IEC-Q to permanently transmit inverted CRCs. This command may be used on LT-side with the LT in transparent or auto-mode. On the terminal side CCRC is only required when the device is operated in transparent mode.

In NT-auto-mode corrupted CRCs can be requested directly from the LT-side with the MON-0 command RCC. Again the CRC will be permanently inverted.

With the MON-8-command SFB it is possible on LT- and NT-side to invert single FEBE-bits. Because this command does not provoke permanent FEBE-bit inversion but sets only one FEBE-bit to (0) per SFB command, it is possible to predict the exact FEBE-counter reading.

Note: The main application for setting single FEBE-bits are repeater stations not operating in the LT-RP- or NT-RP-mode).

With CCRC issued on LT-side, near-end block errors will be observed at the NT and far-end errors are noticed at the LT.

After RCC is issued on the LT-side (NT in auto-mode), near-end block errors will be registered on the LT-side. In NT-modes the functional behavior of the FEBE-counter depends on the mode selected:

Auto-mode	FEBE-detection stopped, no MON-1 FEBE-messages and FEBE-counter disabled
Transparent mode	FEBE-detection enabled, MON-1-message FEBE issued and FEBE-counter enabled

With the MON-0-command NCC issued on LT-side the NEBE-detection can be disabled depending on the NT-mode selected:

Auto-mode	NEBE-detection stopped, no MON-1 NEBE-messages and NEBE-counter disabled
Transparent mode	NEBE-detection enabled, MON-1-message NEBE issued and NEBE-counter enabled

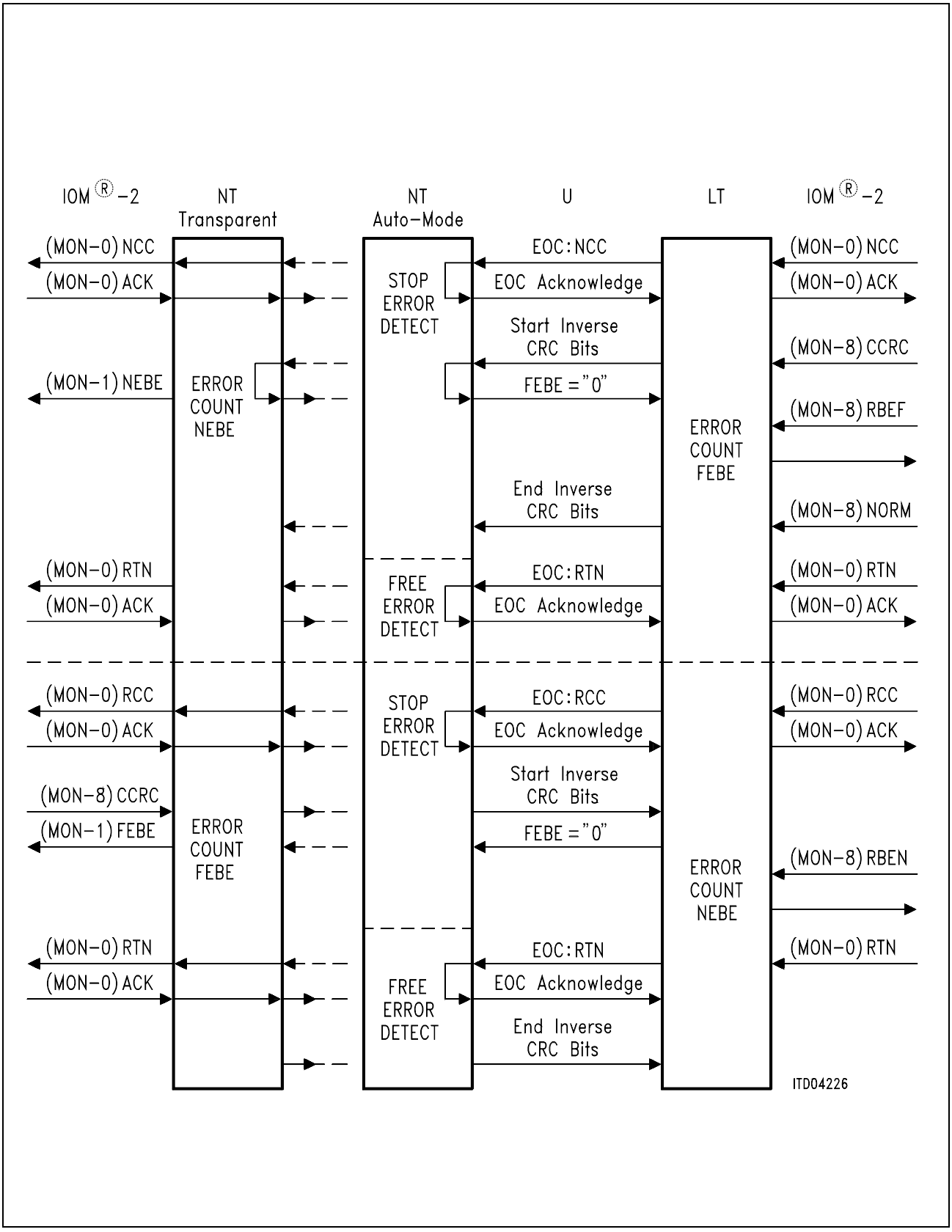


Figure 39
Block Error Counter Test

3.3.3 Test Modes and System Measurements

With a number of operational modes the IEC-Q Vers. 4.3 supports system measurements. These modes along with the most frequently needed system measurements are described in the following sections.

3.3.3.1 Single-Pulses Test Mode

In the single-pulses test mode, the IEC-Q transmits on the U-interface alternating ± 3 pulses spaced by 1.5 ms. This test mode is used in LT- and NT-like modes. Two options exist for selecting the "Send-Single-Pulses" (SSP) mode:

– hardware selection: RESQ = 1 & TSP = 1
– software selection: C/I = SSP (0101_B)

Both methods are fully equivalent. In the SSP-mode the C/I-code transmitted by the IEC is DEAC in LT-modes and DR in the NT-modes.

The SSP-test mode is required for pulse mask measurements.

3.3.3.2 Data-Through Mode

When selecting the data-through mode, the IEC-Q is forced directly into the "Transparent" state. This is possible from any state in the state diagram.

The Data-Through option (DT) provides the possibility to transmit a standard scrambled U-signal even if no U-interface wake-up protocol is possible. This feature is of interest when no counter station can be connected to supply the wake-up protocol signals. The DT-test mode may be used in LT- and NT-like applications.

As with the SSP-mode, two options are available.

– hardware selection: RESQ = 0 & TSP = 1
– software selection: C/I = DT (0110_B)

Compared with the software selection, a hardware selection offers the option to initiate IEC-Q actions via C/I-code (e.g. analog loop-back with C/I = ARL).

The DT-mode is required for power spectral density and total power measurements.

3.3.3.3 Master-Reset Mode

The master-reset mode characterizes the mode where the IEC-Q does not transmit any signals. The chip is in the "Test" state. All echo canceller and equalizer coefficients are reset. As can be seen from the state diagram, no activation is possible in LT- or NT-modes when the device is in the "Test" state.

For measurements two methods are recommended in order to transfer the IEC-Q into the master-reset mode:

– hardware selection: RESQ = 0 & TSP = 0
– software selection: C/I = RES (0001_B)

Both alternatives are fully compatible.

The C/I-code transmitted by the IEC-Q in the “Test” state is DEAC in LT-modes and DR in all NT-modes.

In LT-modes two additional options exist to transfer the device into the “Test” state. They are however intended to be used only to control the power supply, not for test purposes.

– hardware selection: Pin PS1 = (1)
– software selection: C/I = LTD (0011_B)

In case of the first option (PS = 1), HI will be issued instead of DEAC for a C/I-code. The second option results in C/I = DEAC but activates the DISS-pin.

The master-reset test mode is used for the return-loss measurements.

3.3.3.4 Pulse Mask Measurement

– Pulse mask is defined in ANSI T1.601 1991
– U-interface has to be terminated with 135 Ω
– IEC-Q is in “Single-Pulses” mode (C/I = 0101 or/RESQ = 1 & TSP = 1)
– Measurements are done using an oscilloscope

3.3.3.5 Power Spectral-Density Measurement

– PSD is defined in ANSI T1.601 1991
– U-interface has to be terminated with 135 Ω
– IEC-Q is in “Data-Through” mode (C/I = 0110 or/RESQ = 0 & TSP = 1)
– For measurements a spectrum analyzer is employed

3.3.3.6 Total Power Measurement

– Total power is defined in ANSI T1.601 1991
– Total power must be between 13 dBm and 14 dBm
– U-interface has to be terminated with 135 Ω
– IEC-Q is in “Data-Through” mode (C/I = 0110 or/RESQ = 0 & TSP = 1)
– Measurements are done using an 80 kHz high-impedance low-pass filter and true RMS-voltmeter

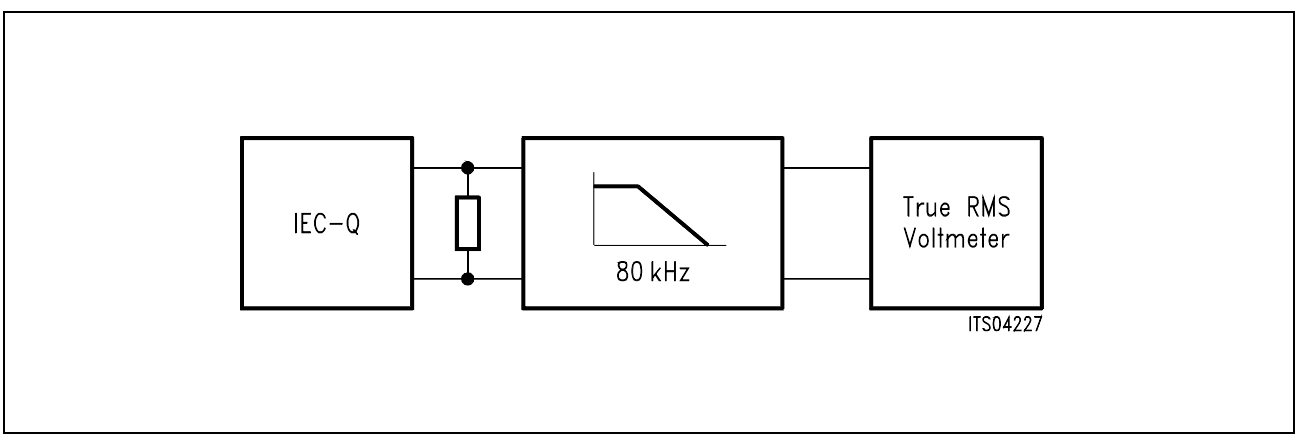


Figure 40
Total Power Measurement Set-Up

3.3.3.7 Return-Loss Measurement

– Return loss is defined in ANSI T1.601 1991
– IEC-Q is in “Test” state (C/I = 0001 or/RESQ = 0 & TSP = 0)
– Measure complex impedance “Z” from 14 kHz – 200 kHz
– Calculate return loss with formula:

RL(dB) = 20log (abs((Z + 135) / (Z –135)))

3.3.3.8 Quiet Mode Measurement

– Quite mode is defined in ANSI T1.601 1991
– IEC-Q is in the “Test” state (C/I = 0001 or/RESQ = 0 & TSP = 0)
– Trigger and exit criteria have to be realized externally

3.3.3.9 Insertion Loss Measurement

– Insertion loss is defined in ANSI T1.601 1991
– IEC-Q is in “Data-Through” mode (C/I = 0110 or/RESQ = 0 & TSP = 1)
– Trigger and exit criteria have to be realized externally

3.3.4 Chip Internal Test Options

In addition to the features described in the previous sections, the IEC-Q permits limited access to internal test procedures and internal data.

3.3.4.1 Self-Test

This test is intended to be requested by the terminal in order to verify correct performance. The self-test is started with the MON-1-command ST. No tests are performed within the IEC-Q. If the ST-message has been received correctly, the device returns the MON-1-message STP (self-test passed) to the terminal. With this function the terminal has a possibility to check the existence of a layer-1 device. This test is available for NT-modes only.

Cross-reference: **3.3.1 MON-1-Messages (Application)**
4.1.1 MON-1-Messages (Technical Description)

3.3.4.2 Coefficient Values

Some of the internal chip registers can be read via MON-8-messages.

Of interest to the user are the values of the coefficients for equalizer and echo canceller. This information will however only proof useful if a detailed, theoretical chip knowledge exists.

Registers are read by sending a two-byte MON-8-message. The first byte identifies the command as an internal register access, the second addresses the register.

The 16-bit register value is returned in two messages of two bytes each.

Cross-reference: **4.4.3 Coefficient Values (Technical Description)**

3.3.4.3 Test Pins

Two test pins, TP (pin 29) and TP1 (pin 20), exist. They are used for Siemens internal testing purposes and have no relevance to the user. For a correct operation of the IEC-Q, these pins should not be connected.

VAKAT