

- Advanced Process Technology
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Ease of Paralleling
- Simple Drive Requirements

### Description

Fifth Generation HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.

The D<sup>2</sup>Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D<sup>2</sup>Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.

The through-hole version (IRF630NL) is available for low-profile application.

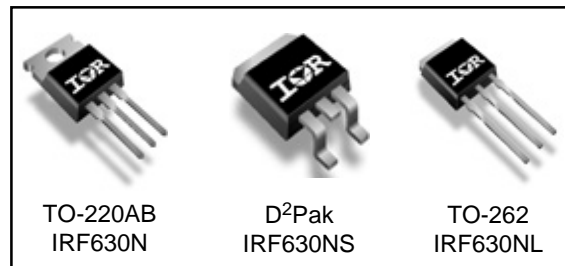
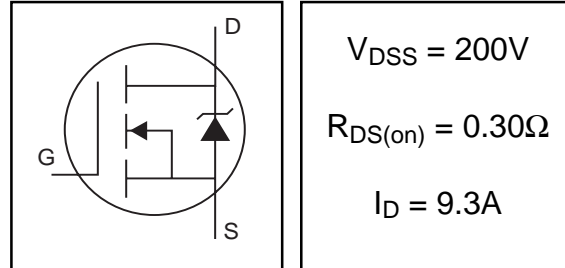
### Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D$ @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	9.3	A
$I_D$ @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	6.5	
$I_{DM}$	Pulsed Drain Current ①	37	
$P_D$ @ $T_C = 25^\circ\text{C}$	Power Dissipation	82	W
	Linear Derating Factor	0.5	W/°C
$V_{GS}$	Gate-to-Source Voltage	±20	V
$E_{AS}$	Single Pulse Avalanche Energy②	94	mJ
$I_{AR}$	Avalanche Current①	9.3	A
$E_{AR}$	Repetitive Avalanche Energy①	8.2	mJ
dv/dt	Peak Diode Recovery dv/dt ③	8.1	V/ns
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to +175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case )	
	Mounting torque, 6-32 or M3 screw④	10 lbf•in (1.1N•m)	

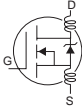
www.irf.com

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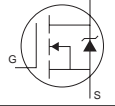
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## Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

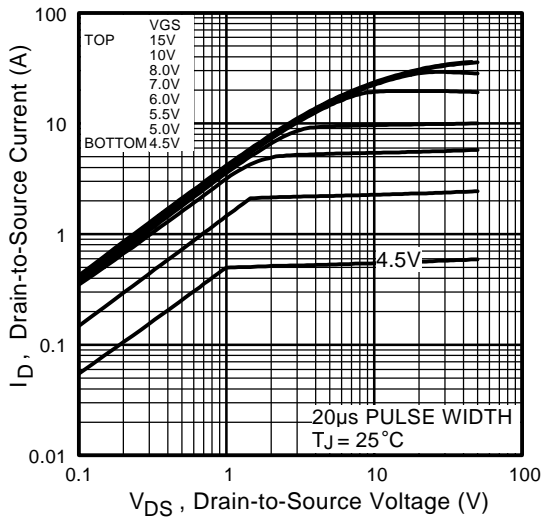
	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	200	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS/ΔT<sub>J</sub></sub>	Breakdown Voltage Temp. Coefficient	—	0.26	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	—	0.30	Ω	V <sub>GS</sub> = 10V, I <sub>D</sub> = 5.4A ③
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
g <sub>fs</sub>	Forward Transconductance	4.9	—	—	S	V <sub>DS</sub> = 50V, I <sub>D</sub> = 5.4A ③
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	25	μA	V <sub>DS</sub> = 200V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 160V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 150°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -20V
Q <sub>g</sub>	Total Gate Charge	—	—	35	nC	I <sub>D</sub> = 5.4A
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	6.5		V <sub>DS</sub> = 160V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	—	17		V <sub>GS</sub> = 10V ③
t <sub>d(on)</sub>	Turn-On Delay Time	—	7.9	—	ns	V <sub>DD</sub> = 100V
t <sub>r</sub>	Rise Time	—	14	—		I <sub>D</sub> = 5.4A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	27	—		R <sub>G</sub> = 13Ω
t <sub>f</sub>	Fall Time	—	15	—		R <sub>D</sub> = 18Ω ③
L <sub>D</sub>	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L <sub>S</sub>	Internal Source Inductance	—	7.5	—		
C <sub>iss</sub>	Input Capacitance	—	575	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	89	—		V <sub>DS</sub> = 25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	25	—		f = 1.0MHz

## Source-Drain Ratings and Characteristics

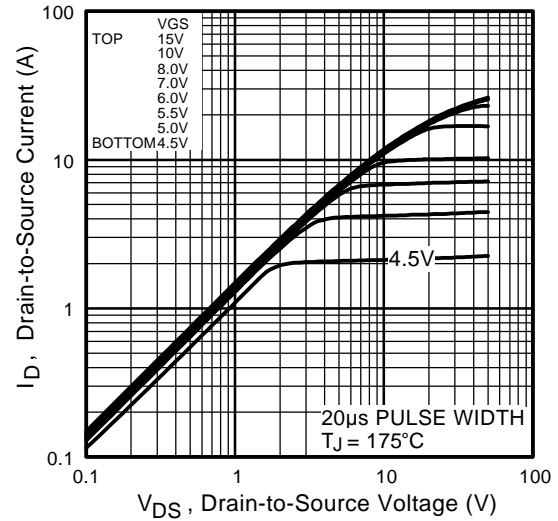
	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	9.3	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode)①	—	—	37		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 5.4A, V <sub>GS</sub> = 0V ③
t <sub>rr</sub>	Reverse Recovery Time	—	117	176	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 5.4A
Q <sub>rr</sub>	Reverse Recovery Charge	—	542	813	nC	di/dt = 100A/μs ③
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

## Thermal Resistance

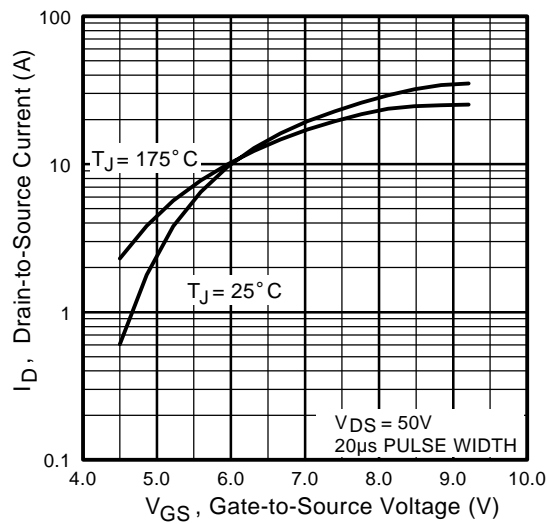
	Parameter	Typ.	Max.	Units
R <sub>θJC</sub>	Junction-to-Case	—	1.83	°C/W
R <sub>θCS</sub>	Case-to-Sink, Flat, Greased Surface ④	0.50	—	
R <sub>θJA</sub>	Junction-to-Ambient④	—	62	
R <sub>θJA</sub>	Junction-to-Ambient (PCB mount)⑤	—	40	



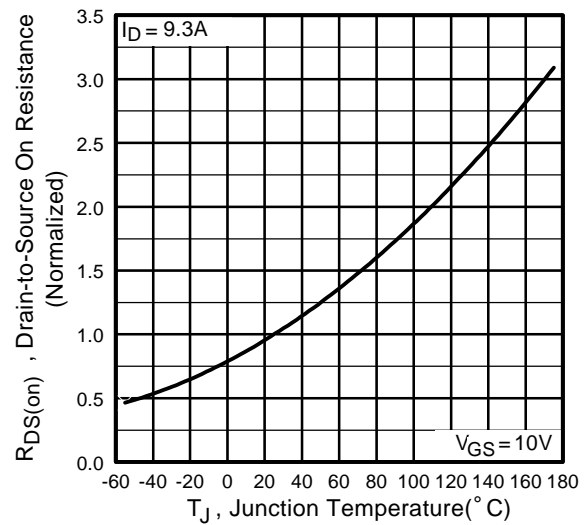
**Fig 1.** Typical Output Characteristics



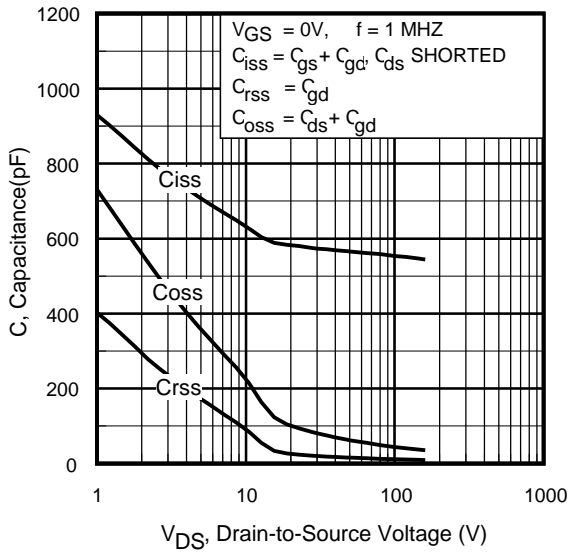
**Fig 2.** Typical Output Characteristics



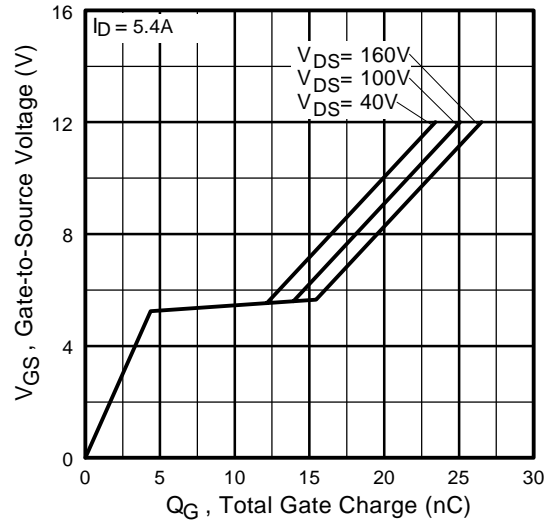
**Fig 3.** Typical Transfer Characteristics



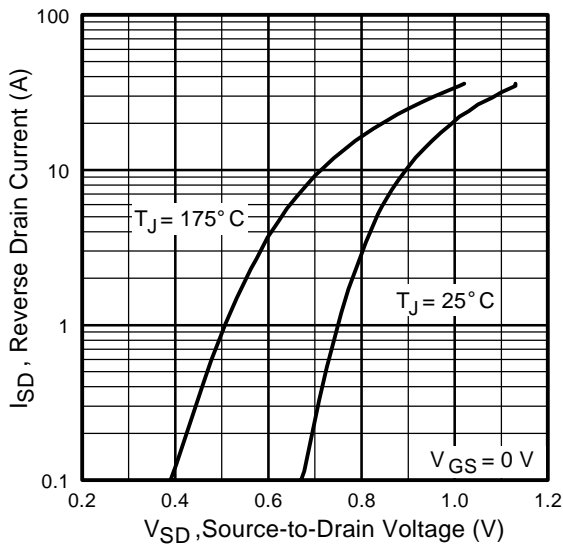
**Fig 4.** Normalized On-Resistance Vs. Temperature



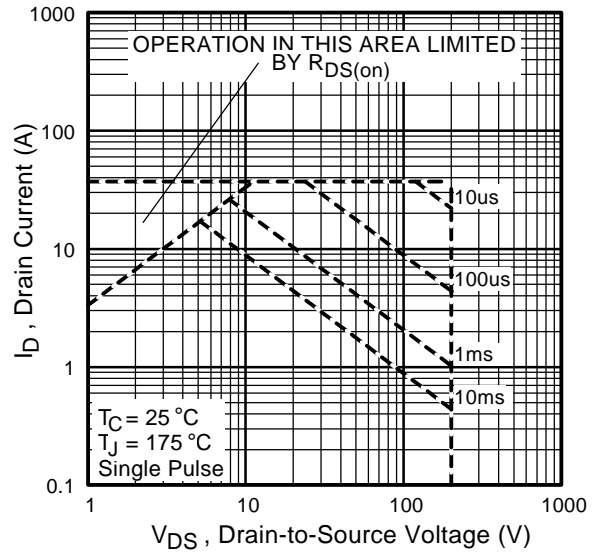
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



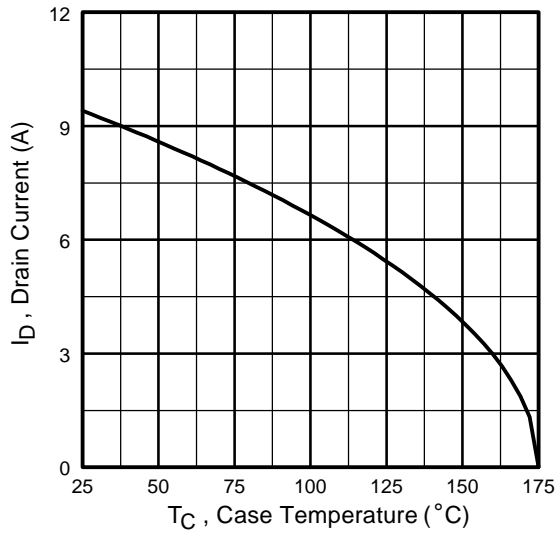
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



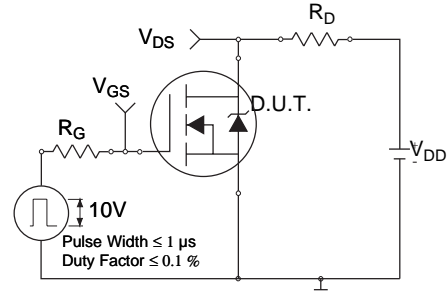
**Fig 7.** Typical Source-Drain Diode Forward Voltage



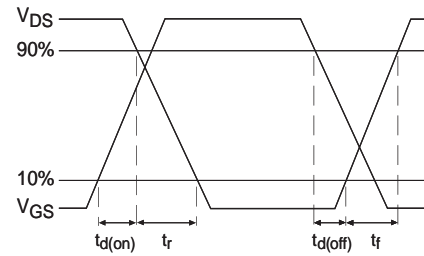
**Fig 8.** Maximum Safe Operating Area



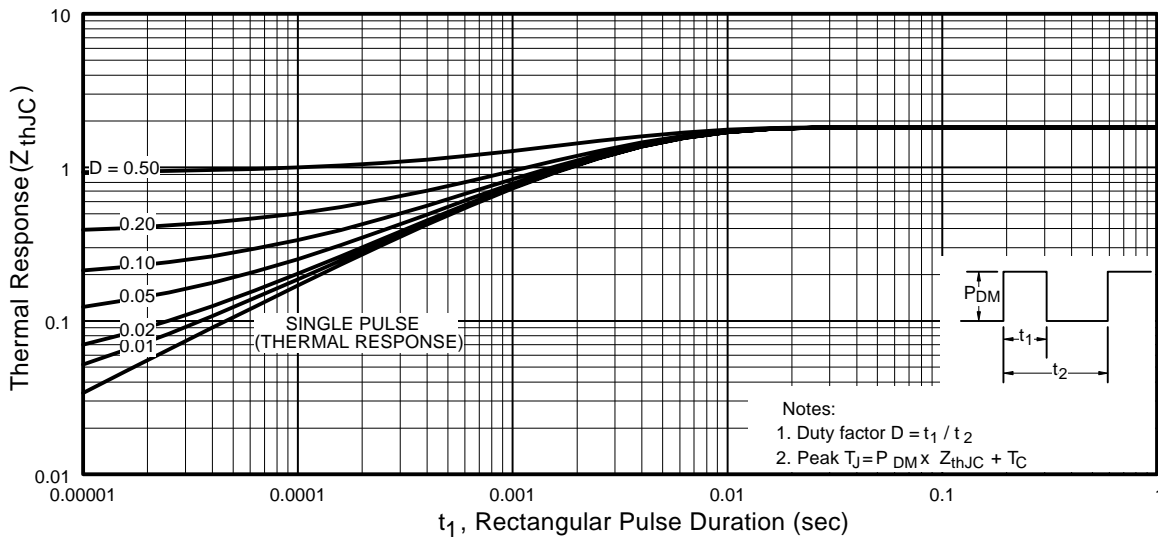
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit

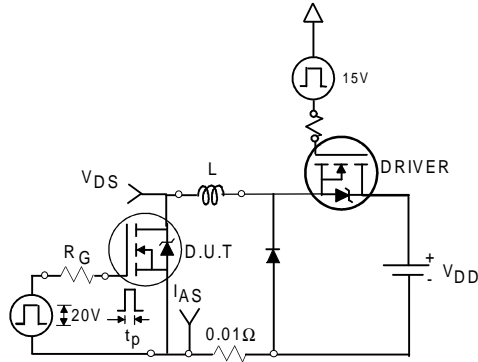


**Fig 10b.** Switching Time Waveforms

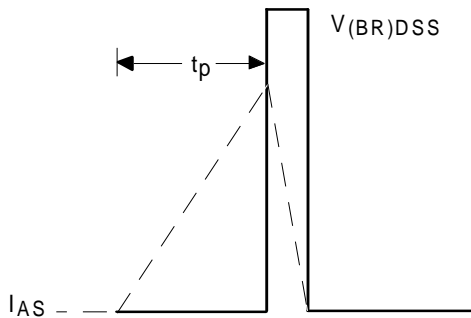


**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

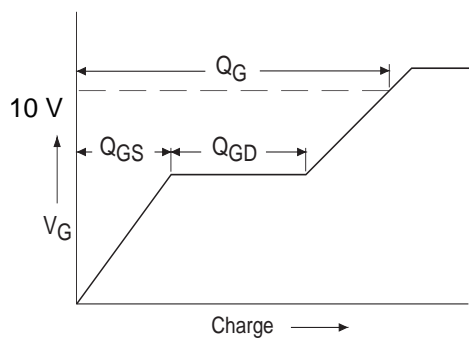
# IRF630N/S/L



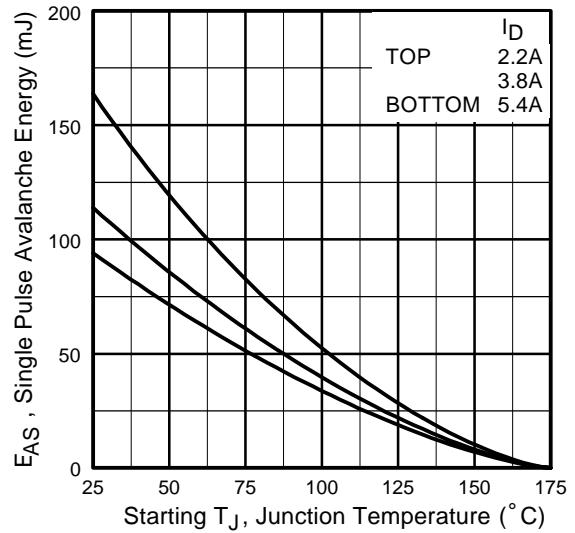
**Fig 12a.** Unclamped Inductive Test Circuit



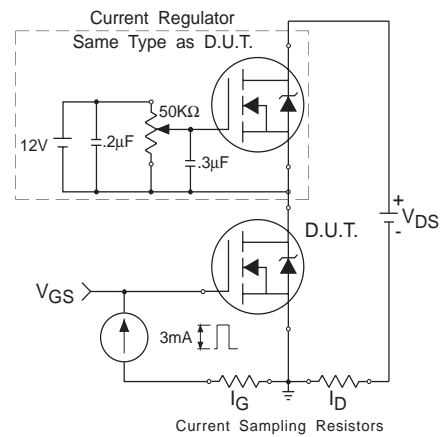
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 13a.** Basic Gate Charge Waveform

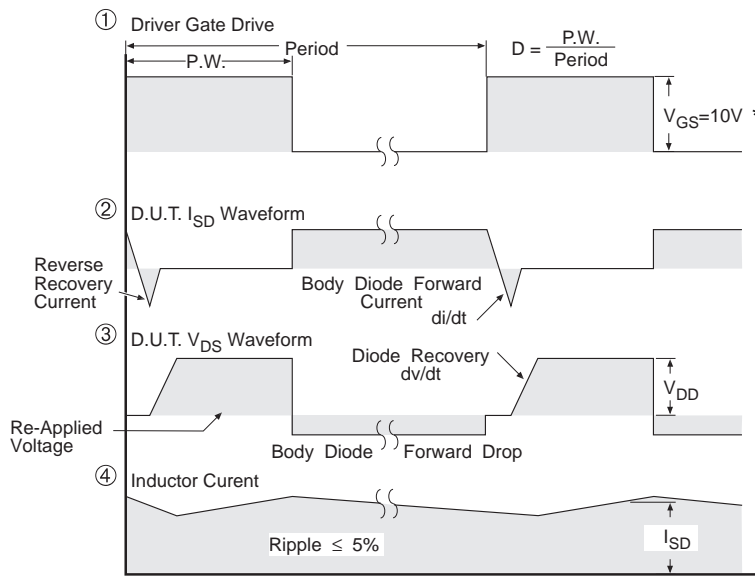
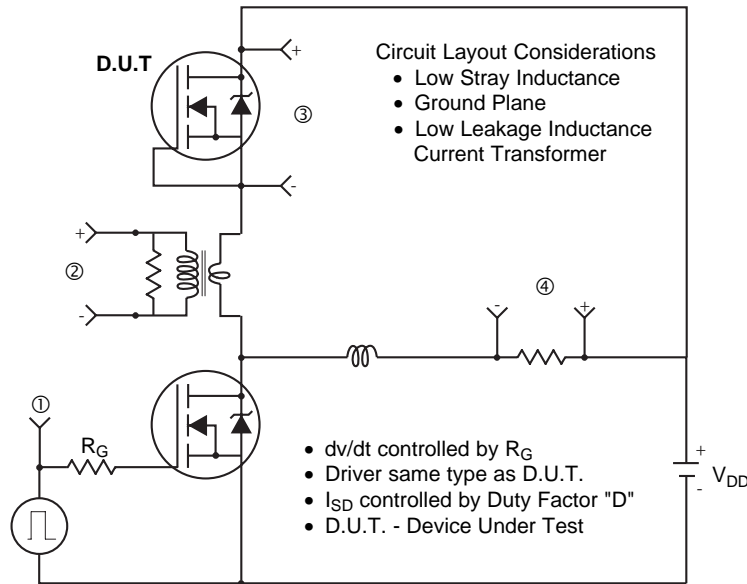


**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 13b.** Gate Charge Test Circuit

**Peak Diode Recovery dv/dt Test Circuit**



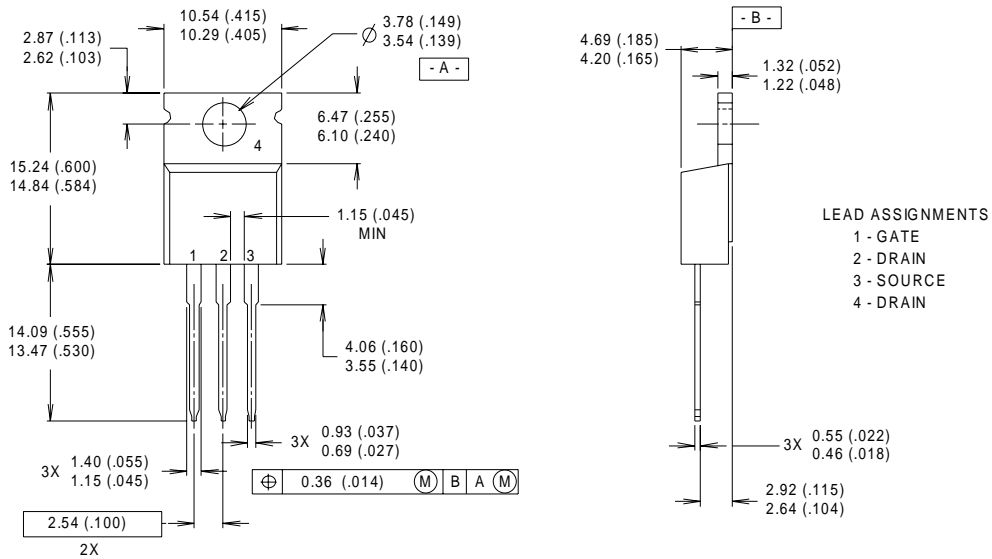
\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 14.** For N-Channel HEXFET® Power MOSFETs

# IRF630N/S/L

## TO-220AB Package Outline

Dimensions are shown in millimeters (inches)

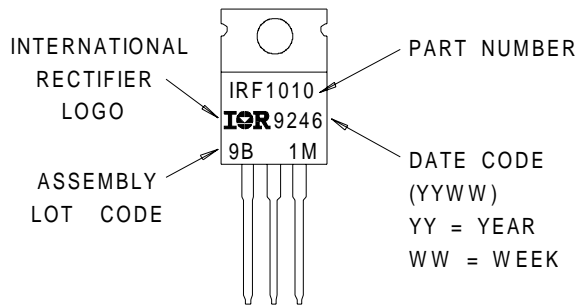


**NOTES:**

- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH
- 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
- 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

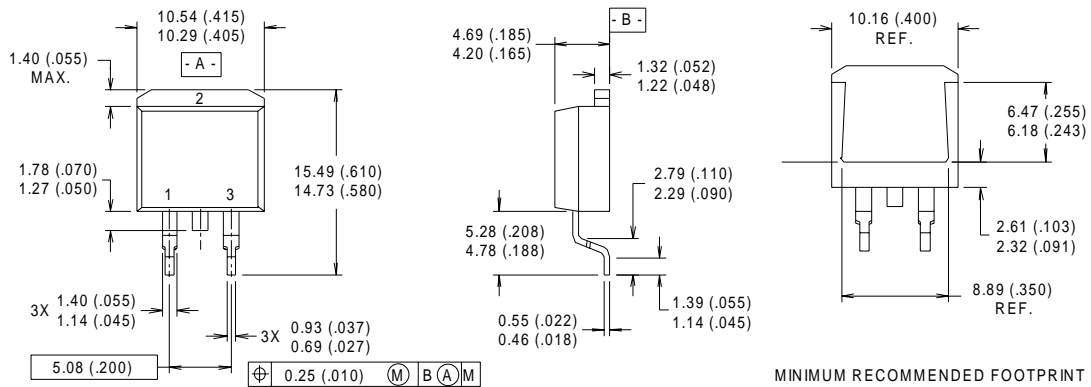
## TO-220AB Part Marking Information

EXAMPLE : THIS IS AN IRF1010  
 WITH ASSEMBLY  
 LOT CODE 9B1M





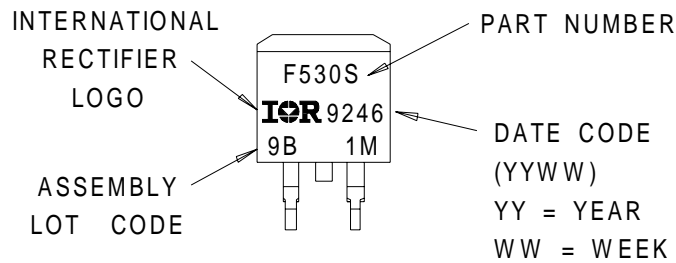
## D<sup>2</sup>Pak Package Outline



- NOTES:
- 1 DIMENSIONS AFTER SOLDER DIP.
  - 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
  - 3 CONTROLLING DIMENSION : INCH.
  - 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

- LEAD ASSIGNMENTS
- 1 - GATE
  - 2 - DRAIN
  - 3 - SOURCE

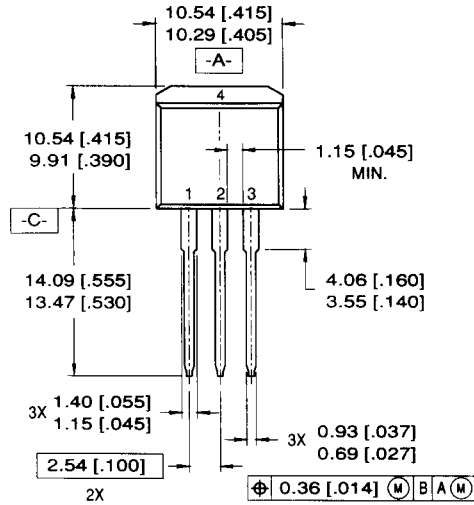
## D<sup>2</sup>Pak Part Marking Information



# IRF630N/S/L

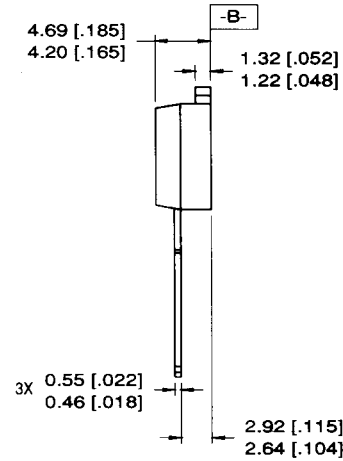


## TO-262 Package Outline



### LEAD ASSIGNMENTS

- 1 = GATE      3 = SOURCE
- 2 = DRAIN     4 = DRAIN

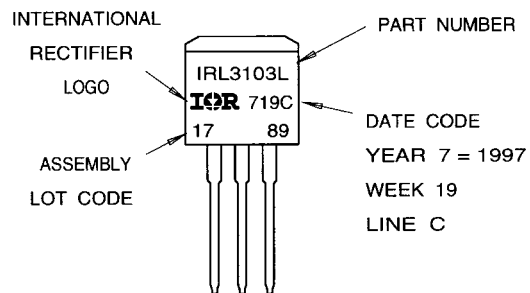


### NOTES:

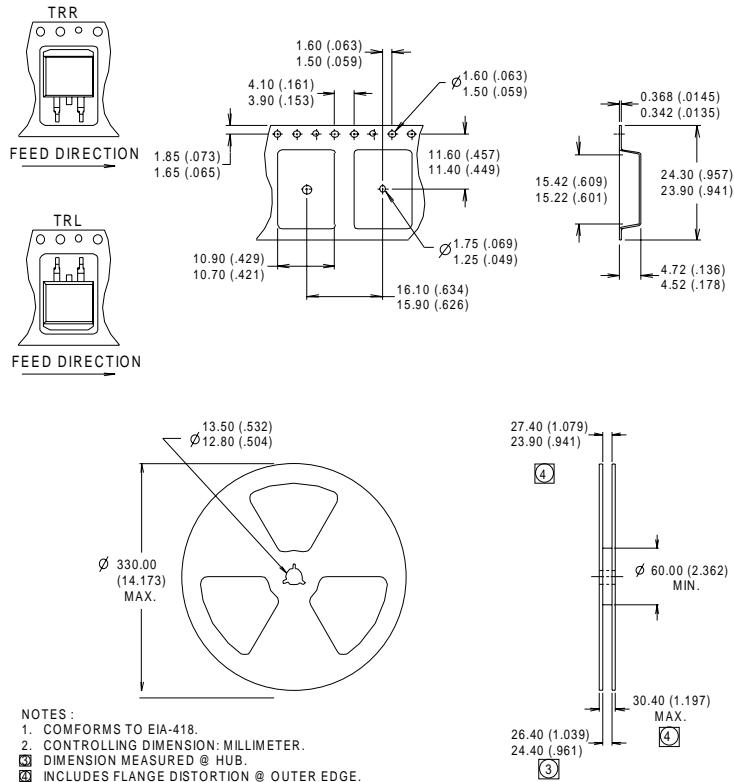
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

## TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE "C"



## D<sup>2</sup>Pak Tape & Reel Information



NOTES:  
 1. CONFORMS TO EIA-418.  
 2. CONTROLLING DIMENSION: MILLIMETER.  
 ② DIMENSION MEASURED @ HUB.  
 ③ INCLUDES FLANGE DISTORTION @ OUTER EDGE.

### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 6.5\text{mH}$   
 $R_G = 25\Omega$ ,  $I_{AS} = 5.4\text{A}$ .
- ③ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ④ This is only applied to TO-220AB package.
- ⑤ This is applied to D<sup>2</sup>Pak, when mounted on 1" square PCB ( FR-4 or G-10 Material ).  
 For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑥  $I_{SD} \leq 5.4\text{A}$ ,  $di/dt \leq 280\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 175^\circ\text{C}$ .

This datasheet has been download from:

[www.datasheetcatalog.com](http://www.datasheetcatalog.com)

Datasheets for electronics components.