

STANDARD RED SCF5740 HIGH EFFICIENCY RED SCF5742 HIGH EFFICIENCY GREEN SCF5744

0.270" 4-Character 5x7 Dot Matrix Serial Input Dot Addressable Intelligent Display[®] Devices



TANNA

FEATURES

- Four 0.270" (6.85 mm) 5x7 Dot Matrix Characters in Red, High Efficiency Red, High Efficiency Green
- Optimum Display Surface Efficiency (display area to package ratio)
- High Speed Data Input Rate: 5.0 MHz
- ROMIess Serial Input, Dot Addressable Display Ideal for User Defined Characters
- Built-in Decoders, Multiplexers and LED Drivers
- Readable from 6 Feet (1.8 meters)
- Wide Viewing Angle, X Axis ±55°, Y Axis ±55°
- Attributes:
 - 140 Bit RAM for User Defined Characters
 - Eight Dimming Levels
 - Power Down Model (<250 μW)
 - Hardware/Software Clear Functions
 - Internal or External Clock

DESCRIPTION

The SCF574X is a four digit, dot addressable 5x7 dot matrix, serial input, alphanumeric Intelligent Display device. The four digits are packaged in a rugged, high quality, optically transparent, plastic 22 pin DIP with 0.1" pin spacing.

The on-board CMOS has a 140 bit RAM, one bit associated with one LED, each to generate User Defined Characters. In Power Down Mode, quiescent current is <50 μ A.

The SCF574X is designed for work with the serial port of most common microprocessors. Data is transferred into the display through the Serial Data Input (DATA), clocked by the Serial Data Clock (SDCLK), and enabled by the Load Input (LOAD).

The Clock I/O (CLK I/O) and Clock Select (CLK SEL) pins offer the user the capability to supply a high speed external multiplex clock. This feature can minimize audio in-band interference for portable communication equipment or eliminate the visual sychronization effects found in high vibration environments such as avionic equipment.

Maximum Ratings

DC Supply Voltage	0.5 to +7.0 Vdc
Input Voltage Levels Relative	
to Ground–0	.5 to V _{CC} +0.5 Vdc
Operating Temperature	
Storage Temperature	
Maximum Solder Temperature 0.063"	
below Seating Plane, t<5 s	
Relative Humidity at 85°C	
Maximum Number of LEDs at 100% Brightn	ess 64
Maximum Power Dissipation	0.65 W
ESD (100 pF, 1.5 kW)	
Maximum Input Current	

Figure 1. Timing Diagram—Data Write Cycle



Figure 2. Timing Diagram—Instruction Cycle



Optical Characteristics at 25°C

 $(V_{CC}=5.0 \text{ V at } 100\% \text{ brightness level, viewing angle: X axis } \pm 55^{\circ}, \text{ Y axis } \pm 65^{\circ})$

Red SCF5740

Description	Symbol	Min.	Тур.	Units
Luminous Intensity	I _V	55	—	µcd/dot
Peak Wavelength	λ(peak)	—	655	nm
Dominant Wavelength	λ(d)		639	nm

High Efficiency Red SCF5742

Description	Symbol	Min.	Тур.	Units
Luminous Intensity	IV	110	—	µcd/dot
Peak Wavelength	λ(peak)	—	630	nm
Dominant Wavelength	λ(d)		626	nm

High Efficiency Green SCF5744

Description	Symbol	Min.	Тур.	Units
Luminous Intensity	I _V	110	—	µcd/dot
Peak Wavelength	λ(peak)	—	568	nm
Dominant Wavelength	λ(d)		574	nm

Notes:

1. Dot to dot intensity matching at 100% brightness is 1.8:1.

2. Displays within a given intensity category have an intensity matching of 1.5:1 (max.)

Switching Specifications

(over operating temperature range and V_{CC} =4.5 V to 5.5 V)

Symbol	Description	Min.	Units
T _{RC}	Reset Active Time	600	ns
T _{LDS}	Load Setup Time	50	ns
T _{DS}	Data Setup Time	50	ns
T _{SDCLK}	Clock Period	200	ns
T _{SDCW}	Clock Width	70	ns
T _{LDH}	Load Hold Time	0	ns
T _{DH}	Data Hold Time	25	ns
T _{WR}	Total Write Time	2.2	μs
T _{BL}	Time Between Loads	600	ns

Note:

 $T_{\rm SDCW}$ is the minimum time the SDCLK may be low or high. The SDCLK period must be a minimum of 200 ns.

Electrical Characteristics (over operating temperature)

Parameter	Min.	Тур.	Max.	Units	Conditions
V _{CC}	4.5	5.0	5.5	V	-
I _{CC} (PWR DWN)(4)	_	_	50	μA	$V_{\rm CC}$ =5.0 V, all inputs=0 V or $V_{\rm CC}$
I _{CC} 4 digits 20 dots/character	—	150	186	mA	V _{CC} =5.0 V, "#" displayed in all 4 digits at 100% brightness at 25°C
I _{IL} Input current	_	_	-10	μA	V _{CC} =5.0 V, V _{IN} =0 (all inputs)
I _{IH} Input current	_	—	10	μA	$V_{\rm CC} = V_{\rm IN} = 5.0 \text{ V} \text{ (all inputs)}$
V _{IH}	3.5	—	_	V	V _{CC} =4.5 V to 5.5 V
V _{IL}	_	—	1.5	V	V _{CC} =4.5 V to 5.5 V
I _{OH} (CLK I/O)	_	-28	_	mA	V _{CC} =4.5 V, V _{OH} =2.4 V
I _{OL} (CLK I/O)	_	23	—	mA	V _{CC} =4.5 V, V _{OL} =0.4 V
θ_{JC} -pin	_	—	32	°C/W	_
Fext External Clock Input Frequency	120	—	347	KHz	V _{CC} =5.0 V, CLKSEL=0
Fosc Internal Clock Input Frequency	120	—	347	KHz	V _{CC} =5.0 V, CLKSEL=1
Clock I/O Bus Loading		-	240	pF	-
Clock Out Rise Time		-	500	ns	V _{CC} =4.5 V, V _{OH} =2.4 V
Clock Out Fall Time		-	500	ns	V _{CC} =4.5 V, V _{OH} =0.4 V
FM, Digit	375	768	1086	Hz	_

Notes:

Peak current ⁵/₃ × I_{CC}.
 Unused inputs must be tied high.

3) Contact Infineon for 3.3 volt operation.

4) External oscillator must be stopped if being used to maintain an I_{CC} <50 μ A.

Input/Output Circuits

Figures 3 and 4 show the input and output resistor/diode networks used for ESD protection and to eliminate substrate latch-up caused by input voltage over/under shoot.

Figure 3. Inputs



Figure 4. Clock I/O



Figure 5. Top View

22	Pin	S	12
Digit 0	Digit 1	Digit 2	Digit 3
1	Pin	S	11

Pin Assignment

Pin	Function	Pin	Function
1	N/C	22	N/C
2	GND	21	CLKSEL
3	N/C	20	CLK I/O
4	N/C	19	RST
5	N/C	18	N/C
6	N/C	17	N/C
7	N/C	16	N/C
8	N/C	15	SCLK
9	V _{LL}	14	DATA
10	V _{CC}	13	LOAD
11	N/C	12	N/C

Figure 6. Dot Matrix Format



Pin Definitions

1 N/C 2 GND Power supply ground 3 N/C 4 N/C 5 N/C 6 N/C 7 N/C 8 N/C 9 V _{LL} LED supply 10 V _{CC} Logic supply 11 N/C 12 N/C 13 LOAD Low input enables data clocking into 8-bit serial shift register. When load goes high, the contents of 8-bit serial shift register will be decoded. 14 DATA Serial data input 15 SDCLK For loading data into the 8-bit serial data register 16 N/C 17 N/C 18 N/C 19 RST Asynchronous input, when low clears the multiplex counter, address register, control word register. Control word register is set to 100% brightness. The display will be blank. 20 CLK I/O Outputs Master Clock or inputs External Clock 21 CLKSEL High=Internal Clock (Master) Lo	Pin	Function	Definitions
3 N/C 4 N/C 5 N/C 6 N/C 7 N/C 8 N/C 9 V _{LL} LED supply 10 V _{CC} Logic supply 11 N/C 12 N/C 13 LOAD Low input enables data clocking into 8-bit serial shift register. When load goes high, the contents of 8-bit serial shift register will be decoded. 14 DATA Serial data input 15 SDCLK For loading data into the 8-bit serial data register 16 N/C 17 N/C 18 N/C 19 RST Asynchronous input, when low clears the multiplex counter, address register, control word register. Set to 100% brightness. The display will be blank. 20 CLK I/O Outputs Master Clock or inputs External Clock 21 CLKSEL High=Internal Clock (Slave)	1	N/C	—
4N/C5N/C6N/C7N/C8N/C9V _{LL} LED supply10V _{CC} Logic supply11N/C12N/C13LOADLow input enables data clocking into 8-bit serial shift register. When load goes high, the contents of 8-bit serial shift register will be decoded.14DATASerial data input15SDCLKFor loading data into the 8-bit serial data register16N/C17N/C18N/C19RSTAsynchronous input, when low clears the multiplex counter, address register, control word register. Control word register, user RAM and data register. Control word register.	2	GND	Power supply ground
5 N/C 6 N/C 7 N/C 8 N/C 9 V _{LL} LED supply 10 V _{CC} Logic supply 11 N/C 12 N/C 13 LOAD Low input enables data clocking into 8-bit serial shift register. When load goes high, the contents of 8-bit serial shift register will be decoded. 14 DATA Serial data input 15 SDCLK For loading data into the 8-bit serial data register 16 N/C 17 N/C 18 N/C 19 RST Asynchronous input, when low clears the multiplex counter, address register, control word register, control word register, user RAM and data register. Control word register. Control word register. Control word register. Set to 100% brightness. The display will be blank. 20 CLK I/O Outputs Master Clock or inputs External Clock (Slave) 21 CLKSEL High=Internal Clock (Slave)	3	N/C	—
6 N/C 7 N/C 8 N/C 9 V _{LL} LED supply 10 V _{CC} Logic supply 11 N/C 12 N/C 13 LOAD Low input enables data clocking into 8-bit serial shift register. When load goes high, the contents of 8-bit serial shift register will be decoded. 14 DATA Serial data input 15 SDCLK For loading data into the 8-bit serial data register 16 N/C 17 N/C 18 N/C 19 RST Asynchronous input, when low clears the multiplex counter, address register, control word register. Control word register. Control word register. Set to 100% brightness. The display will be blank. 20 CLK I/O Outputs Master Clock or inputs External Clock 21 CLKSEL High=Internal Clock (Slave)	4	N/C	
7 N/C 8 N/C 9 V _{LL} LED supply 10 V _{CC} Logic supply 11 N/C 12 N/C 13 LOAD Low input enables data clocking into 8-bit serial shift register. When load goes high, the contents of 8-bit serial shift register will be decoded. 14 DATA Serial data input 15 SDCLK For loading data into the 8-bit serial data register 16 N/C 17 N/C 18 N/C 19 RST Asynchronous input, when low clears the multiplex counter, address register, user RAM and data register. Control word register. Set to 100% brightness. The display will be blank. 20 CLK I/O Outputs Master Clock or inputs External Clock 21 CLKSEL High=Internal Clock (Slave)	5	N/C	—
8 N/C 9 V _{LL} LED supply 10 V _{CC} Logic supply 11 N/C 12 N/C 13 LOAD Low input enables data clocking into 8-bit serial shift register. When load goes high, the contents of 8-bit serial shift register will be decoded. 14 DATA Serial data input 15 SDCLK For loading data into the 8-bit serial data register 16 N/C 17 N/C 18 N/C 19 RST Asynchronous input, when low clears the multiplex counter, address register, control word register, user RAM and data register. Control word register, user RAM and data register. Control word register, user RAM and data register. Control word register is set to 100% brightness. The display will be blank. 20 CLK I/O Outputs Master Clock or inputs External Clock 21 CLKSEL High=Internal Clock (Master) Low=External Clock (Slave)	6	N/C	—
9 V_{LL} LED supply10 V_{CC} Logic supply11N/C—12N/C—13LOADLow input enables data clocking into 8-bit serial shift register. When load goes high, the con- tents of 8-bit serial shift register will be decoded.14DATASerial data input15SDCLKFor loading data into the 8-bit serial data register16N/C—17N/C—18N/C—19RSTAsynchronous input, when low clears the multiplex counter, address register, control word reg- ister, user RAM and data register. Control word register is set to 100% brightness. The display will be blank.20CLK I/OOutputs Master Clock or inputs External Clock21CLKSELHigh=Internal Clock (Master) Low=External Clock (Slave)	7	N/C	—
10 V_{CC} Logic supply11N/C—12N/C—13LOADLow input enables data clocking into 8-bit serial shift register. When load goes high, the con- tents of 8-bit serial shift register will be decoded.14DATASerial data input15SDCLKFor loading data into the 8-bit serial data register16N/C—17N/C—18N/C—19RSTAsynchronous input, when low clears the multiplex counter, address register, control word reg- ister, user RAM and data register. Control word register is set to 100% brightness. The display will be blank.20CLK I/OOutputs Master Clock or inputs External Clock21CLKSELHigh=Internal Clock (Master) Low=External Clock (Slave)	8	N/C	—
11N/C—12N/C—13LOADLow input enables data clocking into 8-bit serial shift register. When load goes high, the con- tents of 8-bit serial shift register will be decoded.14DATASerial data input15SDCLKFor loading data into the 8-bit serial data register16N/C—17N/C—18N/C—19RSTAsynchronous input, when low clears the multiplex counter, address register, control word reg- ister, user RAM and data register. Control word register is set to 100% brightness. The display will be blank.20CLK I/OOutputs Master Clock or inputs External Clock21CLKSELHigh=Internal Clock (Master) Low=External Clock (Slave)	9	V _{LL}	LED supply
12N/C—13LOADLow input enables data clocking into 8-bit serial shift register. When load goes high, the con- tents of 8-bit serial shift register will be decoded.14DATASerial data input15SDCLKFor loading data into the 8-bit serial data register16N/C—17N/C—18N/C—19RSTAsynchronous input, when low clears the multiplex counter, address register, control word reg- ister, user RAM and data register. Control word register is set to 100% brightness. The display will be blank.20CLK I/OOutputs Master Clock or inputs External Clock21CLKSELHigh=Internal Clock (Master) Low=External Clock (Slave)	10	V _{CC}	Logic supply
13LOADLow input enables data clocking into 8-bit serial shift register. When load goes high, the con- tents of 8-bit serial shift register will be decoded.14DATASerial data input15SDCLKFor loading data into the 8-bit serial data register16N/C17N/C18N/C19RSTAsynchronous input, when low clears the multiplex counter, address register, control word reg- ister, user RAM and data register. Control word register is set to 100% brightness. The display will be blank.20CLK I/OOutputs Master Clock or inputs External Clock21CLKSELHigh=Internal Clock (Master) Low=External Clock (Slave)	11	N/C	—
into 8-bit serial shift register. When load goes high, the con- tents of 8-bit serial shift register will be decoded.14DATASerial data input15SDCLKFor loading data into the 8-bit serial data register16N/C—17N/C—18N/C—19RSTAsynchronous input, when low clears the multiplex counter, address register, control word reg- ister, user RAM and data register. Control word register is set to 100% brightness. The display will be blank.20CLK I/OOutputs Master Clock or inputs External Clock21CLKSELHigh=Internal Clock (Master) Low=External Clock (Slave)	12	N/C	—
15SDCLKFor loading data into the 8-bit serial data register16N/C—17N/C—18N/C—19RSTAsynchronous input, when low clears the multiplex counter, address register, control word reg- ister, user RAM and data register. Control word register is set to 100% brightness. The display will be blank.20CLK I/OOutputs Master Clock or inputs External Clock21CLKSELHigh=Internal Clock (Master) Low=External Clock (Slave)	13	LOAD	into 8-bit serial shift register. When load goes high, the con- tents of 8-bit serial shift register
16 N/C 17 N/C 18 N/C 19 RST Asynchronous input, when low clears the multiplex counter, address register, control word register, user RAM and data register. Control word register is set to 100% brightness. The display will be blank. 20 CLK I/O Outputs Master Clock or inputs External Clock 21 CLKSEL High=Internal Clock (Master) Low=External Clock (Slave)	14	DATA	Serial data input
17 N/C — 18 N/C — 19 RST Asynchronous input, when low clears the multiplex counter, address register, control word register, user RAM and data register. Control word register is set to 100% brightness. The display will be blank. 20 CLK I/O Outputs Master Clock or inputs External Clock 21 CLKSEL High=Internal Clock (Master) Low=External Clock (Slave)	15	SDCLK	
18 N/C — 19 RST Asynchronous input, when low clears the multiplex counter, address register, control word register, user RAM and data register. Control word register is set to 100% brightness. The display will be blank. 20 CLK I/O Outputs Master Clock or inputs External Clock 21 CLKSEL High=Internal Clock (Master) Low=External Clock (Slave)	16	N/C	—
19RSTAsynchronous input, when low clears the multiplex counter, address register, control word reg- ister, user RAM and data register. Control word register is set to 100% brightness. The display will be blank.20CLK I/OOutputs Master Clock or inputs 	17	N/C	
clears the multiplex counter, address register, control word reg- ister, user RAM and data register. Control word register is set to 100% brightness. The display will be blank.20CLK I/OOutputs Master Clock or inputs External Clock21CLKSELHigh=Internal Clock (Master) Low=External Clock (Slave)	18	N/C	—
21 CLKSEL High=Internal Clock (Master) Low=External Clock (Slave)	19	RST	clears the multiplex counter, address register, control word reg- ister, user RAM and data register. Control word register is set to 100% brightness. The display will
Low=External Clock (Slave)	20	CLK I/O	
22 N/C	21	CLKSEL	
	22	N/C	

Display Column and Row Format

	C0	C1	C2	С3	C4
Row 0	1	1	1	1	1
Row 1	0	0	1	0	0
Row 2	0	0	1	0	0
Row 3	0	0	1	0	0
Row 4	0	0	1	0	0
Row 5	0	0	1	0	0
Row 6	0	0	1	0	0

1=Display dot "On" 0=Display dot "Off'

Column Data Ranges

Row 0	00H to 1FH
Row 1	00H to LFH
Row 2	00H to LFH
Row 3	00H to LFH
Row 4	00H to LFH
Row 5	00H to LFH
Row 6	00H to LFH

Figure 7. Block Diagram

Operation of the SCF574X

The SCF574X display consists of a CMOS IC containing control logic and drivers for four 5x7 characters. These components are assembled in a compact plastic package.

Individual LED dot addressability allows the user great freedom in creating special characters or mini-icons.

The serial data interface provides a highly efficient interconnection between the display and the mother board. The SCF574X requires only three lines as compared to 14 for an equivalent four character parallel input part.

The on-board CMOS IC is the electronic heart of the display. The IC accepts decoded serial data, which is stored in the internal RAM. Asynchronously the RAM is read by the character multiplexer at a strobe rate that results in a flicker free display. Figure 7 shows the three functional areas of the IC. These include: the input serial data register and control logic, a 140 bits two port RAM, and an internal multiplexer/display driver.



The following explains how to format the serial data to be loaded into the display. The user supplies a string of bit mapped decoded characters. The contents of this string is shown in Figure 8a. Figure 8b shows that each character consist of eight 8 bit words. The first word encodes the display character location and the succeeding seven bytes are row data. The row data represents the status (On, Off) of individual column LEDs. Figure 8c shows that each 8 bit word is formatted to represent Character Address, or Column Data.

Figure 8d shows the sequence for loading the bytes of data. Bringing the LOAD line low enables the serial register to accept data. The shift action occurs on the low to high transition of the serial data clock (SDCLK). The least significant bit (D0) is loaded first. After eight clock pulses the LOAD line is brought high. With this transition the OPCODE is decoded. The decoded OPCODE directs D4–D0 to be latched in the Character Address register, stored in the RAM as Column data, or latched in the Control Word register. The control IC requires a minimum 600 ns delay between successive byte loads. As indicated in Figure 8a, a total of 256 bits of data are required to load all four characters into the display.

The Character Address Register bits, D4–D0 (Table 2), and Row Address Register bits, D7–D5 (Table 3), direct the Column Data bits, D4–D0 (Table 3) to specific RAM location.

Table 1 shows the Row Address for the example character "D." Column data is written and read asynchronously from the 140 bit RAM. Once loaded the internal oscillator and character multiplexer reads the data from the RAM. These characters are row strobed with column data as shown in Figures 9 and 10. The character strobe rate is determined by the internal or user supplied external MUX Clock and the IC's \div 320 counter.

Table	1.	Character	"D"
-------	----	-----------	-----

	-	code D6		D4	umn D3	D2	D1		Hex
				C0	C1	C2	C3	C4	
Row 0	0	0	0	1	1	1	1	0	1E
Row 1	0	0	0	1	0	0	0	1	11
Row 2	0	0	0	1	0	0	0	1	11
Row 3	0	0	0	1	0	0	0	1	11
Row 4	0	0	0	1	0	0	0	1	11
Row 5	0	0	0	1	0	0	0	1	11
Row 6	0	0	0	1	1	1	1	0	1E

Figure 8. Loading Serial Character Data



Table 2. Load Character Address

Op D7	code D6	e D5	Cha D4		er A D2			Hex	Operation Load
1	0	1	0	0	0	0	0	A0	Character 0
1	0	1	0	0	0	0	1	A1	Character 1
1	0	1	0	0	0	1	0	A2	Character 2
1	0	1	0	0	0	1	1	A3	Character 3

Table 3. Load Column Data

	Op code D7 D6 D5			umn D3			D0	Operation Load
0	0	0	CO	C1	C2	СЗ	C4	Row 0
0	0	0	CO	C1	C2	СЗ	C4	Row 1
0	0	0	C0	C1	C2	C3	C4	Row 2
0	0	0	C0	C1	C2	C3	C4	Row 3
0	0	0	C0	C1	C2	СЗ	C4	Row 4
0	0	0	C0	C1	C2	C3	C4	Row 5
0	0	0	C0	C1	C2	СЗ	C4	Row 6

The user can activate four Control functions. These include: LED Brightness Level, IC Power Down, Prescaler, or Display Clear. OPCODEs and six bit words are used to initiate these functions. The OPCODEs and Control Words for the Character Address and Loading Column Data are shown in Tables 2 and 3.

The user can select eight specific LED brightness levels, Tables 4 and 5. Depending on how D3 is selected either one (1) for maximum peak current or zero (0) for 12.5% of maximum peak current in the control word per Tables 4 and 5, the user can select 16 specific LED brightness levels. These brightness levels (in percentages of full brightness of the display) depending on how the user selects D3 can be one (1) or zero (0) are as follows: 100% (E0_{HEX} or E8_{HEX}), 53% (E1_{HEX} or E9_{HEX}), 40% (E2_{HEX} or EA_{HEX}), 27% (E3_{HEX} or EB_{HEX}), 20% (E4_{HEX} or EC_{HEX}), 13% (E5_{HEX} or ED_{HEX}), and 6.6% (E6_{HEX} or EE_{HEX}), 0.0% (E7_{HEX} or EF_{HEX}). The brightness levels are controlled by changing the duty factor of the row strobe pulse.

The SCF574X offers a unique Display Power Down feature which reduces I_{CC} to less than 50 µA. When EF_{HEX} is loaded (Table 6) the display is set to 0% brightness. When in the Power Down mode data may still be written into the RAM. The display is reactivated by loading a new brightness Level Control Word into the display.

Table 4. Display Brightness

		•	· ·	•					
Op D7	code D6	e D5			Wor D2		D0	Hex	Operation Level
1	1	1	0	0	0	0	0	E0	100%
1	1	1	0	0	0	0	1	E1	53%
1	1	1	0	0	0	1	0	E2	40%
1	1	1	0	0	0	1	1	E3	27%
1	1	1	0	0	1	0	0	E4	20%
1	1	1	0	0	1	0	1	E5	13%
1	1	1	0	0	1	1	0	E6	6.6%
1	1	1	0	0	1	1	1	E7	0.0%

Table 5. Display Brightness

	cod D6	e D5		ntrol D3			D0	Hex	Operation Level
1	1	1	0	1	0	0	0	E8	100%
1	1	1	0	1	0	0	1	E9	53%
1	1	1	0	1	0	1	0	EA	40%
1	1	1	0	1	0	1	1	EB	27%
1	1	1	0	1	1	0	0	EC	20%
1	1	1	0	1	1	0	1	ED	13%
1	1	1	0	1	1	1	0	EE	6.6%
1	1	1	0	1	1	1	1	EF	0.0%

Table 6. Power Down

	code D6			Control Word D4 D3 D2 D1 D0					Operation Level
1	1	1	0	1	1	1	1	EF	0% brightness

Figure 9. Row and Column Locations for a Character "D"



Figure 10. Row Strobing



The SCF574X allows a high frequency external oscillator source to drive the display. Data bit, D4, in the control word format controls the prescaler function. The prescaler allows the oscillator source to be divided by 16 by setting D4=1. However, the prescaler should not be used, i.e., when using the internal oscillator source.

The Software Clear ($C0_{HEX}$), given in Table 7, clears the Address Register and the RAM. The display is blanked and the Character Address Register will be set to Character 0. The internal counter and the Control Word Register are unaffected. The Software Clear will remain active until the next data input cycle is initiated.

Table 7. Software Clear

Op code Control Word								Hex	Operation
D7	D6	D5	D4	D3	D2	D1	D0		
1	1	0	0	0	0	0	0	C0	CLEAR

Multiplexer and Display Driver

The four characters are row multiplexed with RAM resident column data. The strobe rate is established by the internal or external MUX Clock rate. The MUX Clock frequency is divided by a 448 counter chain. This results in a typical strobe rate of 768 Hz. By pulling the Clock SEL line low, the display can be operated from an external MUX Clock. The external clock is attached to the CLK I/O connection (pin 9). The maximum external MUX Clock frequency should be limited to 1.0 MHz.

An asynchronous hardware Reset Pin is also provided. Bringing this pin low will clear the Character Address Register, Control Word Register, RAM, and blanks the display. This action leaves the display set at Character Address 0, and the Brightness Level set at 100%.

Electrical and Mechanical Considerations Thermal Considerations

Optimum product performance can be had when the following electrical and mechanical recommendations are adopted. The SCF574X's IC is constructed in a high speed CMOS process, consequently high speed noise on the SERIAL DATA, SERIAL DATA CLOCK, LOAD and RESET lines may cause incorrect data to be written into the serial shift register. Adhere to transmission line termination procedures when using fast line drivers and long cables (>10 cm).

Good ground (pin 2) and power supply decoupling (pins 9 and 10) will insure that I_{CC} (<400 mA peak) switching currents do not generate localized ground bounce. Therefore it is recommended that each display package use a 0.1 μ F and 20 μ F capacitor between V_{CC} and ground.

When the internal MUX Clock is being used connect the CLKSEL pin to V_{CC} . In those applications where RESET will not be connected to the system's reset control, it is recommended that this pin be connected to the center node of a series 0.1, μ F and 100 k Ω RC network. Thus upon initial power up the RESET will be held low for 10 ms allowing adequate time for the system power supply to stabilize.

ESD Protection

The input protection structure of the SCF574X provides significant protection against ESD damage. It is capable of withstanding discharges greater than 2.0 kV. Take all the standard precautions, normal for CMOS components. These include properly grounding personnel, tools, tables, and transport carriers that come in contact with unshielded parts. If these conditions are not, or cannot be met, keep the leads of the device shorted together or the parts in anti-static packaging.

Soldering Considerations

The SCF574X can be hand soldered with SN63 solder using a grounded iron set to 260°C.

Wave soldering is also possible following these conditions: Preheat that does not exceed 93°C on the solder side of the PC board or a package surface temperature of 85°C. Water soluble organic acid flux (except carboxylic acid) or rosin-based RMA flux without alcohol can be used.

Wave temperature of $245^{\circ}C \pm 5^{\circ}C$ with a dwell between 1.5 sec. to 3.0 sec. Exposure to the wave should not exceed temperatures above 260°C for five seconds at 0.063" below the seating plane. The packages should not be immersed in the wave.

Post Solder Cleaning Procedures

The least offensive cleaning solution is hot D.I. water (60°C) for less than 15 minutes. Addition of mild saponifiers is acceptable. Do not use commercial dishwasher detergents.

For faster cleaning, solvents may be used. Exercise care in choosing solvents as some may chemically attack the nylon package. For further information refer to Appnotes 18 and 19.

An alternative to soldering and cleaning the display modules is to use sockets. Naturally, 14 pin DIP sockets .300" wide with .100" centers work well for single displays. Multiple display assemblies are best handled by longer SIP sockets or DIP sockets when available for uniform package alignment. Socket manufacturers are Aries Electronics, Inc., Frenchtown, NJ; Garry Manufacturing, New Brunswick, NJ; Robinson-Nugent, New Albany, IN; and Samtec Electronic Hardward, New Albany, IN.

For further information refer to Appnote 22.

Optical Considerations

The 0.270" high character of the SCF574X gives readability up to five feet. Proper filter selection enhances readability over this distance.

Using filters emphasizes the contrast ratio between a lit LED and the character background. This will increase the discrimination of different characters. The only limitation is cost. Take into consideration the ambient lighting environment for the best cost/benefit ratio for filters.

Incandescent (with almost no green) or fluorescent (with almost no red) lights do not have the flat spectral response of sunlight. Plastic band-pass filters are an inexpensive and effective way to strengthen contrast ratios. The SCF5740 is a red display and should be used with long wavelength pass filter having a sharp cut-off in the 600 nm to 620 nm range. The SCF5742 is a high efficiency red display and should be used with long wavelength pass filter having a sharp cut-off in the 570 nm to 600 nm range. The SCF5744 is a high efficiency green display and should be used with long wavelength pass filter that peaks at 565 nm.

Figure 11. Display Interface to Siemens/Intel 8031 Microprocessor (using serial port in mode 0)

Additional contrast enhancement is gained by shading the displays. Plastic band-pass filters with built-in louvers offer the next step up in contrast improvement. Plastic filters can be improved further with anti-reflective coatings to reduce glare. The trade-off is fuzzy characters. Mounting the filters close to the display reduces this effect. Take care not to overheat the plastic filter by allowing for proper air flow.

Optimal filter enhancements are gained by using circular polarized, anti-reflective, band-pass filters. The circular polarizing further enhances contrast by reducing the light that travels through the filter and reflects back off the display to less than 1.0 %.

Several filter manufacturers supply quality filter materials. Some of them are: Panelgraphic Corporation, W. Caldwell, NJ; SGL Homalite, Wilmington, DE; 3M Company, Visual Products Division, St. Paul, MN; Polaroid Corporation, Polarizer Division, Cambridge, MA; Marks Polarized Corporation, Deer Park, NY, Hoya Optics, Inc., Fremont, CA.

One last note on mounting filters: recessing displays and bezel assemblies is an inexpensive way to provide a shading effect in overhead lighting situations. Several Bezel manufacturers are: R.M.F. Products, Batavia, IL; Nobex Components, Griffith Plastic Corp., Burlingame, CA; Photo Chemical Products of California, Santa Monica, CA; I.E.E.-Atlas, Van Nuys, CA.

Microprocessor Interface

The microprocessor interface is through the serial port, SPI port or one out of eight data bits on the eight bit parallel port and also control lines SDCLK and LOAD.

Power Up Sequence

Upon power up display will come on at random. Thus the display should be reset at power-up. The reset will set the Address Register to Digit 0, User RAM is set to 0 (display blank) the Control Word is set to 0 (100% brightness) and the internal counters are reset.



Figure 12. Display Interface to Siemens/Intel 8031 Microprocessor

(using one bit of parallel port as serial port)



Figure 13. Display Interface with Motorola 68HC05C4 Microprocessor (using SPI port)



Figure 14. Cascading Multiple Displays



Multiple displays can be cascaded using the CLK SEL and CLK I/O pins (Figure 14). The display designated as the Master-Clock source should have its CLK SEL pin tied high and the slaves should have their CLK SEL pins tied low. All CLK I/O pins should be tied together. One display CLK I/O can drive 15 slave CLK I/Os. Use RST to synchronize all display counters.

Loading Data into the Display

Use following procedure to load data into the display:

- 1. Power up the display.
- 2. Bring RST low (600 ns duration minimum) to clear the Multiplex Counter, Address Register, Control Word Register, User Ram and Data Register. The display will be blank. Display brightness is set to 100%.
- 3. If a different brightness is desired, load the proper brightness opcode into the Control Word Register.
- 4. Load the Digit Address into the display.
- 5. Load display row and column data for the selected digit.
- 6. Repeat steps 4 and 5 for all digits.

Data Conte	ents	for t	ne vv	ora	AD	J			
Step	D7	D6	D5	D4	D3	D2	D1	D0	Function
A B (optional)	1 1	1 1	0 1	0 0	0 0	0 0	0 0	0 0	CLEAR 100% BRIGHTNESS
1 2 3 4 5 6 7 8	1 0 0 0 0 0 0	0 0 0 0 0 0 0	1 0 0 0 0 0 0	0 0 1 1 1 1 1	0 0 1 0 1 0 0 0	0 1 0 1 0 0	0 0 1 0 1 0 0	0 0 1 1 1 1	DIGIT D0 SELECT ROW 0 (A) ROW 1 (A) ROW 2 (A) ROW 3 (A) ROW 4 (A) ROW 5 (A) ROW 6 (A)
9 10 11 12 13 14 15 16	1 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 0 0 0 0 0 0	0 1 1 1 1 1 1 1	0 1 0 1 0 0 1	0 1 0 1 0 0 1	0 1 0 1 0 0 1	1 1 1 0 1 1	DIGIT D1 SELECT ROW 0 (B) ROW 1 (B) ROW 2 (B) ROW 3 (B) ROW 4 (B) ROW 5 (B) ROW 6 (B)
17 18 19 20 21 22 23 24	1 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 0 0 0 0 0 0	0 0 1 1 1 0 0	0 0 1 0 0 0 1 0	0 1 0 0 0 0 1	1 0 0 0 0 0 1	0 1 0 0 0 0 1	DIGIT D2 SELECT ROW 0 (C) ROW 1 (C) ROW 2 (C) ROW 3 (C) ROW 4 (C) ROW 5 (C) ROW 6 (C)
25 26 27 28 29 30 31 32	1 0 0 0 0 0 0 0	0 0 0 0 0 0 0	1 0 0 0 0 0 0	0 1 1 1 1 1 1 1	0 1 0 0 0 0 1	0 1 0 0 0 0 1	1 0 0 0 0 0	1 0 1 1 1 1 1 0	DIGIT D3 SELECT ROW 0 (D) ROW 1 (D) ROW 2 (D) ROW 3 (D) ROW 4 (D) ROW 5 (D) ROW 6 (D)

Data Contents for the Word "ABCD"