IP3048CX5

Integrated dual channel passive LC-filter network with ESD protection to IEC 61000-4-2 level 4

Rev. 3 — 10 February 2011 Product data sheet

1. Product profile

1.1 General description

The IP3048CX5 is a low-ohmic, dual channel LC low-pass filter array which is designed to provide filtering of undesired RF signals. In addition, IP3048CX5 incorporates diodes to provide protection to downstream components from ElectroStatic Discharge (ESD) voltages as high as ±15 kV contact discharge according the IEC 61000-4-2 model, far exceeding standard level 4.

The device is fabricated using monolithic silicon technology and integrates two inductors and four pairs of back-to-back diodes in a 0.5 mm pitch Wafer-Level Chip-Scale Package (WLCSP). These features make the IP3048CX5 ideal for use in applications requiring the utmost in miniaturization such as mobile phone handsets, cordless telephones and other portable electronic devices.

1.2 Features and benefits

- Pb-free, RoHS compliant and free of halogen and antimony (Dark Green compliant)
- Integrated dual channel π-type LC-filter network
- 0.25 Ω series resistance per channel; 190 pF channel capacitance
- Integrated ESD protection withstanding ±15 kV contact discharge, far exceeding IEC 61000-4-2 level 4
- WLCSP with 0.5 mm pitch

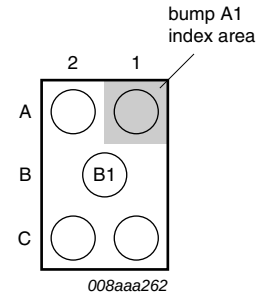
1.3 Applications

Audio line ElectroMagnetic Interference (EMI) filtering and ESD protection in e.g.

- Cellular and Personal Communication System (PCS) mobile handsets
- DECT
- Portable media player

2. Pinning information

2.1 Pinning



transparent top view,
solder balls facing down

Fig 1. Pin configuration for WLCSP5

2.2 Pin description

Table 1. Pinning

Pin	Description
A1	channel 1
A2	channel 2
B1	ground
C1	channel 1
C2	channel 2

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
IP3048CX5	WLCSP5	wafer level chip-size package; 5 bumps (2-1-2)	IP3048CX5

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4. Functional diagram

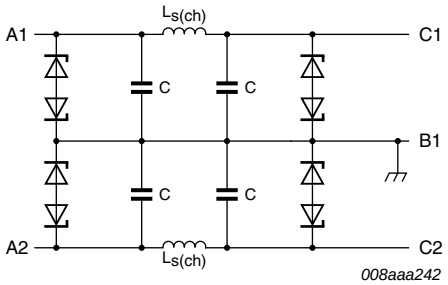

Fig 2. Schematic diagram of IP3048CX5

5. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{RWM}	reverse standoff voltage			-	5	V
I_{ch}	channel current (DC)			-	625	mA
V_{ESD}	electrostatic discharge voltage	all pins to ground				
		contact discharge	[1][2]	−15	+15	kV
		air discharge		−15	+15	kV
		IEC 61000-4-2 level 4; all pins to ground				
		contact discharge		−8	+8	kV
		air discharge		−15	+15	kV
P_{ch}	channel power dissipation	continuous; T_{amb} = 85 °C		-	135	mW
P_{tot}	total power dissipation	continuous; T_{amb} = 85 °C		-	270	mW
P_{PP}	peak pulse power	T_{amb} = 85 °C; maximum peak power dissipation < 120 s; δ < 50 %		-	270	mW
T_{stg}	storage temperature			−65	+150	°C
$T_{reflow(peak)}$	peak reflow temperature	10 s maximum		-	260	°C
T_{amb}	ambient temperature			−40	+85	°C

[1] Device is qualified with 1000 pulses of ±15 kV contact discharges each, according to the IEC 61000-4-2 model and far exceeds the specified level 4 (8 kV contact discharge).

[2] A special robust test is performed stressing the devices with ≥ 1000 contact discharges according to the IEC 61000-4-2 model and far exceeds the specified level 4 (8 kV contact discharge).

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6. Characteristics

Table 4. Channel characteristics

T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{s(ch)}$	channel series resistance			-	0.25	0.35	Ω
$L_{s(ch)}$	channel series inductance			-	3	-	nH
C_{ch}	channel capacitance	$V_{bias(DC)}$ = 2.5 V; f = 100 kHz	[1]	150	190	225	pF
V_{BR}	breakdown voltage	positive clamp; I_{test} = 1 mA		6	-	10	V
		negative clamp; I_{test} = −1 mA		−10	-	−6	V
I_{LR}	reverse leakage current	per channel; V_I = 3 V		-	-	1	μA
		per channel; V_I = −3 V		−1	-	-	μA

[1] Guaranteed by design.

Table 5. Frequency characteristics

T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
α_{il}	insertion loss	R_{gen} = 50 Ω; 800 MHz < f_i < 2 GHz				
		R_L = 50 Ω	-	35	-	dB
		R_L = 4 Ω	-	40	-	dB

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7. Application information

The setup for measuring insertion loss in a 50 Ω system is shown in Figure 3.

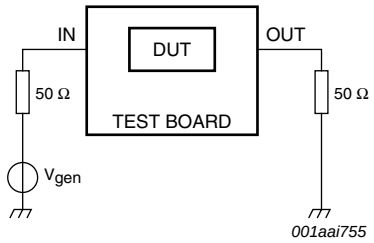
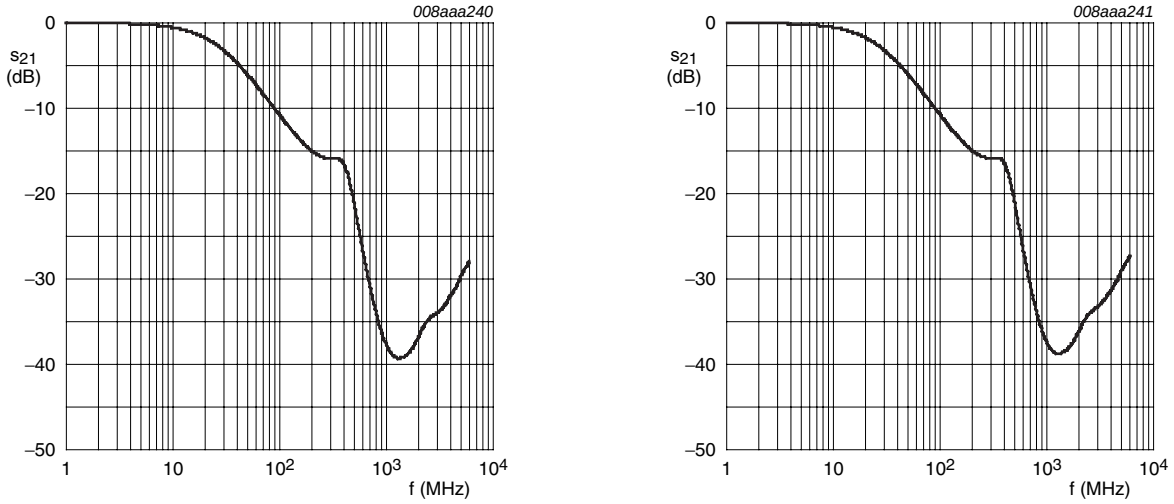


Fig 3. Frequency response measurement configuration

The insertion loss in a 50 Ω system for the two channels of the IP3048CX5 is shown in Figure 4. The insertion loss is measured directly on the wafer with coplanar probes. Unused pins are connected to ground with 50 Ω.



a. Channel 1 (pins A1 and C1).

b. Channel 2 (pins A2 and C2).

Fig 4. Measured insertion loss magnitudes

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8. Package outline

WLCSP5: wafer level chip-size package; 5 bumps (2-1-2)

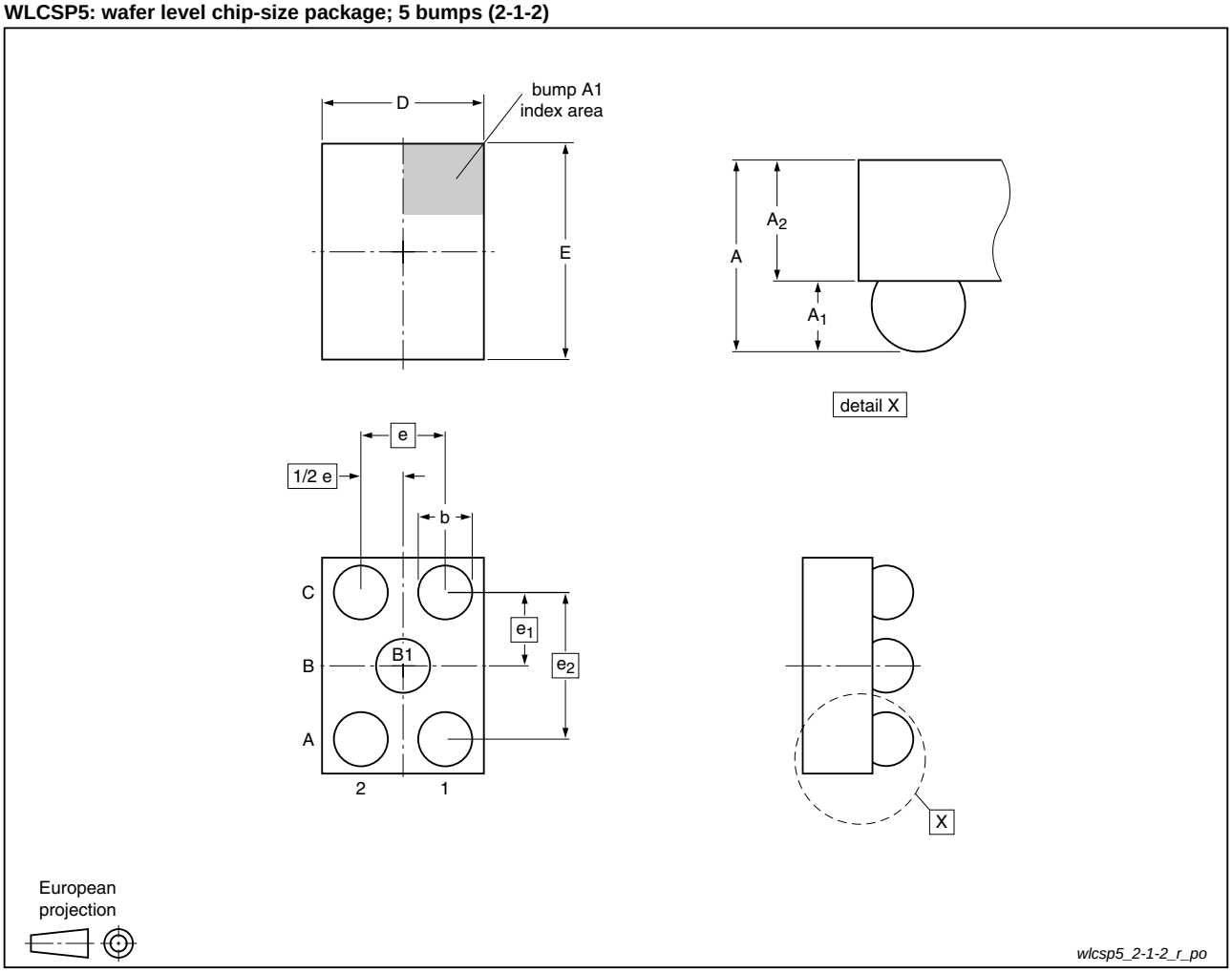

Fig 5. Package outline IP3048CX5 (WLCSP5)

Table 6. Dimensions for Figure 5

Symbol	Min	Typ	Max	Unit
A	0.61	0.65	0.69	mm
A_1	0.22	0.24	0.26	mm
A_2	0.39	0.41	0.43	mm
b	0.27	0.32	0.37	mm
D	1.09	1.14	1.19	mm
E	1.46	1.51	1.56	mm
e	-	0.5	-	mm
e_1	-	0.435	-	mm
e_2	-	0.87	-	mm

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9. Design and assembly recommendations

9.1 PCB design guidelines

It is recommended, for optimum performance, to use a Non-Solder Mask Defined (NSMD), also known as a copper-defined design, incorporating laser-drilled micro-vias connecting the ground pads to a buried ground-plane layer. This results in the lowest possible ground inductance and provides the best high frequency and ESD performance. Refer to Table 7 for the recommended PCB design parameters.

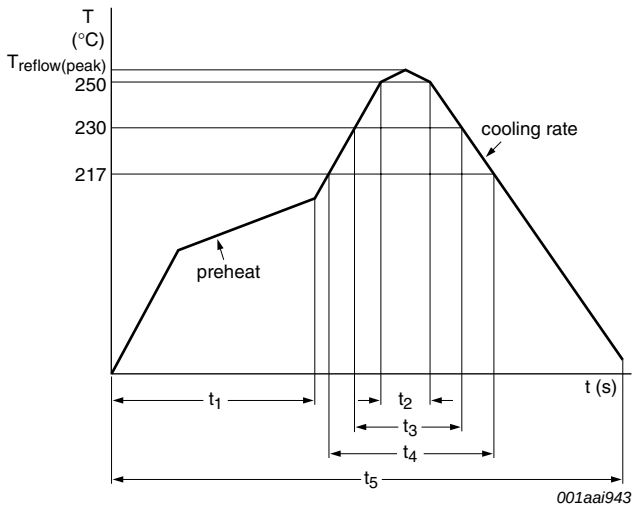
Table 7. Recommended PCB design parameters

Parameter	Value or specification
PCB pad diameter	275 μm
Micro-via diameter	100 μm (0.004 inch)
Solder mask aperture diameter	375 μm
Copper thickness	20 μm to 40 μm
Copper finish	AuNi
PCB material	FR4

9.2 PCB assembly guidelines for Pb-free soldering

Table 8. Assembly recommendations

Parameter	Value or specification
Solder screen aperture diameter	330 μm
Solder screen thickness	100 μm (0.004 inch)
Solder paste: Pb-free	SnAg (3 % to 4 %); Cu (0.5 % to 0.9 %)
Solder to flux ratio	50 : 50
Solder reflow profile	see Figure 6



The device is capable of withstanding at least three reflows of this profile.

Fig 6. Pb-free solder reflow profile

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Table 9. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{reflow(peak)}$	peak reflow temperature		230	-	260	°C
t_1	time 1	soak time	60	-	180	s
t_2	time 2	time during T ≥ 250 °C	-	-	30	s
t_3	time 3	time during T ≥ 230 °C	10	-	50	s
t_4	time 4	time during T > 217 °C	30	-	150	s
t_5	time 5		-	-	540	s
dT/dt	rate of change of temperature	cooling rate	-	-	–6	°C/s
		preheat	2.5	-	4.0	°C/s

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
DUT	Device Under Test
EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharge
FR4	Flame Retard 4
NSMD	Non-Solder Mask Defined
PCB	Printed-Circuit Board
PCS	Personal Communication System
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
WLCSP	Wafer-Level Chip-Scale Package

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
IP3048CX5 v.3	20110210	Product data sheet	-	IP3048CX5 v.2
Modifications:	• Figure 1 and Figure 5: changed			
IP3048CX5 v.2	20101104	Product data sheet	-	IP3048CX5 v.1
IP3048CX5 v.1	20101018	Product data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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14. Contents

1	**Product profile**	**1**
1.1	General description	1
1.2	Features and benefits	1
1.3	Applications	1
2	**Pinning information**	**2**
2.1	Pinning	2
2.2	Pin description	2
3	**Ordering information**	**2**
4	**Functional diagram**	**3**
5	**Limiting values**	**3**
6	**Characteristics**	**4**
7	**Application information**	**5**
8	**Package outline**	**6**
9	**Design and assembly recommendations**	**7**
9.1	PCB design guidelines	7
9.2	PCB assembly guidelines for Pb-free soldering	7
10	**Abbreviations**	**8**
11	**Revision history**	**8**
12	**Legal information**	**9**
12.1	Data sheet status	9
12.2	Definitions	9
12.3	Disclaimers	9
12.4	Trademarks	10
13	**Contact information**	**10**
14	**Contents**	**11**

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