HMC677LP5 / 677LP5E

v05.0810

6-Bit SERIAL/PARALLEL SWITCH DRIVER/CONTROLLER

Designer's Kit Available

Typical Applications

The HMC677LP5(E) is ideal for:

- Microwave and Millimeterwave Control Circuits
- Test and Measurement Equipment
- Complex Multi-Function Assemblies
- Military and Space Subsystems
- Transmit/Receive Module Controllers

Features

Accepts Serial or Parallel Data

Compatible with TTL and CMOS Logic

Complementary Outputs

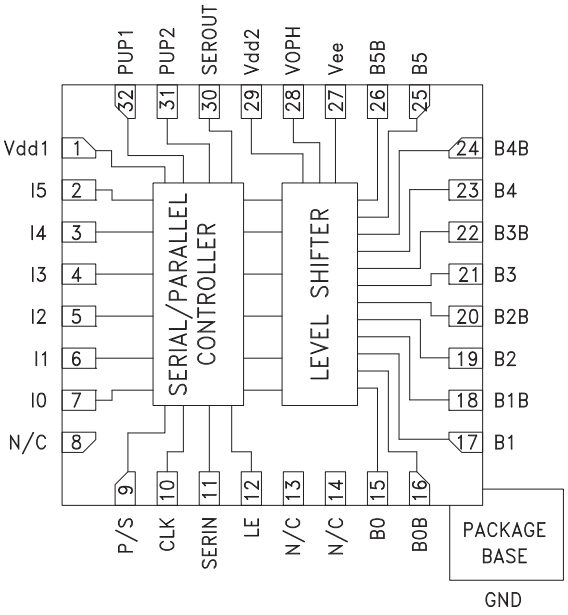
6-Bit Control Word

Power-up State Selection

Low Power Consumption

Fast Clock Rate

Functional Diagram



General Description

The HMC677LP5(E) is a multi-function BiCMOS control interface IC which is ideal for driving the gates of FET and pHEMT based MMIC control devices. This unique IC can be used to simplify the control of microwave and millimeterwave transmit/receive modules, military subsystems, and multi-throw/multi-port test and measurement equipment. The HMC677LP5(E) accepts serial or parallel data, and can drive up to 6 complementary sets of outputs.

The HMC677LP5(E) also provides additional functionality such as a power-up state selection, adjustable output voltage levels, and a latched parallel control mode which allows multiple control devices to share a common data bus. The HMC677LP5(E) is ideal for controlling digital phase shifters, digital attenuators, digital variable gain amplifiers, and switching matrices embedded in complex microwave and millimeterwave assemblies.

Electrical Specifications, T_A = +25° C, Vdd1 = Vdd2 = +5V, Vee = -5V, Voph = 0V

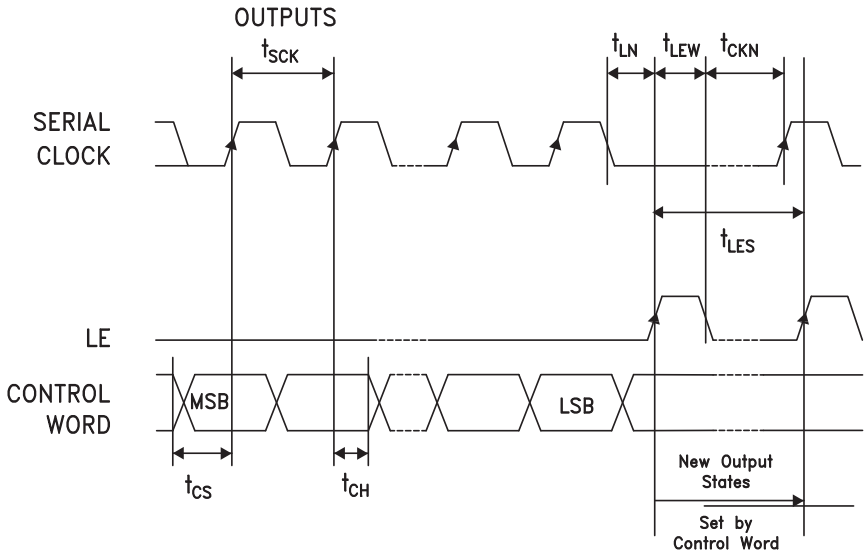
Parameter	Min	Typ	Max	Units
Input High Voltage, Vih	2	-	-	V
Low Voltage, Vil	-	-	0.8	V
Output High Voltage, Voh (Ioh = 1 mA, Vee = -4.5V)	Voph - 0.1	-	-	V
Output Low Voltage, Vol (Iol = 2 mA, Vee = -4.5V)	-	-	Vee + 0.1	V
Maximum Input Leakage Current, Iin	-	-	1	µA
Propagation Delay, tplh	-	-	80	nS
Maximum Serial Bit Rate	-	-	10	Mbps
Maximum I/O Update Rate	-	-	100	ns

Serial Control Interface

The HMC677LP5(E) contains a 3-wire SPI compatible digital interface (DATA, CLK, LE). It is activated when P/S is kept high. The 6-bit serial word must be loaded MSB first. The positive-edge sensitive CLK and LE requires clean transitions. Standard logic families work well. When LE is high, 6-bit data in the serial input register is transferred to the outputs. When LE is high CLK is masked to prevent data transition during output loading.

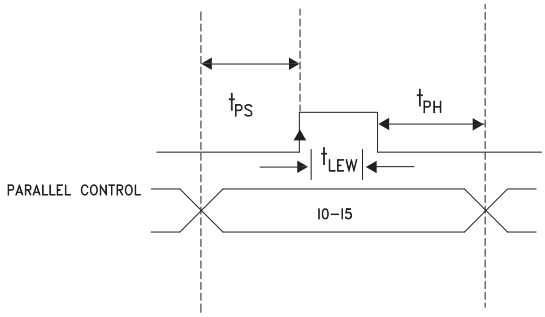
When P/S is low, 3-wire SPI interface inputs (DATA, CLK, LE) are disabled and the serial input register is loaded asynchronously with parallel digital inputs (I0-I5). When LE is high, 6-bit parallel data is transferred.

For all modes of operations, the outputs will stay constant while LE is kept low.



Parameter	Typ.
Min. serial period, t_{SCK}	100 ns
Control set-up time, t_{CS}	20 ns
Control hold-time, t_{CH}	20 ns
LE setup-time, t_{LN}	10 ns
Min. LE pulse width, t_{LEW}	10 ns
Min LE pulse spacing, t_{LES}	630 ns
Serial clock hold-time from LE, t_{CKN}	10 ns
Hold Time, $t_{PH.}$	0 ns
Latch Enable Minimum Width, t_{LEN}	10 ns
Setup Time, t_{PS}	2 ns

Timing Diagram (Latched Parallel Mode)



Parallel Mode (Direct Parallel Mode & Latched Parallel Mode)

Note: The parallel mode is enabled when P/S is set to low.

Direct Parallel Mode - Outputs are changed by the Control Voltage Inputs directly. The LE (Latch Enable) must be at a logic high to control in this manner.

Latched Parallel Mode - Outputs are selected using the Control Voltage Inputs and set while the LE is in the Low state. This will not change state while LE is Low. Once all Control Voltage Inputs are at the desired states the LE is pulsed. See timing diagram above for reference.

Operating Ranges

Function	Parameter	Min.	Typ.	Max	Units
Vdd	Positive DC Supply Voltage	4.5	5.0	5.5	V
Vee	Negative DC Supply Voltage	-5.5	-5.0	-4.5	V
Voph [1]	DC Output Supply	0	-	2.2	V
Voph - Vee	Negative Supply Voltage Range	4.5	-	7.7	V
Vdd - Vee	Positive to Negative Supply Range	9	10	11	V
Ta	Operating Ambient Temperature	-40	25	85	C
Ioh [2]	DC Output Current - High	1	-	-	mA
Iol [2]	DC Output Current - Low	2	-	-	mA

[1] Voph can be used from 0V to 2.2V. Higher voltages can be used to increase low frequency performance of GaAs switches.
[2] Ioh and Iol are measured at 0.1V variation from Voph and Vee.

DC Characteristics

Function	Parameter	Conditions		Min.	Typ.	Max	Units
Vih	Input High Voltage	High Input Voltage		2.0	-	-	V
Vil	Input Low Voltage	Low Input Voltage		-	-	0.8	V
Voh	Output High Voltage	Ioh = 1 mA	Vee = -4.5V	Voph - 0.1	-	-	V
Vol	Output Low Voltage	Iol = 2 mA	Vee = -4.5V	-	-	Vee +0.1	V
Iin	Input Leakage Current	Vin = Vdd or GND	Vdd = Max	-	-	1	µA
Idd	Quiescent Supply Current	Vdd = Max	Vin = Vdd or GND	-	-	1.5	mA
^ Idd	Additional Supply Current Per TTL Input Pin	Vdd = Max	Vin = 2V	-	-	50	µA

Worst Case AC Characteristics at Voph = 2.2V (Vdd = 4.5V, Vee = -4.5V)

Function	Parameter	-40 °C	+25 °C	+85 °C	Units
Tplh	Rising Propagation Delay	30	30	30	ns
Tphl	Falling Propagation Delay	30	30	30	ns
Ttlh	Output Rising Transition Time	30	40	40	ns
Tthl	Output Falling Transition Time	15	20	20	ns
Tskew	Delay Skew	50	50	50	nS
Cpdd[1]	Power Dissipation Capacitance of Vdd	100	100	100	pF
Cpde[1]	Power Dissipation Capacitance of Vee	400	400	400	pF

Worst Case AC Characteristics at Voph = 0V (Vdd = 4.5V, Vee = -4.5V)

Function	Parameter	-40 °C	+25 °C	+85 °C	Units
Tplh	Rising Propagation Delay	80	80	80	ns
Tphl	Falling Propagation Delay	80	80	80	ns
Ttlh	Output Rising Transition Time	100	100	100	ns
Tthl	Output Falling Transition Time	50	50	50	ns
Tskew	Delay Skew	50	50	50	nS
Cpdd[1]	Power Dissipation Capacitance of Vdd	100	100	100	pF
Cpde[1]	Power Dissipation Capacitance of Vee	400	400	400	pF

[1] Total Power Dissipation is calculated by the following formula: PD = Vdd^2 f Cpdd + $(Voph - Vee)^2$ f Cpde, where f = frequency in Hz

Power-Up States

If LE is set to logic LOW at power-up, the logic state of PUP1 and PUP2 determines the power-up state of the part per PUP truth table. If the LE is set to logic HIGH at power-up, the logic state of I5-I0 determines the power-up state of the part per truth table. The attenuator latches in the desired power-up state approximately 200 ms after power-up.

Power-On Sequence

The required power-up sequence is: GND, Vdd, Vee, Voph, Digital Inputs (I_0 - I_5). The relative application of input signal order of the digital inputs are not important. Deviations from this sequence may inadvertently forward bias ESD protection structures and damage them. For added protection you may install 2 kOhm resistors in series with each digital input signal line, however these resistors will increase the RC time constant.

Control Voltage Table

State	Vdd = +3V	Vdd = +5V
Low	0 to 0.5V @ <1 µA	0 to 0.8V @ <1 µA
High	2 to 3V @ <1 µA	2 to 5V @ <1 µA

Truth Table

Input	Outputs	
Ix	Bx	BxB
Low	Vee	Voph
High	Voph	Vee

PUP Truth Table

LE	PUP2	PUP1	Output States					
			B5	B4	B3	B2	B1	B0
0	0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0
0	1	0	1	0	0	0	0	0
0	1	1	1	1	1	1	1	1
1	X	X	Set by the inputs Ix					

For the Inputs (LE, PUP1, PUP2), Logic “0” = 0V and Logic “1” = Vdd

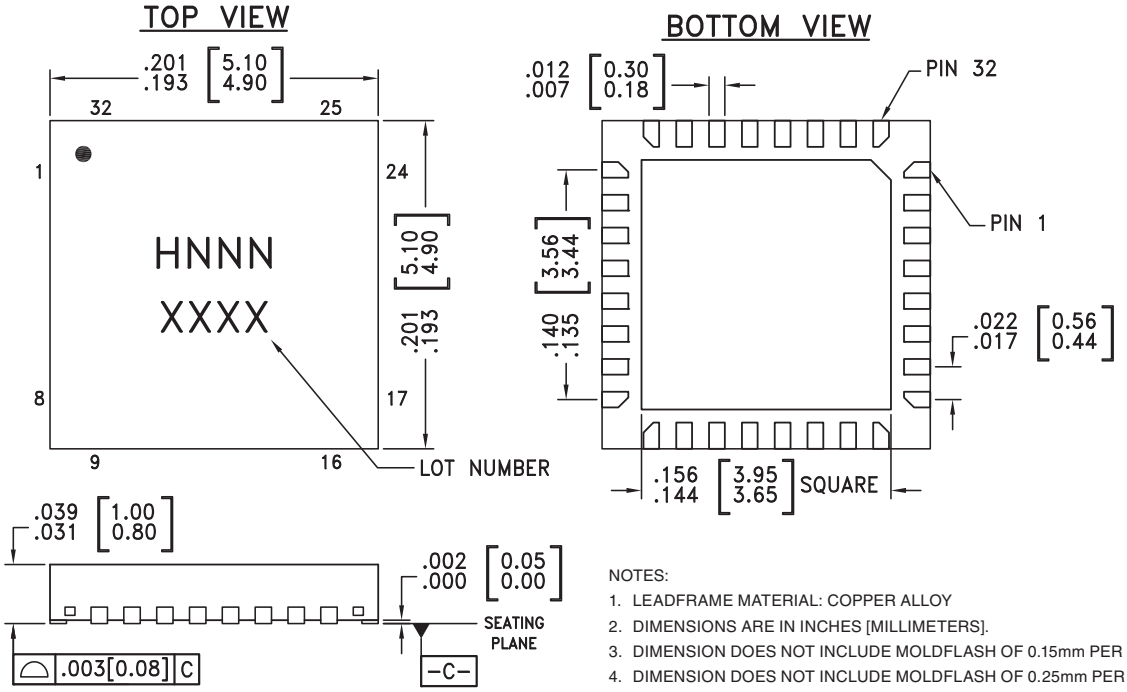
For the outputs, Logic “0” is Bx = Vee, BxB = Voph, and Logic “1” is Bx = Voph, BxB = Vee

Absolute Maximum Ratings

Digital Inputs (I0-I5, Shift Clock, Latch Enable, P/S, PUP and Data Inputs)	-0.5 to Vdd +0.5V
Bias Voltage (Vdd)	5.6 V
Bias Voltage (Vee)	-5.6 V
Bias Voltage (Voph)	2.3 V
Channel Temperature	125 °C
Continuous Pdiss (T = 85 °C) (derate 8.2 mW/°C above 85 °C) [1]	325 mW
Thermal Resistance (Channel to ground paddle)	123 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

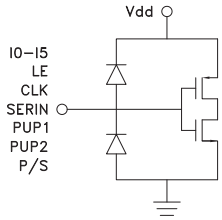
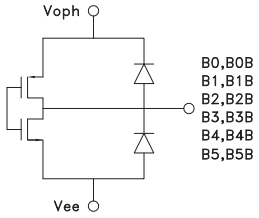
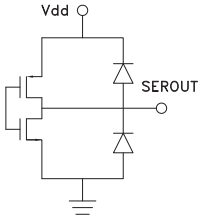
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS].
3. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.15mm PER SIDE.
4. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.25mm PER SIDE.
5. ALL GROUND LEADS MUST BE SOLDERED TO PCB GROUND.
6. CLASSIFIED AS MOISTURE SENSITIVITY LEVEL (MSL) 1.

Package Information

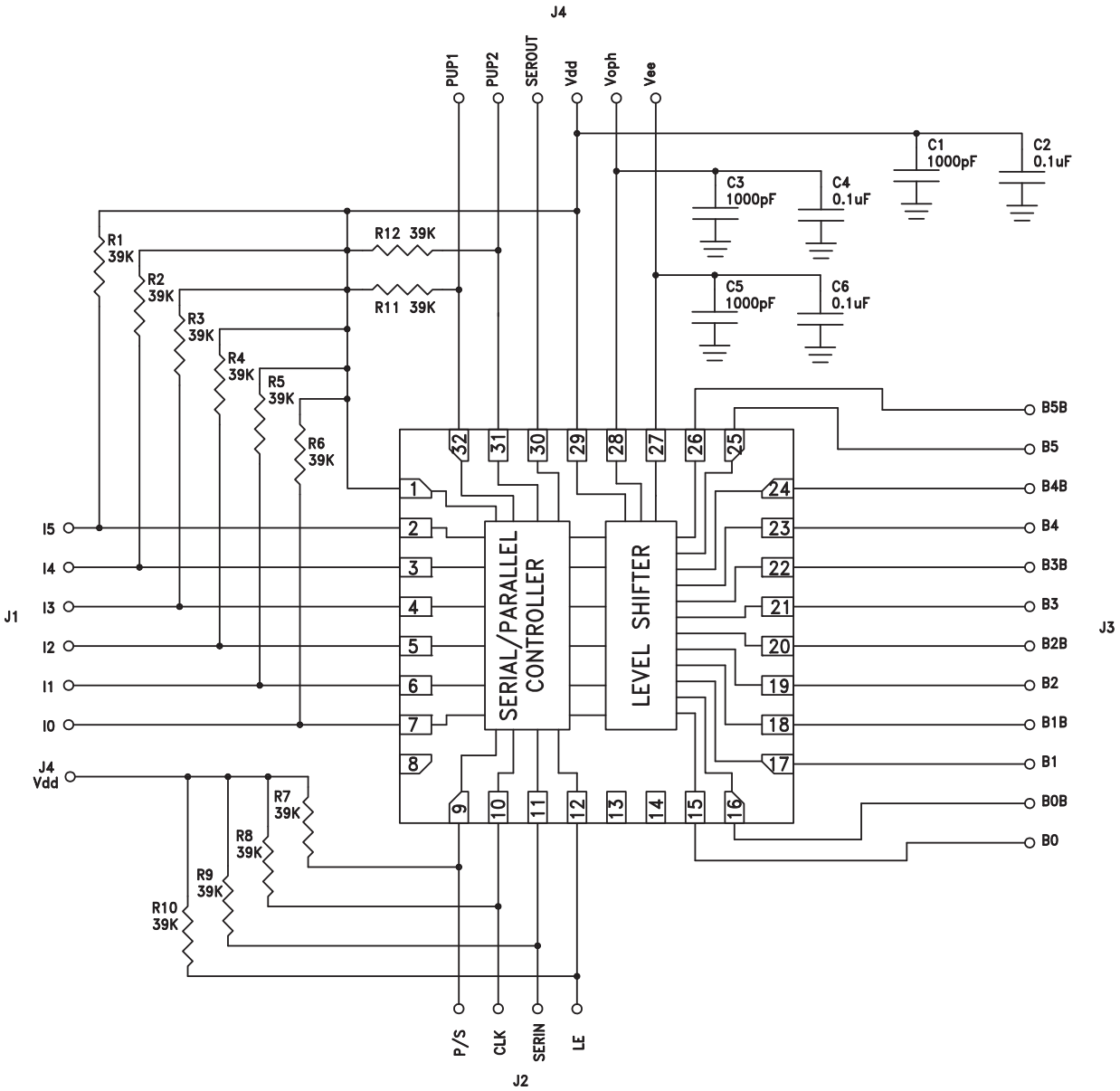
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC677LP5	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	H677 XXXX
HMC677LP5E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H677 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

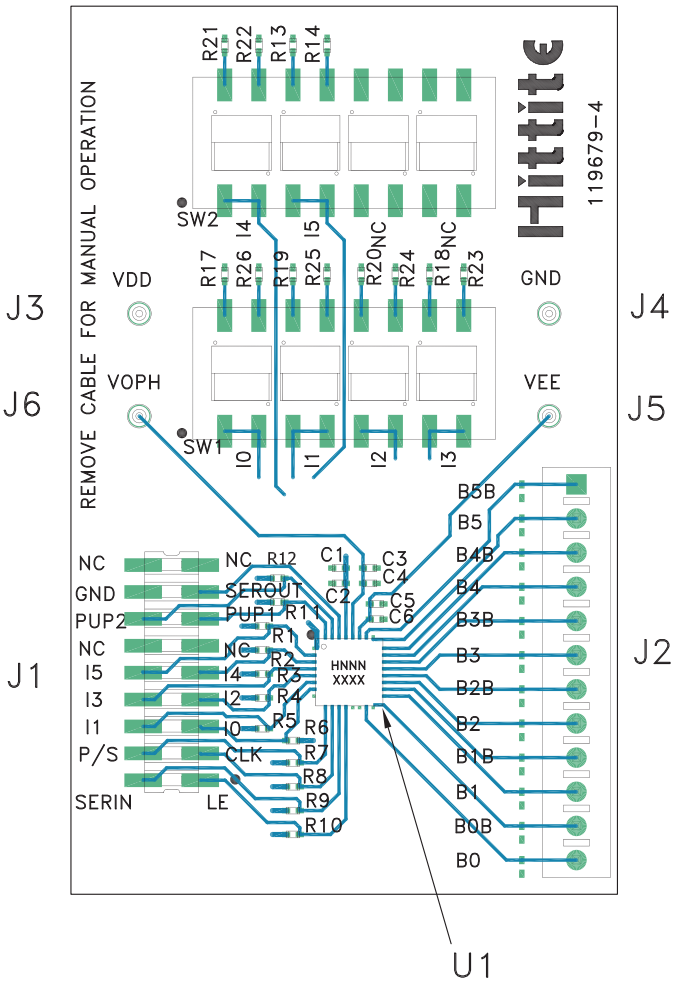
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 29	Vdd1, Vdd2	Supply Voltage	
2 - 7	I0 - I5	See Truth Table, Control Voltage Table and Timing Diagram	
9	P/S		
10	CLK		
11	SERIN		
12	LE		
31, 32	PUP2, PUP1		
8, 13, 14	N/C	No connection necessary. These pins may be connected to DC ground.	
15, 17, 19, 21, 23, 25	B0 - B5	Complementary Outputs	
16, 18, 20, 22, 24, 26	B0B - B5B		
27	Vee	Negative Supply.	
28	VOPH	User selectable output high voltage 0 to +2.2V	
30	SEROUT	Serial input data delayed by six clock cycles.	

Application & Evaluation PCB Schematic



Evaluation PCB



List of Materials for Evaluation PCB 119681 [1][3]

Item	Description
J1	18 Pin DC Connector
J2	12 Pin DC Connector
J3 - J6	DC Pin
C1, C3, C5	1000 pF Capacitor, 0402 Pkg.
C2, C4, C6	0.1 µF Capacitor, 0402 Pkg.
R1 - R12	39 kΩ Resistor, 0402 Pkg.
R13, R14, R17 - R26	100 kΩ Resistor, 0402 Pkg.
SW1, SW2	SPDT 4 Position DIP Switch
U1	HMC677LP5(E) 6-Bit Digital Level Shifter
PCB [2]	119679 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: FR4

[3] Please refer to part's pin description and functional diagram for pin out assignments on evaluation board.

The evaluation circuit board shown is available from Hittite upon request.