

## Features

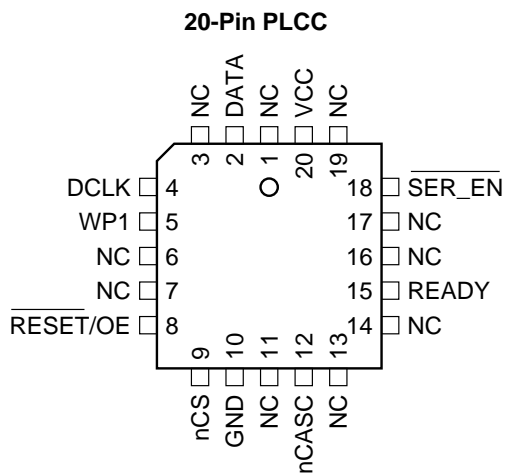
- Serial EEPROM Family for Configuring Altera FLEX® 10K Devices
- Simple, Easy-to-use 4-pin Interface
- E<sup>2</sup> Programmable 1M Bit Serial Memories Designed To Store Configuration Programs For Programmable Gate Arrays
- Cascadable To Support Additional Configurations or Future Higher-density Arrays
- Low-power CMOS EEPROM Process
- Programmable Reset Polarity
- Available in the Space-efficient Surface-mount PLCC Package
- In-System Programmable Via 2-Wire Bus
- Emulation of 24CXX Serial EPROMs
- Available in 3.3V ± 10% LV and 5V ± 5% C Versions

## Description

The AT17C512/010A and AT17LV512/010A (AT17A Series) FPGA Configuration EEPROMs (Configurators) provide an easy-to-use, cost-effective configuration memory for programming Altera FLEX Field Programmable Gate Arrays, FPGA, (the “devices”). The AT17A Series is packaged in the popular 20-pin PLCC package. The AT17A Series family uses a simple serial-access procedure to configure one or more FPGA devices. The AT17A Series organization supplies enough memory to configure one or multiple smaller FPGAs. Using a special feature of the AT17A Series, the user can select the polarity of the reset function by programming an EEPROM byte. The AT17C/LV512/010A parts generate their own internal clock and can be used as a system “master” for loading the FPGA devices.

The Atmel devices also supports a system friendly READY pin and a write protect mechanism. The READY pin is used to simplify system power-up considerations. The WP1 pin is used to protect part of the device memory during in-system programming. The AT17A Series can be programmed with industry standard programmers.

## Pin Configurations

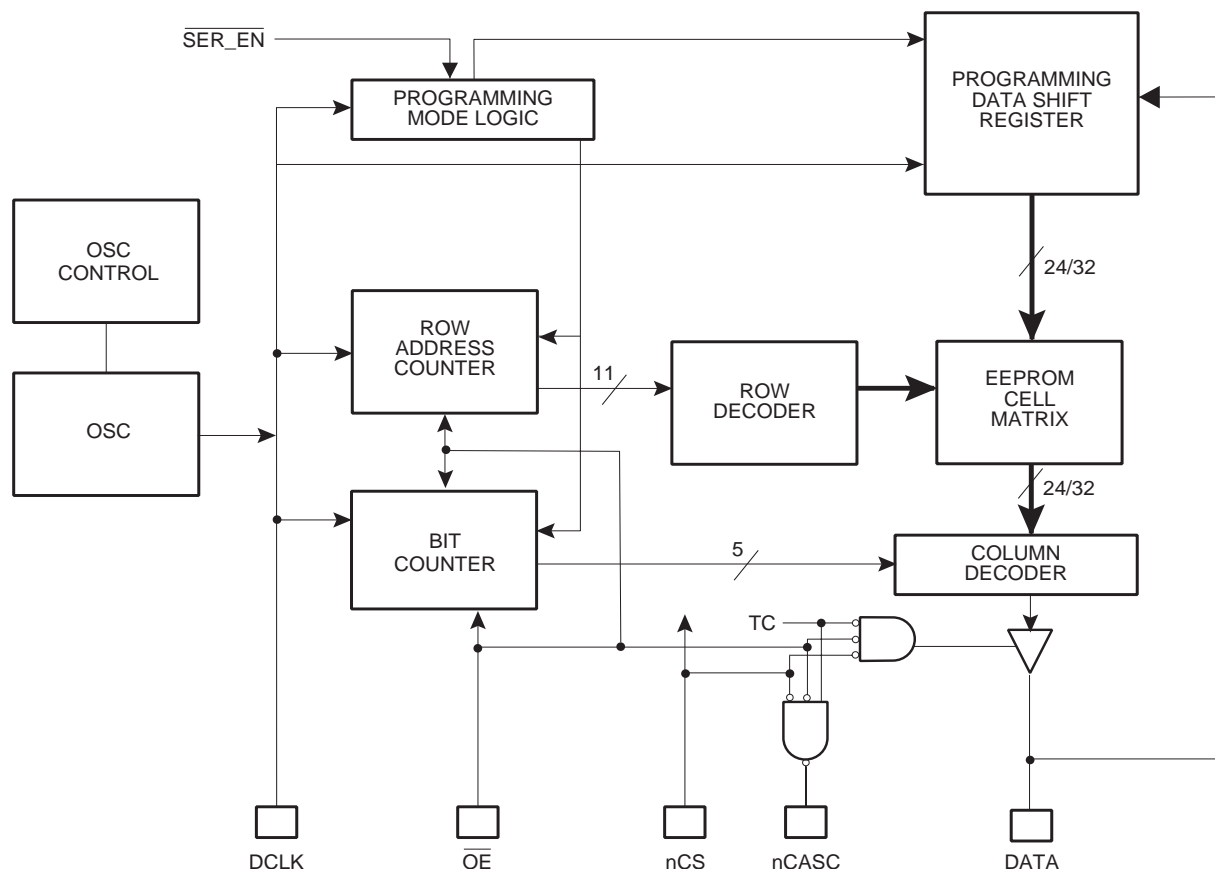


## FPGA Serial Configuration Memories

**AT17C512A**  
**AT17LV512A**  
**AT17C010A**  
**AT17LV010A**



## Block Diagram



## Device Configuration

The control signals for configuration EEPROMs—nCS, OE, and DCLK—interface directly with the FPGA device control signals. All FPGA devices can control the entire configuration process and retrieve data from the configuration EEPROM without requiring an external intelligent controller.

The configuration EEPROM device's OE and nCS pins control the tri-state buffer on the DATA output pin and enable the address counter and the oscillator. When OE is driven low, the configuration EEPROM device resets the address counter and tri-states its DATA pin. The nCS pin controls the output of the AT17A Series. If nCS is held high after the OE reset pulse, the counter is disabled and the DATA output pin is tri-stated. When nCS is driven low, the counter and the DATA output pin are enabled. When OE is driven low again, the address counter is reset and the DATA output pin is tri-stated, regardless of the state of the nCS.

When the configurator has driven out all of its data and nCASC is driven low, the device tri-states the DATA pin to avoid contention with other configurators. Upon power-up, the address counter is automatically reset.

## FPGA Device Configuration

FPGA devices can be configured with an AT17A Series EEPROM. The AT17A Series device stores configuration data in its EEPROM array and clocks the data out serially with its internal oscillator. The OE, nCS, and DCLK pins supply the control signals for the address counter and the output tri-state buffer. The AT17A Series device sends a serial bitstream of configuration data to its DATA pin, which is connected to the DATA0 input pin on the FPGA device.

When configuration data for a FPGA device exceeds the capacity of a single AT17A Series device, multiple AT17A Series devices can be serially linked together. When multiple AT17A Series devices are required, the nCASC and nCS pins provide handshaking between the AT17A Series devices.

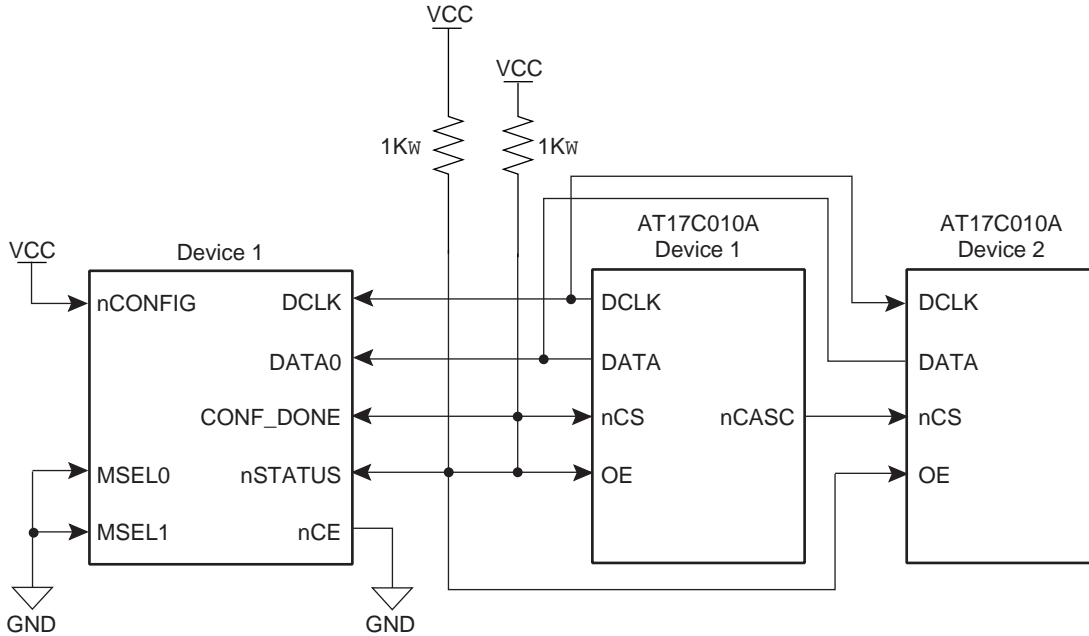
The position of an AT17A Series device in a chain determines its operation. The first AT17A Series device in a Configurator chain is powered up or reset with nCS low and is configured for FPGA devices protocol. This AT17A Series device supplies all clock pulses to one or more FPGA devices and to any downstream AT17A Series during configuration. The first AT17A Series device also provides the first stream of data to the FPGA devices during

multi-device configuration. Once the first AT17A Series device finishes sending configuration data, it drives its nCASC pin low, which drives the nCS pin of the second AT17A Series device low. This activates the second AT17A Series device to send configuration data to the FPGA device.

The first AT17A Series device clocks all subsequent AT17A Series devices until configuration is complete. Once all configuration data is transferred and nCS on the first

AT17A Series device is driven high by CONF\_DONE on the FPGA devices, the first AT17A Series device clocks 16 additional cycles to initialize the FPGA device. Then the first AT17A Series device goes into zero-power (idle) state. If nCS on the first AT17A Series device is driven high before all configuration data is transferred—or if the nCS is not driven high after all configuration data is transferred—the nSTATUS is driven low, indicating a configuration error.

**Figure 1.** FPGA Device Configured with Two AT17A Series Devices





## Pin Configurations

| Pin Number<br>(20-Pin PLCC) | Pin Name                     | Pin Type | Description   |
|-----------------------------|------------------------------|----------|---|
| 2                           | DATA                         | Output   | Serial data output.   |
| 4                           | DCLK                         | I/O      | Clock output or clock input. Rising edges on DCLK increment the internal address counter and present the next bit of data to the DATA pin. The counter is incremented only if the OE input is held high, the nCS input is held low, and all configuration data has not been transferred to the target device (otherwise, in FPGA 10K master mode, the DCLK pin drives low). |
| 5                           | WP1                          | Input    | WRITE PROTECT (1). Used to protect portions of memory during programming. See programming guide for details.  |
| 8                           | $\overline{\text{RESET/OE}}$ | Input    | Output enable (active high) and reset (active low). A low logic level resets the address counter. A high logic level enables DATA and permits the address counter to count. In the mode, if this pin is low (reset), the internal oscillator becomes inactive and DCLK drives low.  |
| 9                           | nCS                          | Input    | Chip select input (active low). A low input allows DCLK to increment the address counter and enables DATA to drive out. If the AT17A Series is reset with nCS low, the device initializes as the first device in a daisy-chain. If the AT17A Series is reset with nCS high, the device initializes as the next AT17A Series device in the chain                             |
| 10                          | GND                          | Ground   | A 0.2 $\mu\text{F}$ decoupling capacitor should be placed between the $V_{\text{CC}}$ and GND pins.   |
| 12                          | nCASC                        | Output   | Cascade select output (active low). This output goes low when the address counter has reached its maximum value. In a daisy-chain of AT17A Series devices, the nCASC pin of one device is usually connected to the nCS input pin of the next device in the chain, which permits DCLK to clock data from the next AT17A Series device in the chain.                          |
|                             | A2                           | Input    | Device selection input, A2. This is used to enable (or select) the device during programming, when $\overline{\text{SER\_EN}}$ is Low (see Programming Guide for more details)  |
| 15                          | READY                        | Output   | Open collector reset state indicator. Driven Low during power-up reset, released when power-up is complete. (Recommend a 4.7K $\Omega$ Pull-up on this pin if used).  |
| 18                          | $\overline{\text{SER\_EN}}$  | Input    | Serial enable is normally high during FPGA loading operations. Bringing SER_EN Low, enables the two wire serial interface mode for programming.   |
| 20                          | $V_{\text{CC}}$              | Power    | Power pin.  |

## Absolute Maximum Ratings\*

|   |                                 |
|---|---------------------------------|
| Operating Temperature .....   | -55°C to +125°C                 |
| Storage Temperature .....   | -65°C to +150°C                 |
| Voltage on Any Pin<br>with Respect to Ground .....                              | -0.1V to $V_{\text{CC}}$ + 0.5V |
| Supply Voltage ( $V_{\text{CC}}$ ) .....  | -0.5V to +7.0V                  |
| Maximum Soldering Temp. (10 s @ 1/16 in.).....                                  | 260°C                           |
| ESD ( $R_{\text{ZAP}} = 1.5\text{K}$ , $C_{\text{ZAP}} = 100\text{ pF}$ ) ..... | 2000V                           |

\*NOTICE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

**Operating Conditions**

| Symbol          | Description |   | AT17CXXXA |      | AT17LVXXXA |     | Units |
|-----------------|-------------|---|-----------|------|------------|-----|-------|
|                 |             |   | Min       | Max  | Min        | Max |       |
| V <sub>CC</sub> | Commercial  | Supply voltage relative to GND<br>-0°C to +70°C   | 4.75      | 5.25 | 3.0        | 3.6 | V     |
|                 | Industrial  | Supply voltage relative to GND<br>-40°C to +85°C  | 4.5       | 5.5  | 3.0        | 3.6 | V     |
|                 | Military    | Supply voltage relative to GND<br>-55°C to +125°C | 4.5       | 5.5  | 3.0        | 3.6 | V     |



## DC Characteristics

$V_{CC} = 5V \pm 5\%$  Commercial /  $5V \pm 10\%$  Ind./Mil.

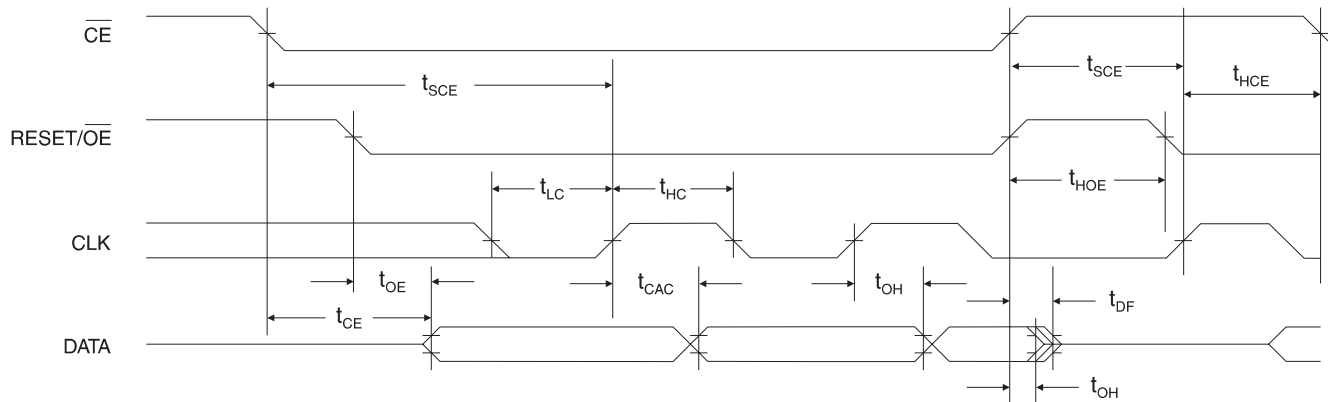
| Symbol    | Description   |                     | Min | Max      | Units   |
|-----------|---|---------------------|-----|----------|---------|
| $V_{IH}$  | High-level input voltage                                    |                     | 2.0 | $V_{CC}$ | V       |
| $V_{IL}$  | Low-level input voltage                                     |                     | 0   | 0.8      | V       |
| $V_{OH}$  | High-level output voltage ( $I_{OH} = -4$ mA)               | Commercial          | 3.7 |          | V       |
| $V_{OL}$  | Low-level output voltage ( $I_{OL} = +4$ mA)                |                     |     |          |         |
| $V_{OH}$  | High-level output voltage ( $I_{OH} = -4$ mA)               | Industrial          | 3.6 |          | V       |
| $V_{OL}$  | Low-level output voltage ( $I_{OL} = +4$ mA)                |                     |     |          |         |
| $V_{OH}$  | High-level output voltage ( $I_{OH} = -4$ mA)               | Military            | 3.5 |          | V       |
| $V_{OL}$  | Low-level output voltage ( $I_{OL} = +4$ mA)                |                     |     |          |         |
| $I_{CCA}$ | Supply current, active mode                                 |                     |     | 10       | mA      |
| $I_L$     | Input or output leakage current ( $V_{IN} = V_{CC}$ or GND) |                     | -10 | 10       | $\mu$ A |
| $I_{CCS}$ | Supply current, standby mode AT17010A/512A                  | Commercial          |     | 150      | $\mu$ A |
|           |   | Industrial/Military |     | 150      | $\mu$ A |

## DC Characteristics

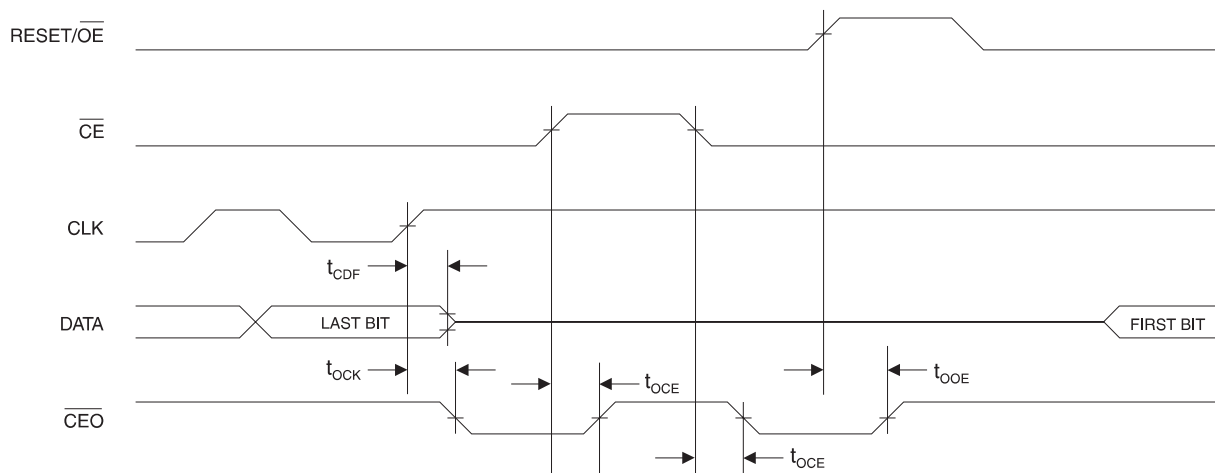
$V_{CC} = 3.3V \pm 10\%$

| Symbol    | Description   |                     | Min | Max      | Units   |
|-----------|---|---------------------|-----|----------|---------|
| $V_{IH}$  | High-level input voltage                                    |                     | 2.0 | $V_{CC}$ | V       |
| $V_{IL}$  | Low-level input voltage                                     |                     | 0   | 0.8      | V       |
| $V_{OH}$  | High-level output voltage ( $I_{OH} = -2.5$ mA)             | Commercial          | 2.4 |          | V       |
| $V_{OL}$  | Low-level output voltage ( $I_{OL} = +3$ mA)                |                     |     |          |         |
| $V_{OH}$  | High-level output voltage ( $I_{OH} = -2$ mA)               | Industrial          | 2.4 |          | V       |
| $V_{OL}$  | Low-level output voltage ( $I_{OL} = +3$ mA)                |                     |     |          |         |
| $V_{OH}$  | High-level output voltage ( $I_{OH} = -2$ mA)               | Military            | 2.4 |          | V       |
| $V_{OL}$  | Low-level output voltage ( $I_{OL} = +2.5$ mA)              |                     |     |          |         |
| $I_{CCA}$ | Supply current, active mode                                 |                     |     | 5        | mA      |
| $I_L$     | Input or output leakage current ( $V_{IN} = V_{CC}$ or GND) |                     | -10 | 10       | $\mu$ A |
| $I_{CCS}$ | Supply current, standby mode                                | Commercial          |     | 50       | $\mu$ A |
|           |   | Industrial/Military |     | 50       | $\mu$ A |

### AC Characteristics



### AC Characteristics When Cascading





## AC Characteristics for AT17C010A/512A

$V_{CC} = 5V \pm 5\%$  Commercial /  $V_{CC} = 5V \pm 10\%$  Ind./Mil

| Symbol          | Description   | Commercial |     | Industrial/Military |     | Units |
|-----------------|---|------------|-----|---------------------|-----|-------|
|                 |   | Min        | Max | Min                 | Max |       |
| $T_{OE}^{(2)}$  | OE to Data Delay                                      |            | 30  |                     | 35  | ns    |
| $T_{CE}^{(2)}$  | nCS to Data Delay                                     |            | 45  |                     | 45  | ns    |
| $T_{CAC}^{(2)}$ | CLK to Data Delay                                     |            | 50  |                     | 55  | ns    |
| $T_{OH}^{(2)}$  | Data Hold From nCS, OE, or DCLK                       | 0          |     | 0                   |     | ns    |
| $T_{DF}^{(3)}$  | nCS or OE to Data Float Delay                         |            | 50  |                     | 50  | ns    |
| $T_{LC}$        | CLK Low Time Slave Mode                               | 20         |     | 20                  |     | ns    |
| $T_{HC}$        | CLK High Time Slave Mode                              | 20         |     | 20                  |     | ns    |
| $T_{SCE}$       | nCS Setup Time to DCLK (to guarantee proper counting) | 20         |     | 25                  |     | ns    |
| $T_{HCE}$       | nCS Hold Time to DCLK (to guarantee proper counting)  | 0          |     | 0                   |     | ns    |
| $T_{HOE}$       | OE High Time (Guarantees Counter Is Reset)            | 20         |     | 20                  |     | ns    |
| $F_{MAX}$       | MAX Input Clock Frequency Slave Mode                  | 15         |     | 15                  |     | MHz   |
| $T_{LC}$        | CLK Low Time Master Mode                              | 30         | 250 | 30                  | 250 | ns    |
| $T_{HC}$        | CLK High Time Master Mode                             | 30         | 250 | 30                  | 250 | ns    |
| $V_{RDY}$       | Ready Pin Open Collector Voltage                      | 1.2        | 2.4 | 1.2                 | 2.4 | V     |

## AC Characteristics for AT17C010A/512A When Cascading

$V_{CC} = 5V \pm 5\%$  Commercial /  $V_{CC} = 5V \pm 10\%$  Ind./Mil.

| Symbol          | Description              | Commercial |     | Industrial/Military |     | Units |
|-----------------|--------------------------|------------|-----|---------------------|-----|-------|
|                 |                          | Min        | Max | Min                 | Max |       |
| $T_{CDF}^{(3)}$ | DCLK to Data Float Delay |            | 50  |                     | 50  | ns    |
| $T_{OCK}^{(2)}$ | DCLK to nCASC Delay      |            | 35  |                     | 40  | ns    |
| $T_{OCE}^{(2)}$ | CE to nCASC Delay        |            | 35  |                     | 35  | ns    |
| $T_{OOE}^{(2)}$ | OE to nCASC Delay        |            | 30  |                     | 30  | ns    |

- Notes:
1. Preliminary specifications for military operating range only.
  2. AC test load = 50 pF.
  3. Float delays are measured with 5 pF AC loads. Transition is measured  $\pm 200$  mV from steady state active levels.



### AC Characteristics for AT17C010A/512A

$V_{CC} = 3.3V \pm 10\%$  Commercial /  $V_{CC} = 3.3V \pm 10\%$  Ind./Mil

| Symbol          | Description   | Commercial |     | Industrial/Military |     | Units |
|-----------------|---|------------|-----|---------------------|-----|-------|
|                 |   | Min        | Max | Min                 | Max |       |
| $T_{OE}^{(2)}$  | OE to Data Delay                                      |            | 50  |                     | 55  | ns    |
| $T_{CE}^{(2)}$  | nCS to Data Delay                                     |            | 55  |                     | 60  | ns    |
| $T_{CAC}^{(2)}$ | CLK to Data Delay                                     |            | 60  |                     | 65  | ns    |
| $T_{OH}^{(2)}$  | Data Hold From nCS, OE, or DCLK                       | 0          |     | 0                   |     | ns    |
| $T_{DF}^{(3)}$  | nCS or OE to Data Float Delay                         |            | 50  |                     | 50  | ns    |
| $T_{LC}$        | CLK Low Time Slave Mode                               | 25         |     | 25                  |     | ns    |
| $T_{HC}$        | CLK High Time Slave Mode                              | 25         |     | 25                  |     | ns    |
| $T_{SCE}$       | nCS Setup Time to DCLK (to guarantee proper counting) | 35         |     | 40                  |     | ns    |
| $T_{HCE}$       | nCS Hold Time to DCLK (to guarantee proper counting)  | 0          |     | 0                   |     | ns    |
| $T_{HOE}$       | OE High Time (Guarantees Counter Is Reset)            | 20         |     | 20                  |     | ns    |
| $F_{MAX}^{(4)}$ | MAX Input Clock Frequency Slave Mode                  | 15         |     | 10                  |     | MHz   |
| $T_{LC}$        | CLK Low Time Master Mode                              | 30         | 300 | 30                  | 300 | ns    |
| $T_{HC}$        | CLK High Time Master Mode                             | 30         | 300 | 30                  | 300 | ns    |
| $V_{RDY}$       | Ready Pin Open Collector Voltage                      | 1.2        | 2.4 | 1.2                 | 2.4 | V     |

### AC Characteristics for AT17C010A/512A When Cascading

$V_{CC} = 3.3V \pm 10\%$  Commercial /  $V_{CC} = 3.3V \pm 10\%$  Ind./Mil.

| Symbol          | Description              | Commercial |     | Industrial/Military |     | Units |
|-----------------|--------------------------|------------|-----|---------------------|-----|-------|
|                 |                          | Min        | Max | Min                 | Max |       |
| $T_{CDF}^{(3)}$ | DCLK to Data Float Delay |            | 50  |                     | 50  | ns    |
| $T_{OCK}^{(2)}$ | DCLK to nCASC Delay      |            | 50  |                     | 55  | ns    |
| $T_{OCE}^{(2)}$ | CE to nCASC Delay        |            | 35  |                     | 40  | ns    |
| $T_{OOE}^{(2)}$ | OE to nCASC Delay        |            | 35  |                     | 35  | ns    |

- Notes:
1. Preliminary specifications for military operating range only.
  2. AC test load = 50 pF.
  3. Float delays are measured with 5 pF AC loads. Transition is measured  $\pm 200$  mV from steady state active levels.
  4. During cascade  $F_{MAX} = 12.5$  MHz



## Ordering Information - 5V Devices

| Memory Size (K)       | Ordering Code  | Package | Operation Range               |
|-----------------------|----------------|---------|-------------------------------|
| 512K <sup>(1)</sup>   | AT17C512A-10JC | 20J     | Commercial<br>(0°C to 70°C)   |
|                       | AT17C512A-10JI | 20J     | Industrial<br>(-40°C to 85°C) |
| 1M Bit <sup>(2)</sup> | AT17C010A-10JC | 20J     | Commercial<br>(0°C to 70°C)   |
|                       | AT17C010A-10JI | 20J     | Industrial<br>(-40°C to 85°C) |

## Ordering Information - 3.3V Devices

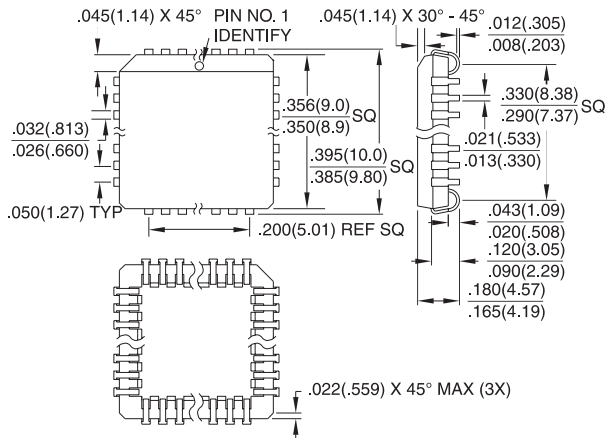
| Memory Size (K)       | Ordering Code   | Package | Operation Range               |
|-----------------------|-----------------|---------|-------------------------------|
| 512K <sup>(1)</sup>   | AT17LV512A-10JC | 20J     | Commercial<br>(0°C to 70°C)   |
|                       | AT17LV512A-10JI | 20J     | Industrial<br>(-40°C to 85°C) |
| 1M Bit <sup>(2)</sup> | AT17LV010A-10JC | 20J     | Commercial<br>(0°C to 70°C)   |
|                       | AT17LV010A-10JI | 20J     | Industrial<br>(-40°C to 85°C) |

- Notes: 1. Use 512K density parts to replace Altera EPC1441.  
2. Use 1M density parts to replace Altera EPC1

| Package Type |   |
|--------------|---|
| 20J          | 20-Lead, Plastic J-Leaded Chip Carrier (PLCC) |

Packaging Information

20J, 20-Lead, Plastic J-Leaded Chip Carrier (PLCC)  
 Dimensions in Inches and (Millimeters)  
 JEDEC STANDARD MS-018 AA



This datasheet has been downloaded from:

[www.DatasheetCatalog.com](http://www.DatasheetCatalog.com)

Datasheets for electronic components.