TPS60130, TPS60131, TPS60132, TPS60133
REGULATED 5-V, 300 mA HIGH EFFICIENCY CHARGE PUMP DC/DC CONVERTERS

SLVS258A – NOVEMBER 1999 – REVISED DECEMBER 1999

features

- **Up to 90% Efficiency From 2.7-V to 5.4-V Input Voltage Range Because of Special Switching Topology**
- **Up to 300-mA Output Current (TPS60130 and TPS60131)**
- **No Inductors Required, Low EMI**
- **Regulated 5-V ±4% Output**
- **Only Four External Components Required**
- **60-μA Quiescent Supply Current**
- **0.05-μA Shutdown Current**
- **Load Disconnected in Shutdown**
- **Space-Saving, Thermally-Enhanced PowerPAD™ Package**
- **Evaluation Module Available (TPS60130EVM–143)**

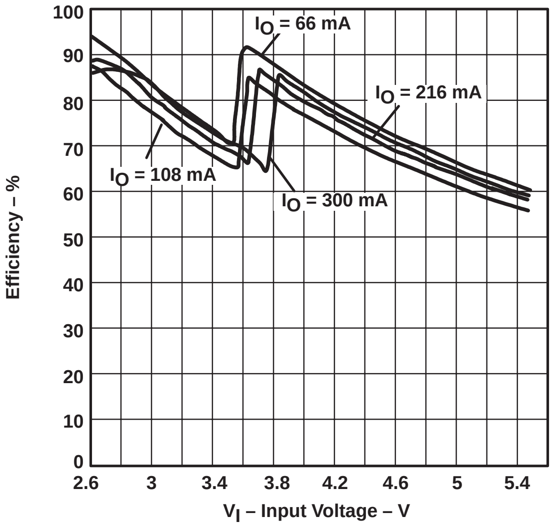
applications

- **Battery-Powered Applications**
- **Three Battery Cells to 5-V Conversion or Point-of-Use 3.3 V to 5-V Conversion**
- **LiIon Battery to 5-V Conversion**
- **Portable Instruments**
- **Battery-Powered Microprocessor Systems**
- **Backup-Battery Boost Converters**
- **PDA's, Organizers, Laptops**
- **Handheld Instrumentation**
- **Medical Instruments (e.g., Glucose Meters)**
- **PCMCIA and 5-V Smart Card Supply**

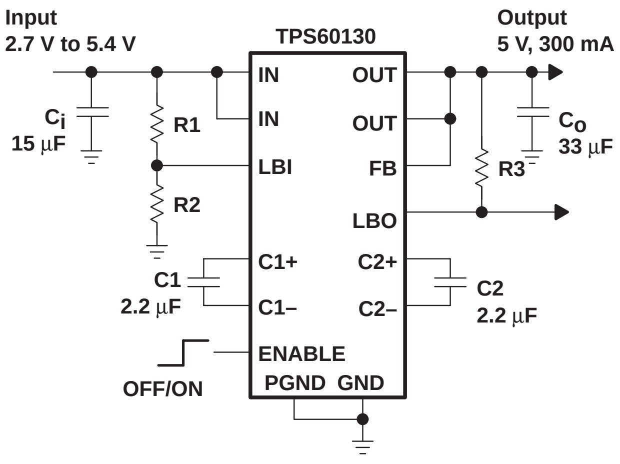
description

The TPS6013x step-up, regulated charge pumps generate a 5-V ±4% output voltage from a 2.7-V to 5.4-V input voltage (three alkaline, NiCd, or NiMH batteries or one Lithium or LiIon battery). The output current is 300 mA for the TPS60130/ TPS60131 and 150 mA for the TPS60132/ TPS60133, all from a 3-V input. Only four external capacitors are needed to build a complete high efficiency dc/dc charge pump converter. To achieve the high efficiency over a wide input voltage range, the charge pump automatically selects between a 1.5x or doubler conversion mode. From a 3-V input, all ICs can start with full load current.

efficiency (TPS60130, TPS60131)



typical operating circuit

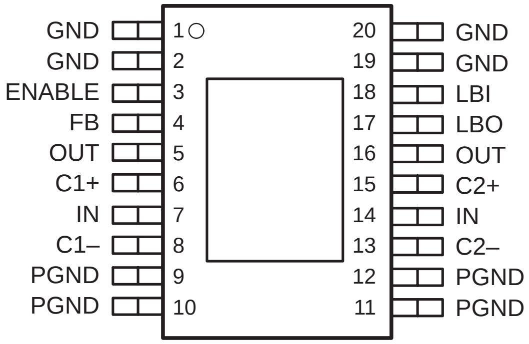


PowerPAD is a trademark of Texas Instruments Incorporated.

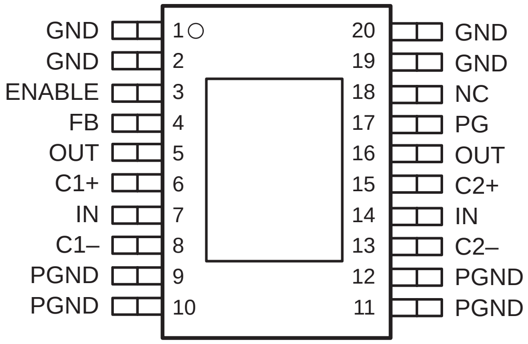
description (continued)

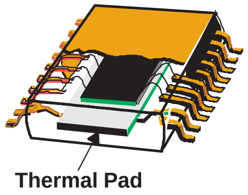
The devices feature the power-saving pulse-skip mode to extend battery life at light loads. TPS60130 and TPS60132 include a low-battery comparator; TPS60131 and TPS60133 feature a power-good output. The logic shut-down function reduces the supply current to 1 µA (max) and disconnects the load from the input. Special current-control circuitry prevents excessive current from being drawn from the battery during startup. This dc/dc converter requires no inductors and therefore EMI is of low concern. It is available in the small, thermally enhanced 20-pin PowerPAD™ package (PWP).

PWP PACKAGE
(TPS60130/TPS60132)
(TOP VIEW)



PWP PACKAGE
(TPS60131/TPS60133)
(TOP VIEW)





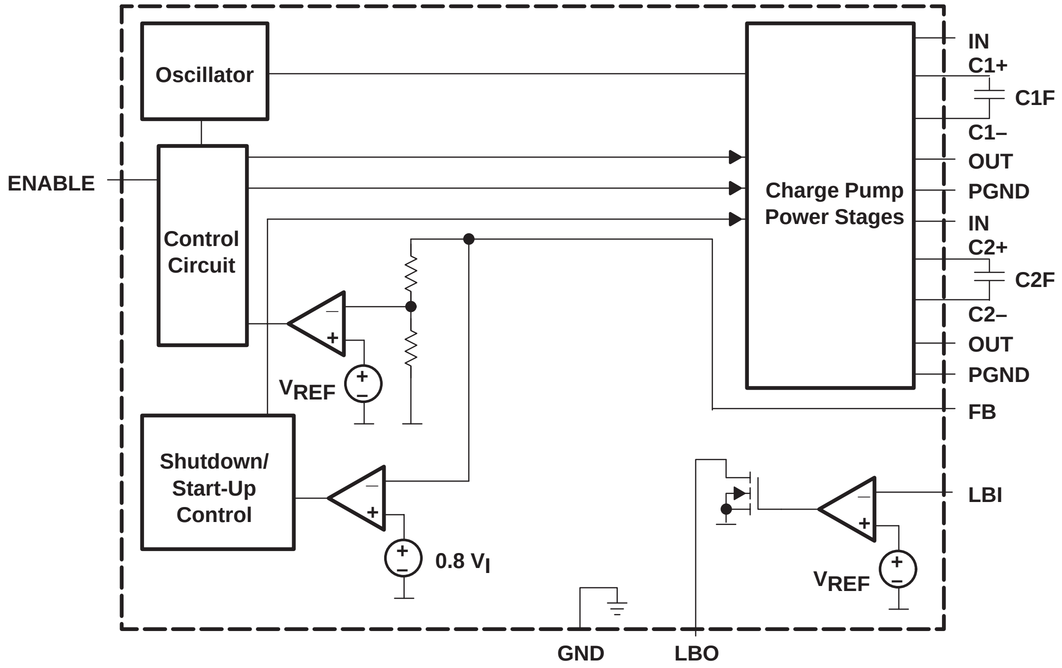
AVAILABLE OPTIONS

T_A	PART NUMBER[†]	PACKAGE		DEVICE FEATURES	
−40°C to 85°C	TPS60130PWP	PWP	20-Pin thermally enhanced TSSOP	3-cell to 5 V, 300 mA	Low battery detector
	TPS60131PWP				Power good detector
	TPS60132PWP			3-cell to 5 V, 150 mA	Low battery detector
	TPS60133PWP				Power good detector

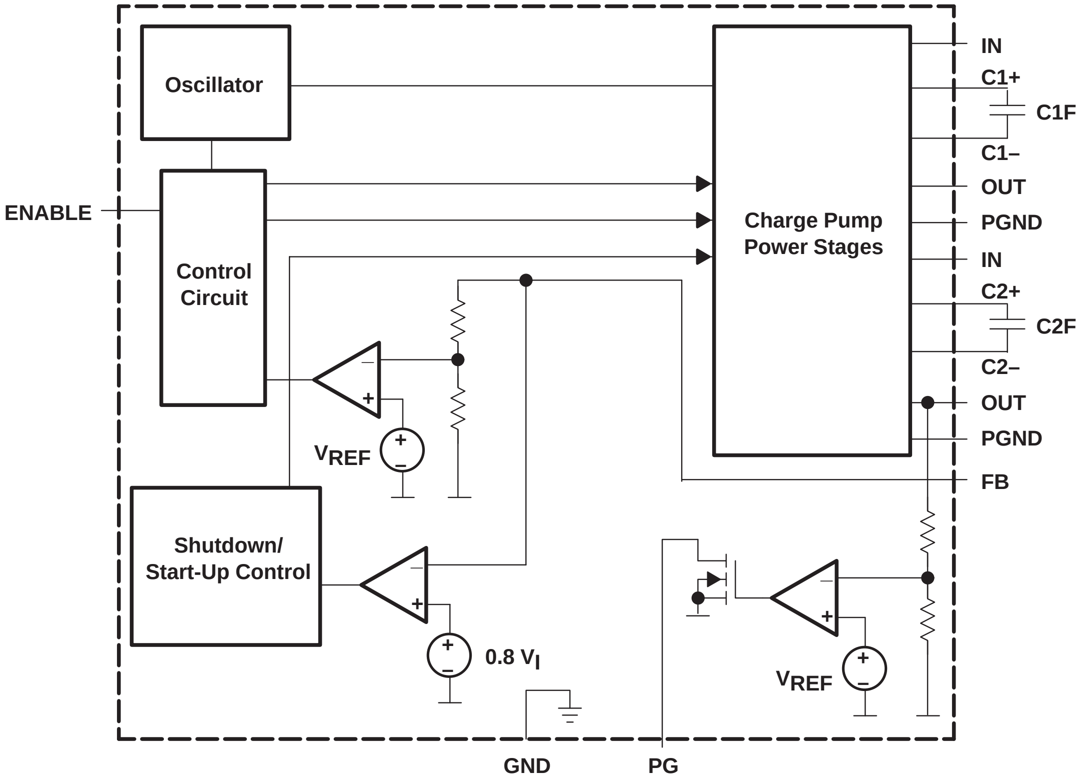
[†] The PWP package is available taped and reeled. Add R suffix to device type (e.g. TPS60130PWPR) to order quanities of 2000 devices per reel.

functional block diagram

TPS60130/TPS60132



TPS60131/TPS60133



Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
C1+	6		Positive terminal of the flying capacitor C1
C1–	8		Negative terminal of the flying capacitor C1
C2+	15		Positive terminal of the flying capacitor C2
C2–	13		Negative terminal of the flying capacitor C2
ENABLE	3	I	Enable input. Connect ENABLE to IN for normal operation. When ENABLE is a logic low, the device turns off and the supply current decreases to 0.05 μA. The output is disconnected from the input when the device is disabled.
FB	4	I	Feedback input. Connect FB to OUT as close to the load as possible to achieve best regulation. A resistive divider is on the chip to match internal reference voltage of 1.21 V.
GND	1, 2, 19, 20		Ground. Analog ground for internal reference and control circuitry. Connect to PGND terminals through a short trace.
IN	7,14	I	Supply input. Bypass IN to PGND with a capacitor that has half of the capacitance of the output capacitor. Connect both IN terminals together through a short trace.
LBO/PG	17	O	Low battery detector output (TPS60130 and TPS60132) or power good output (TPS60131 and TPS60133). Open drain output of the low battery or power good comparator. It can sink 1 mA. A 100-kΩ to 1-MΩ pullup resistor to OUT is recommended. Leave the terminal unconnected if the low battery or power good detector is not used.
LBI/NC	18	I	Low battery detector input (TPS60130 and TPS60132 only). The voltage at this input is compared to the internal 1.21 V reference voltage. Connect this terminal to ground if the low-battery detection function is not used. On the TPS60131 and TPS60133, this terminal is not connected.
OUT	5, 16	O	Regulated 5-V power output. Connect both OUT terminals through a short trace and bypass OUT to GND with the output filter capacitor C_O.
PGND	9–12		Power ground. Charge-pump current flows through this pin. Connect all PGND terminals together.

detailed description

operating principle

The TPS6013x charge pumps provide a regulated 5-V output from a 2.7-V to 5.4-V input. They deliver a maximum load current of 300 mA or 150 mA, respectively. Designed specifically for space-critical, battery-powered applications, the complete charge pump circuit requires four external capacitors. The circuit is optimized for efficiency over a wide input voltage range.

The TPS6013x charge pumps consist of an oscillator, a 1.21-V bandgap reference, an internal resistive feedback circuit, an error amplifier, high current MOSFET switches, a shutdown/startup circuit, a low-battery or power-good comparator, and a control circuit (see functional block diagrams).

The device consists of two single-ended charge pumps. These charge pumps are automatically configured to amplify the input voltage with a conversion factor of 1.5 or 2. The conversion ratio is dependent on the input voltage and load current. This assures high efficiency over a wide input voltage range and is further described in the *adaptive mode switching* section below.

adaptive mode switching

The ON-resistance of the MOSFETs that are in the charge path of the flying capacitors is regulated when the charge pump operates in voltage doubler mode. It is changed depending on the output voltage that is fed back into the control loop. This way, the time-constant during the charging phase can be modified and increased versus a time-constant for fully switched-on MOSFETs. The ON-resistance of both switches and the capacitance of the flying capacitor define the time constant. The MOSFET switches in the discharge path of the charge pump are always fully switched on to their minimum $r_{DS(on)}$. With the time-constant during charge phase being bigger than the time constant in discharge phase, the voltage on the flying capacitors stabilizes to the lowest possible value necessary to get a stable V_O.

adaptive mode switching (continued)

The voltage on the flying capacitors is measured and compared with the supply voltage V_I. If the voltage across the flying capacitors is smaller than half of the supply voltage, then the charge pump switches into the 1.5x conversion-mode. The charge pump switches back from a 1.5x conversion-mode to a voltage doubler mode if the load current in 1.5x conversion-mode can no more be delivered.

With this control mode the device runs in *doubler* -mode at low V_I and in 1.5x conversion-mode at high V_I to optimize the efficiency. The most desirable transfer mode is automatically selected depending on both V_I and I_L. This means that at light loads the device selects the 1.5x conversion-mode already at smaller supply voltages than at heavy loads.

The TPS60130 output voltage is regulated using the *ACTIVE-CYCLE*-regulation. An active cycle controlled charge pump utilizes two methods to control the output voltage. At high load currents it varies the on-resistances of the internal switches and keeps the ratio ON/OFF time (=frequency) constant. That means the charge pump runs at a fixed frequency. It also keeps the output voltage ripple as low as in linear-mode. At light loads the internal resistance and also the amount of energy transferred per pulse is fixed and the charge pump regulates the voltage by means of a variable ratio of ON-to-OFF time. In this operating point it runs like a skip mode controlled charge pump with a very high internal resistance, which also enables a low ripple in this operation mode. Since the charge pump does effectively switch at lower frequencies at light loads, it achieves a low quiescent current.

pulse-skip mode

In pulse-skip mode the error amplifier disables switching of the power stages when it detects an output higher than 5 V. The oscillator halts and the IC then skips switching cycles until the output voltage drops below 5 V. The error amplifier reactivates the oscillator and starts switching the power stages again. The pulse-skip regulation mode minimizes operating current because it does not switch continuously and deactivates all functions except bandgap reference, error amplifier, and low-battery/power-good comparator when the output is higher than 5 V. When switching is disabled from the error amplifier, the load is also isolated from the input. In pulse-skip mode, a special current control circuitry, limits the peak current. This assures moderate output voltage ripple and also prevents the device from drawing excessive current spikes out of the battery.

start-up procedure

During start-up, i.e. when ENABLE is set from logic low to logic high, the output capacitor is charged up, with a limited current, until the output voltage V_O reaches $0.8 \times V_I$. When the start-up comparator detects this voltage limit, the IC begins switching. This start-up charging of the output capacitor assures a short start-up time and eliminates the need of a Schottky diode between IN and OUT. The IC starts with a maximum load, which is defined by a 16-Ω or 33-Ω resistor, respectively.

shutdown

Driving ENABLE low places the device in shutdown mode. This disables all switches, the oscillator, and control logic. The device typically draws 0.05 µA (1 µA max) of supply current in this mode. Leakage current drawn from the output is as low as 1 µA max. The device exits shutdown once ENABLE is set to a high level. The typical no-load shutdown exit time is 10 µs. When the device is in shutdown, the load is isolated from the input.

undervoltage lockout

The TPS6013x devices have an undervoltage lockout feature that deactivates the device and places it in shutdown mode when the input voltage falls below 1.6 V.

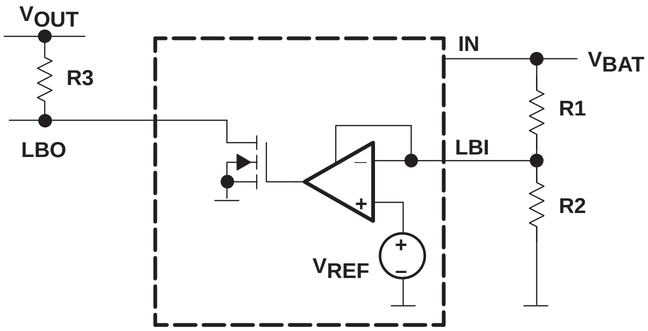
low-battery detector (TPS60130 and TPS60132)

The internal low-battery comparator trips at 1.21 V ±5% when the voltage on pin LBI ramps down. The battery voltage at which the comparator initiates a low battery warning at the LBO output can easily be programmed with a resistive divider as shown in Figure 3. The sum of resistors R1 and R2 is recommended to be in the 100-kΩ to 1-MΩ range.

low-battery detector (TPS60130 and TPS60132) (continued)

LBO is an open drain output. An external pullup resistor to OUT, in the 100-kΩ to 1-MΩ range is recommended. During start-up, the LBO output signal is invalid for the first 500 µs. LBO is high impedance when the device is disabled.

If the low-battery comparator function is not used, connect LBI to ground and leave LBO unconnected.



$$V_{TRIP} = 1.21\ V \times \left(1 + \frac{R1}{R2}\right)$$

Figure 1. Programming of the Low-Battery Comparator Trip Voltage

Formulas to calculate the resistive divider for low battery detection, with V_{LBI} = 1.15 V – 1.27 V:

$$R2 = 1\ M\Omega \times \frac{V_{LBI}}{V_{BAT}}$$

$$R1 = 1\ M\Omega - R2$$

Formulas to calculate the minimum and maximum battery voltage that triggers the low battery detector:

$$V_{BAT(min)} = V_{LBI(min)} \times \frac{R1_{(min)} + R2_{(max)}}{R2_{(max)}}$$

$$V_{BAT(max)} = V_{LBI(max)} \times \frac{R1_{(max)} + R2_{(min)}}{R2_{(min)}}$$

Table 1. Recommended Values for the Resistive Divider from the E96 Series (±1%), V_{LBI} = 1.15 V – 1.27 V

V_{BAT}/V	R_1/kΩ	R_2/kΩ	$V_{BAT(MIN)}$/V		$V_{BAT(MAX)}$/V	
2.7	562	453	2.548	–5.61%	2.877	6.57%
2.8	576	442	2.619	–6.47%	2.958	5.66%
2.9	590	422	2.726	–6.00%	3.081	6.26%
3.0	590	402	2.804	–6.53%	3.172	5.72%
3.1	604	383	2.928	–5.56%	3.313	6.88%
3.2	619	374	3.016	–5.76%	3.414	6.70%
3.3	649	374	3.106	–5.88%	3.518	6.62%

A 100 nF bypass capacitor should be connected in parallel to R2 if large line transients are expected. These voltage drops can inadvertently trigger the low-battery comparator and produce a wrong low-battery warning signal at the LBO pin.

Power-Good detector (TPS60131 and TPS60133)

The PG pin is an open-drain output that is pulled low when the output is out of regulation. When the output voltage rises to about 90% of its nominal voltage, power-good output is released. PG is high impedance when the device is disabled. An external pullup resistor must be connected between PG and OUT. The pullup resistor should be in the 100 kΩ to 1 MΩ range. If the power-good function is not used, the PG-pin should remain unconnected.

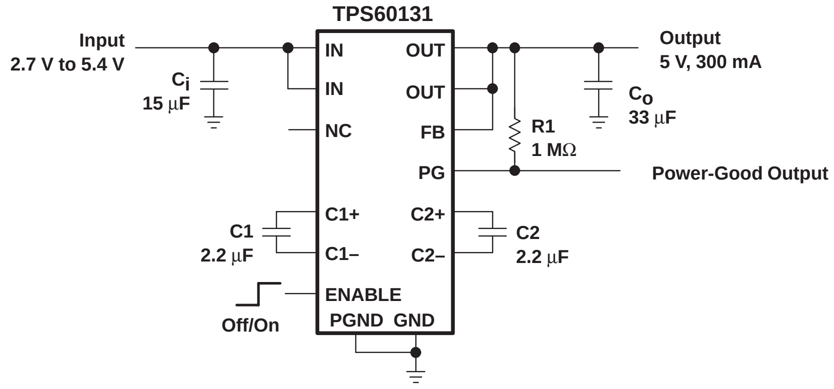


Figure 2. Typical Operating Circuit Using Power-Good Comparator

absolute maximum ratings (see Note 1)†

Input voltage range, V_I (IN, OUT, ENABLE, FB, LBI, LBO/PG)		–0.3 V to 5.5 V
Differential input voltage, V_{ID} (C1+, C2+ to GND)		–0.3 V to (V_O + 0.3 V)
Differential input voltage, V_{ID} (C1–, C2– to GND)		–0.3 V to (V_I + 0.3 V)
Continuous total power dissipation		See Dissipation Rating Table
Continuous output current:	TPS60130, TPS60131	400 mA
	TPS60132, TPS60133	200 mA
Storage temperature range, T_{stg}		–55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10s		260°C
Maximum junction temperature, T_J		150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: $V_{(ENABLE)}$, $V_{(LBI)}$ and $V_{(LBO/PG)}$ can exceed V_I up to the maximum rated voltage without increasing the leakage current drawn by these inputs.

DISSIPATION RATING TABLE FREE-AIR TEMPERATURE (see Figure 1)

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
PWP	700 mW	5.6 mW/°C	448 mW	364 mW

DISSIPATION RATING TABLE CASE TEMPERATURE (see Figure 2)

PACKAGE	$T_C \leq 62.5°C$ POWER RATING	DERATING FACTOR ABOVE $T_C = 62.5°C$	$T_C = 70°C$ POWER RATING	$T_C = 85°C$ POWER RATING
PWP	25 mW	285.7 mW/°C	22.9 mW	18.5 mW

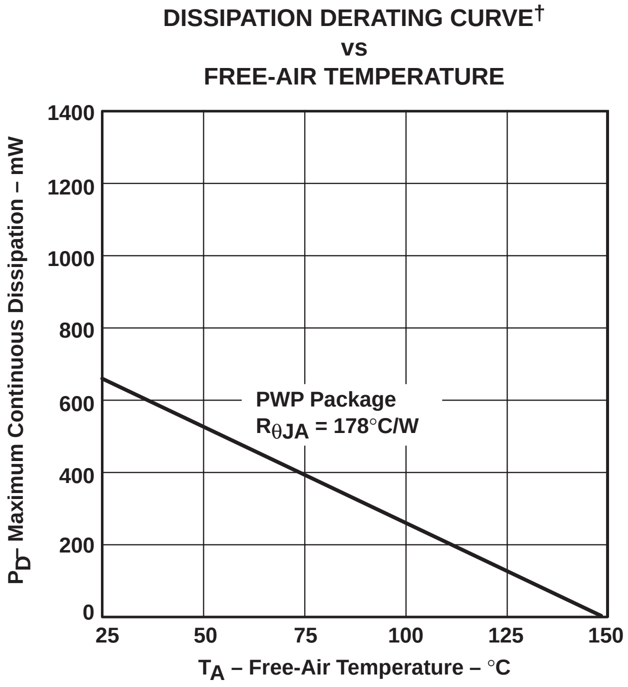


Figure 3

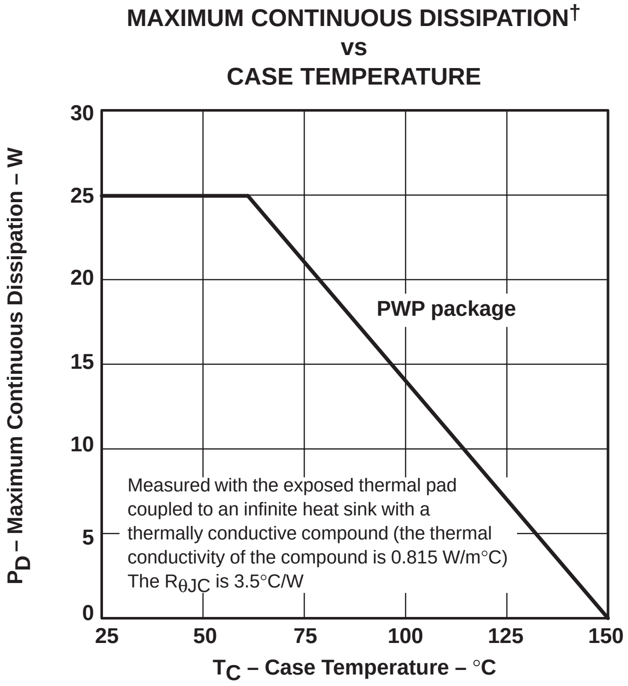


Figure 4

[†] Dissipation rating tables and figures are provided for maintenance of junction temperature at or below absolute maximum temperature of 150°C. It is recommended not to exceed a junction temperature of 125°C.

recommended operating conditions

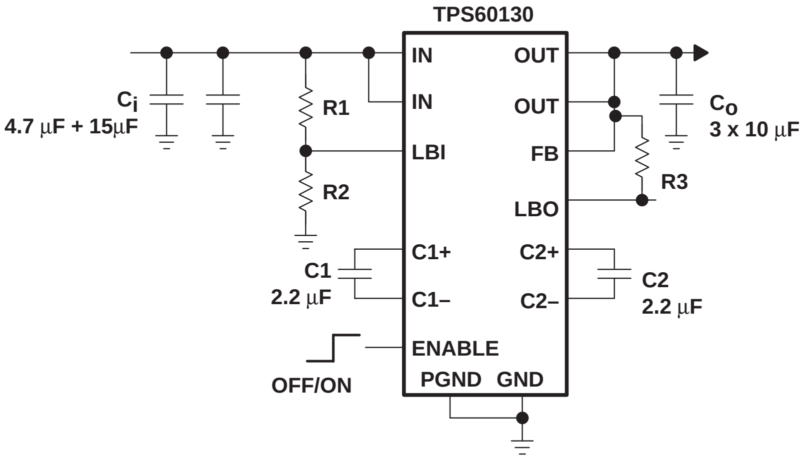
		MIN	MAX	UNIT
Input voltage, V_I		2.7	5.4	V
Output current, I_O	TPS60130 and TPS60131		300	mA
	TPS60132 and TPS60133		150	
Operating junction temperature, T_J			125	°C

electrical characteristics at C_I = 15 µF, $C_{1F} = C_{2F}$ = 2.2 µF, C_O = 33 µF, T_C = –40°C to 85°C, V_I = 3 V, $V_{(FB)} = V_O$ and $V_{(ENABLE)} = V_I$ (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_I	Input voltage			2.7		5.4	V
$V_{(UVLO)}$	Input undervoltage lockout threshold		T_C = 25°C		1.6	1.8	V
$I_{O(MAX)}$	Maximum output current	TPS60130/TPS60131		300			mA
		TPS60132/TPS60133		150			mA
V_O	Output voltage		2.7 V < V_I < 3 V, 0 < I_O < $I_{O(MAX)}$/2, T_C = 0°C to 70°C	4.8		5.2	V
			3 V < V_I < 5 V, 0 < I_O < $I_{O(MAX)}$	4.8		5.2	V
			5 V < V_I < 5.4 V, 0 < I_O < $I_{O(MAX)}$	4.8		5.25	V
$I_{lkg(OUT)}$	Output leakage current		V_I = 3.6 V, $V_{(ENABLE)}$ = 0 V			1	µA
I_Q	Quiescent current (no-load input current)		V_I = 3.6 V		60	100	µA
$I_{Q(SDN)}$	Shutdown supply current		V_I = 3.6 V, $V_{(ENABLE)}$ = 0 V		0.05	1	µA
$f_{OSC(INT)}$	Internal switching frequency			210	320	450	kHz
V_{IL}	Enable input voltage low		V_I = 2.7 V			0.3 x V_I	V
V_{IH}	Enable input voltage high		V_I = 5.4 V	0.7 x V_I			V
$I_{lkg(ENABLE)}$	Enable input leakage current		$V_{(ENABLE)}$ = V_{GND} or V_I		0.01	0.1	µA
	Output load regulation		V_I = 3.8 V, 1 mA < I_O(max) T_C = 25°C		0.002%		mA
	Output line regulation		3 V < V_I < 5 V, I_O = 150 mA, T_C = 25°C		0.2		%/V
	Short circuit current limit		V_I = 3.6 V, V_O = 0 V, T_C = 25°C		115		mA
$V_{(LBITRIP)}$	LBI trip voltage	TPS60130/TPS60132	V_I = 2.7 V to 3.3 V, Hysteresis 0.8% for rising LBI, T_C = 0°C to 70°C	1.15	1.21	1.27	V
$I_{I(LBI)}$	LBI input current	TPS60130/TPS60132	$V_{(LBI)}$ = 1.3 V			100	nA
$V_{O(LBO)}$	LBO output voltage low (see Note 2)	TPS60130/TPS60132	$V_{(LBI)}$ = 0 V, $I_{(LBO)(SINK)}$ = 1 mA			0.4	V
$I_{lkg(LBO)}$	LBO leakage current	TPS60130/TPS60132	$V_{(LBI)}$ = 1.3 V, $V_{(LBO)}$ = 5 V		0.01	0.1	µA
$V_{(PGTRIP)}$	Power-good trip voltage	TPS60131/TPS60133	T_C = 0°C to 70°C	0.86 × V_O	0.9 × V_O	0.94 × V_O	V
$V_{hys(PG)}$	Power–good trip voltage hysteresis	TPS60131/TPS60133	V_O ramping negative, T_C = 0°C to 70°C		0.8%		
$V_{O(PG)}$	Power-good output voltage low (see Note 2)	TPS60131/TPS60133	V_O = 0 V, $I_{(PG)(SINK)}$ = 1 mA			0.4	V
$I_{lkg(PG)}$	Power-good leakage current	TPS60131/TPS60133	V_O = 5 V, $V_{(PG)}$ = 5 V		0.01	0.1	µA

NOTE 2: During start-up the LBO and PG output signal is invalid for the first 500 µs.

PARAMETER MEASUREMENT INFORMATION



Used capacitor types:
C_i: Ceramic, X7R
C_O: Ceramic, X7R
C1, C2: Ceramic, X7R

Figure 5. Circuit Used For Typical Characteristics Measurements

TYPICAL CHARACTERISTICS

Table of Graphs

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TYPICAL CHARACTERISTICS

TPS60130
EFFICIENCY
vs
OUTPUT CURRENT

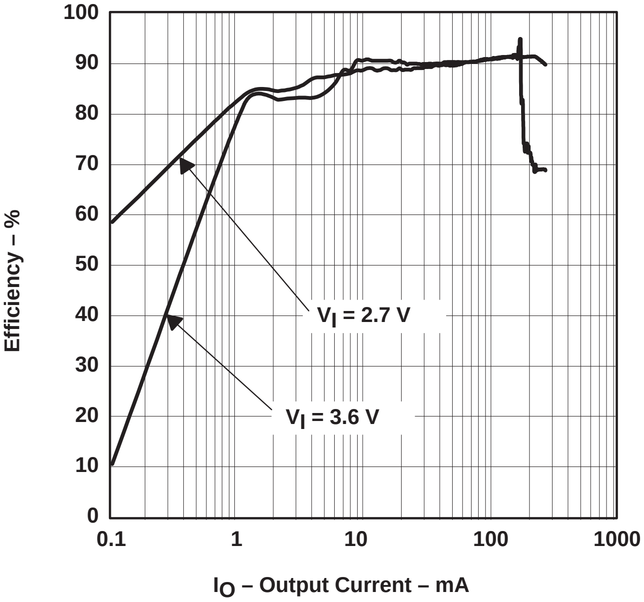


Figure 6

TPS60132
EFFICIENCY
vs
OUTPUT CURRENT

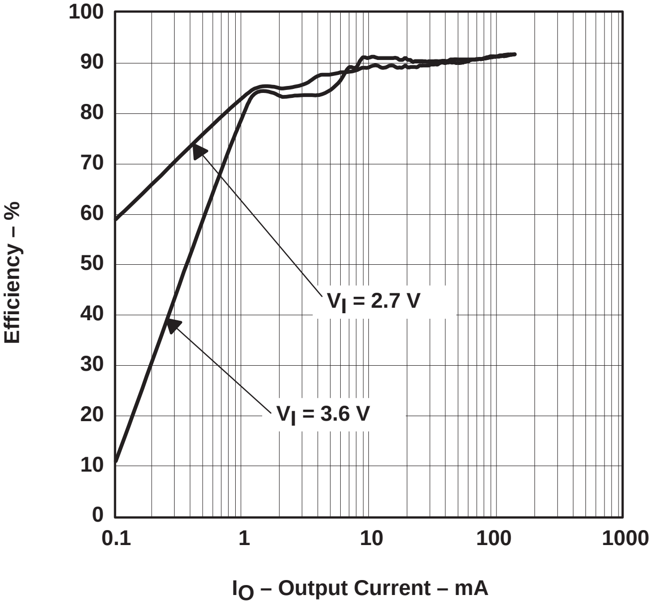


Figure 7

TPS60130
EFFICIENCY
vs
INPUT VOLTAGE

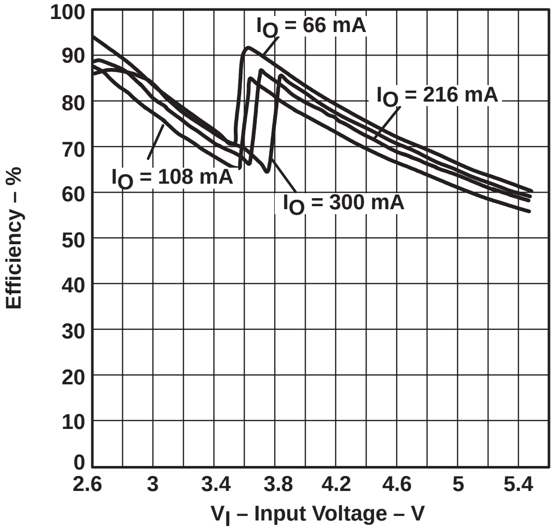


Figure 8

TPS60132
EFFICIENCY
vs
INPUT VOLTAGE

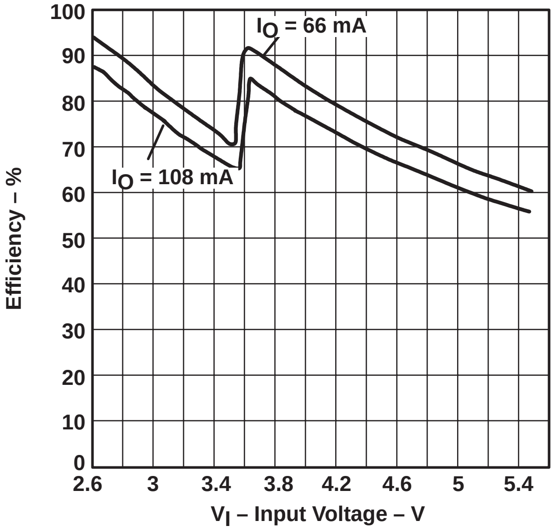


Figure 9

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs INPUT VOLTAGE

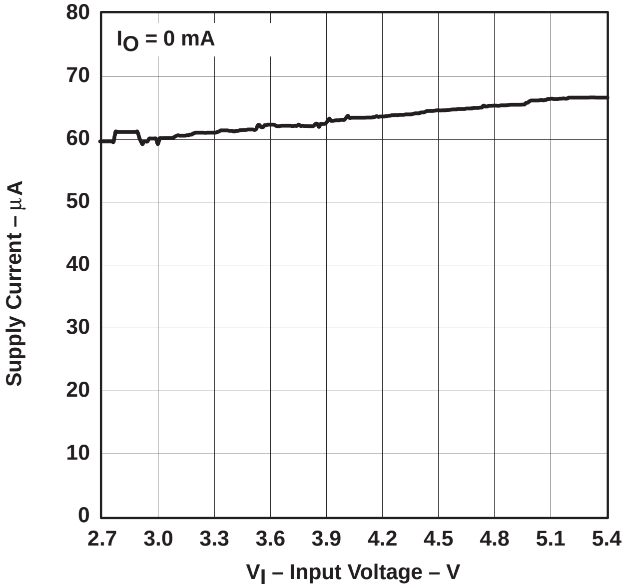


Figure 10

TPS60132 OUTPUT VOLTAGE vs OUTPUT CURRENT

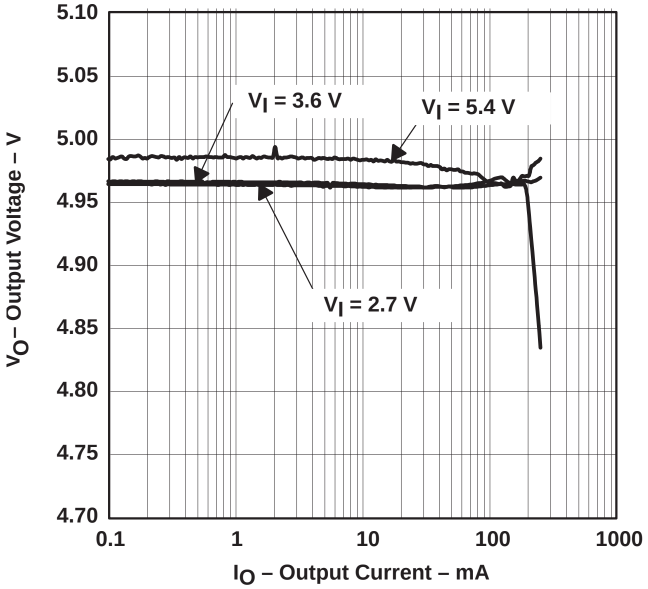


Figure 11

TPS60132 OUTPUT VOLTAGE vs OUTPUT CURRENT

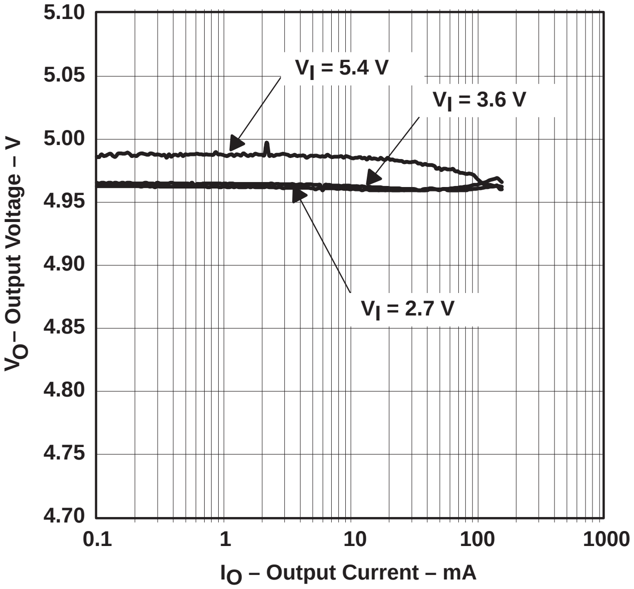


Figure 12

TPS60130 OUTPUT VOLTAGE vs INPUT VOLTAGE

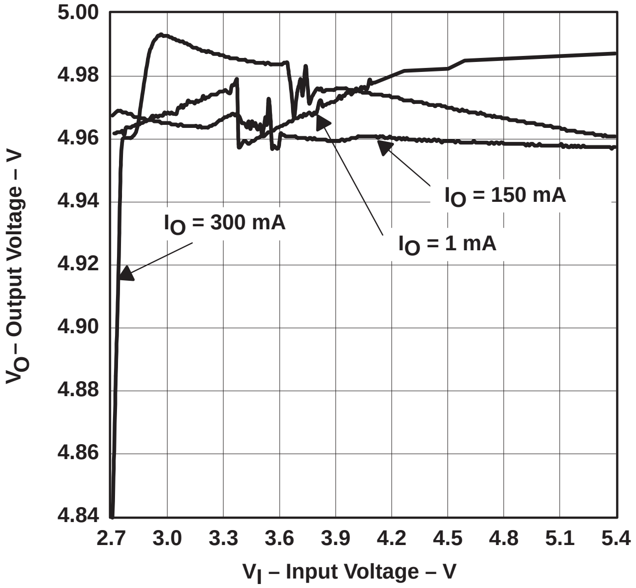


Figure 13

TYPICAL CHARACTERISTICS

TPS60132
OUTPUT VOLTAGE
vs
INPUT VOLTAGE

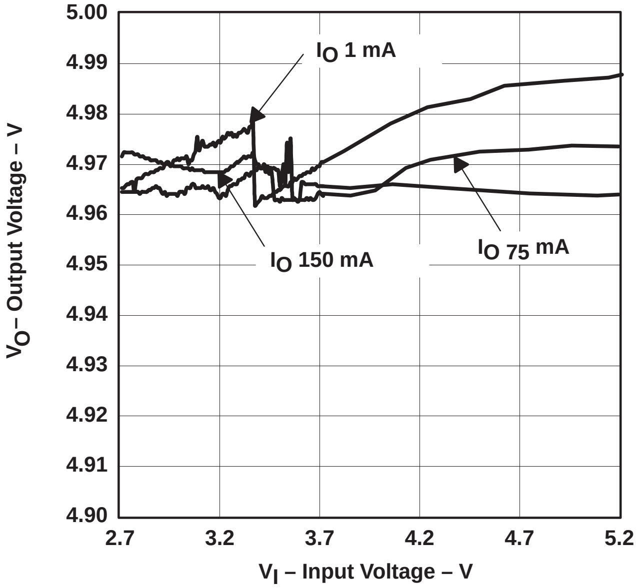


Figure 14

OUTPUT VOLTAGE RIPPLE
vs
TIME

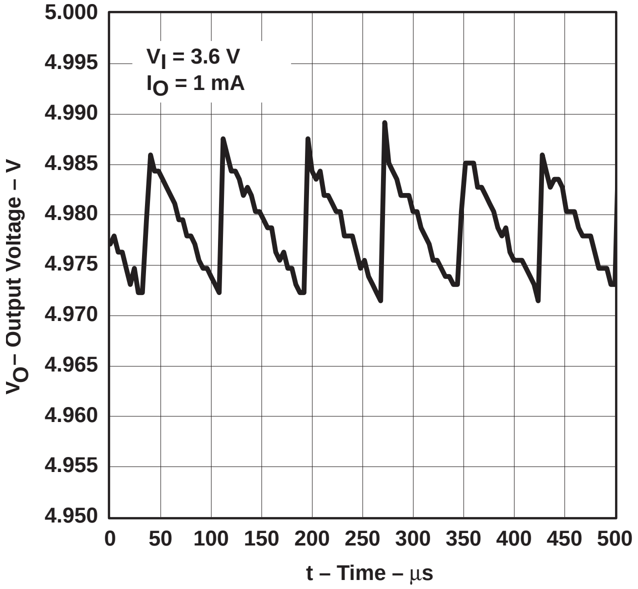


Figure 15

OUTPUT VOLTAGE RIPPLE
vs
TIME

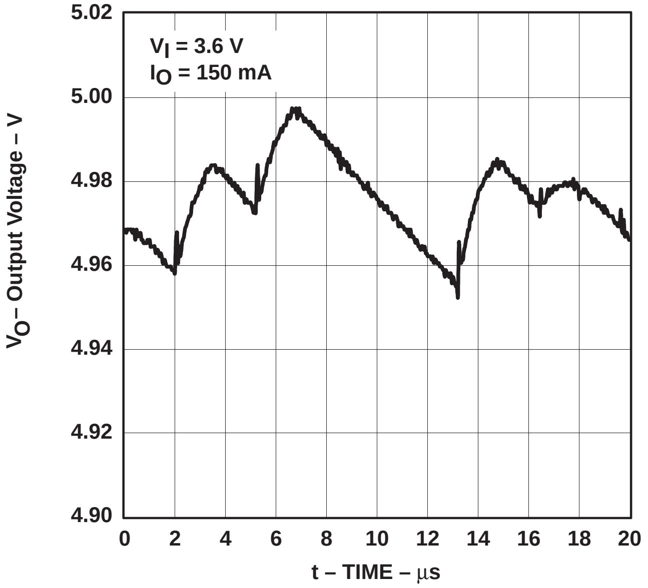


Figure 16

OUTPUT VOLTAGE RIPPLE
vs
TIME

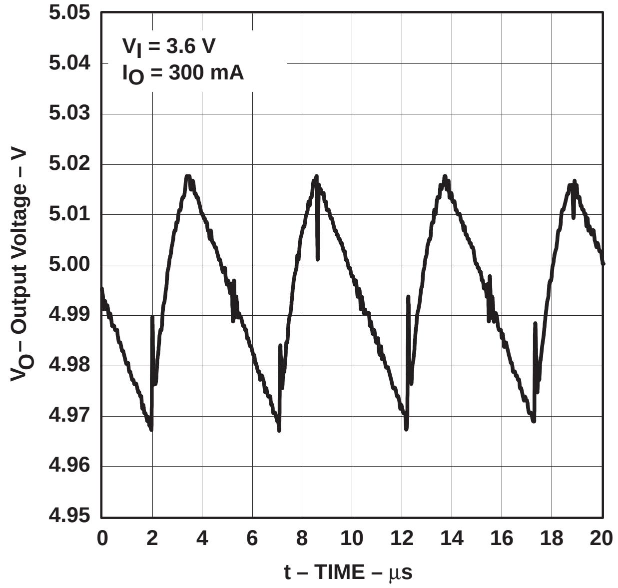


Figure 17

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE RIPPLE AMPLITUDE
vs
INPUT VOLTAGE

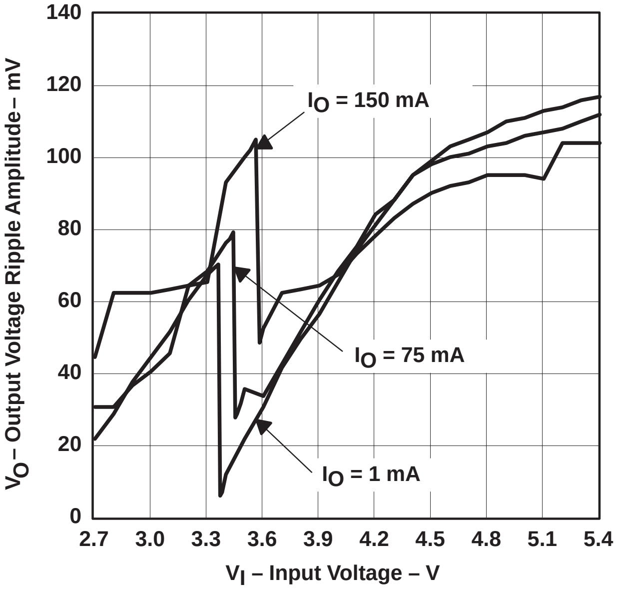


Figure 18

OSCILLATOR FREQUENCY
vs
INPUT VOLTAGE

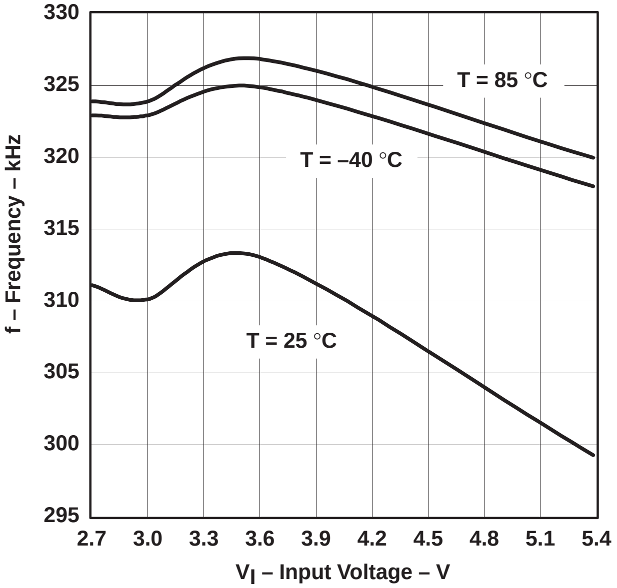


Figure 19

LOAD TRANSIENT RESPONSE

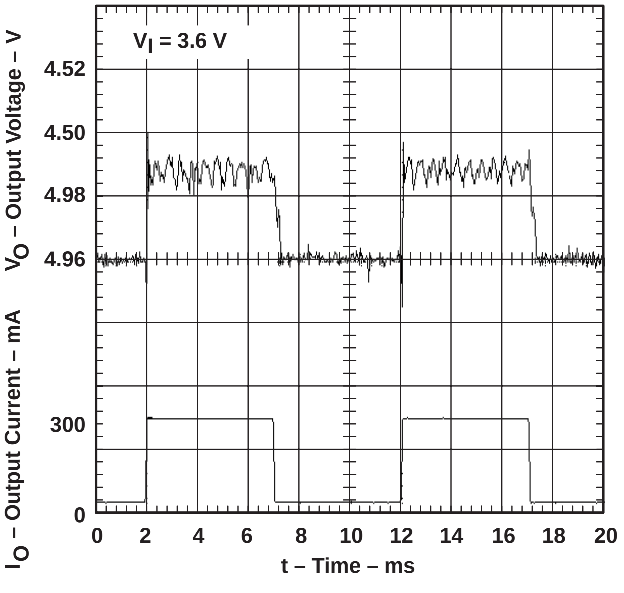


Figure 20

LINE TRANSIENT RESPONSE

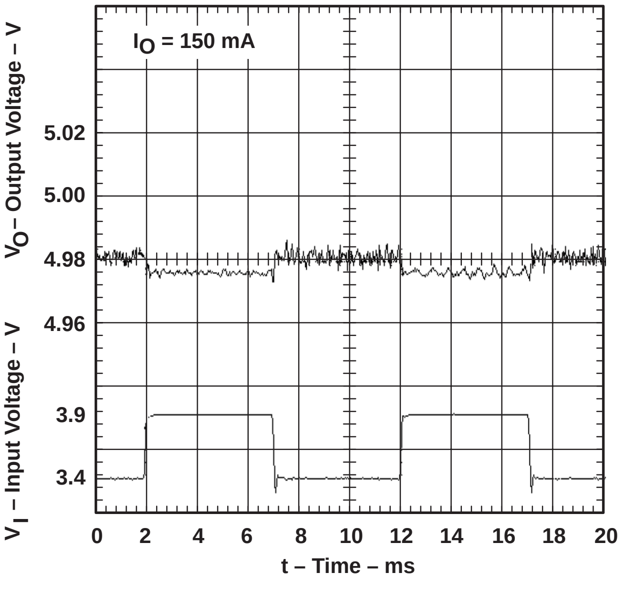


Figure 21

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
TIME
(START-UP TIMING)

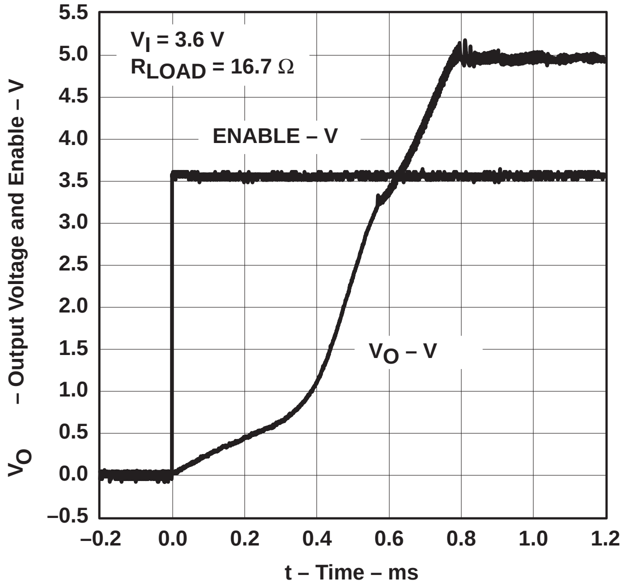


Figure 22

APPLICATION INFORMATION

capacitor selection

The TPS6013x charge pumps require only four external capacitors as shown in the basic application circuit. Their capacitance values and types are closely linked to the output current and output noise/ripple requirements. For lowest noise and ripple, low ESR (< 0.1 Ω) capacitors should be used for input and output capacitors.

The input capacitor improves system efficiency by reducing the input impedance. It also stabilizes the input current of the power source. The input capacitor should be chosen according to the power supply used and the distance from power source to the converter IC. The input capacitor also has an impact on the output voltage ripple. The lower the ESR of the input capacitor C_i, the lower is the output ripple. C_i is recommended to be about two to four times as large as $C_{(xF)}$.

The output capacitor C_o can be selected from 5-times to 50-times larger than $C_{(xF)}$, depending on the ripple tolerance. The larger C_o, the lower will be the output voltage ripple. C_i and C_o can be either ceramic or low-ESR tantalum; aluminum capacitors are not recommended.

Generally, the flying capacitors $C_{(xF)}$ will be the smallest. Only ceramic capacitors are recommended, due to their low ESR and because they retain their capacitance at the switching frequency. Because the device regulates the output voltage using the pulse-skip technique, a larger flying capacitor will lead to a higher output voltage ripple if the size of the output capacitor is not increased. Be aware that, depending on the material used to manufacture them, ceramic capacitors might lose their capacitance over temperature. Ceramic capacitors of type X7R or X5R material will keep their capacitance over temperature and voltage, whereas Z5U or Y5V-type capacitors will decrease in capacitance. Table 2 lists recommended capacitor values.

capacitor selection (continued)

Table 2. Recommended Capicator Values

PART	V_I (V)	I_O (mA)	C_i (µF)		$C_{(xF)}$ (µF) CERAMIC (X7R)	C_O (µF)		$V_{PP(TYP)}$ (V)
			TANTALUM	CERAMIC (X7R)		TANTALUM	CERAMIC (X7R)	
TPS60130 TPS60131	3.6	225		10	2.2	22	4.7	90
							22	60
		300		10	2.2	33	4.7	120
							22 and 10 in parallel	45
TPS60132 TPS60133	3.6	75		4.7	1		10	
		150	4.7	2.2		15	22	100
				4.7			22	90

The TPS6013x devices are charge pumps that regulate the output voltage using pulse-skip regulation mode. The output voltage ripple is therefore dependent on the values and the ESR of the input, output and flying capacitors. The only possibility to reduce the output voltage ripple is to choose the appropriate capacitors. The lowest output voltage ripple can be achieved using ceramic capacitors because of their low ESR and their frequency characteristic.

Ceramic capacitors typically have an ESR that is more than 10 times lower than tantalum capacitors and they retain their capacitance at frequencies more than 10 times higher than tantalum. Many different tantalum capacitors act as an inductance for frequencies higher than 200 kHz. This behavior increases the output voltage ripple. Therefore the best choice for a minimized ripple is the ceramic capacitor. For applications that do not need a higher performance in output voltage ripple, tantalum capacitors with a low ESR are a possibility for input and output capacitor, but a ceramic capacitor should be connected in parallel. Be aware that the ESR of tantalum capacitors is indirectly proportional to the physical size of the capacitor.

Table 2 is a good starting point for choosing the capacitors. If the output voltage ripple is too high for the application, it can be improved by selecting the appropriate capacitors. The first step is to increase the capacitance at the output. If the ripple is still too high, the second step would be to increase the capacitance at the input.

For the TPS60130 and TPS60131, the smallest board space can be achieved using Sprague’s 595D-series tantalum capacitors for input and output. However, high capacitance ceramic capacitors will become competitive in package size soon.

The smallest size for the lower-current devices TPS60132 and TPS60133 can be achieved using the suggested ceramic capacitors.

APPLICATION INFORMATION

capacitor selection (continued)

Tables 3 and 4 lists the manufacturers of recommended capacitors. In most applications surface-mount tantalum capacitors will be the right choice. However, ceramic capacitors provide the lowest output voltage ripple due to their typically lower ESR.

Table 3. Recommended Capacitors

MANUFACTURER	PART NUMBER	CAPACITANCE	CASE SIZE	TYPE
Taiyo Yuden	LMK212BJ105KG–T	1 µF	0805	Ceramic
	LMK212BJ225MG–T	2.2 µF	0805	Ceramic
	LMK316BJ475KL–T	4.7 µF	1206	Ceramic
	LMK325BJ106MN–T	10 µF	1210	Ceramic
	LMK432BJ226MM–T	22 µF	1812	Ceramic
AVX	0805ZC105KAT2A	1 µF	0805	Ceramic
	1206ZC225KAT2A	2.2 µF	1206	Ceramic
	TPSC475035R0600	4.7 µF	Case C	Tantalum
	TPSC156025R0500	15 µF	Case C	Tantalum
	TPSC336010R0375	33 µF	Case C	Tantalum
Sprague	595D156X0016B2T	15 µF	Case B	Tantalum
	595D226X0016B2T	22 µF	Case B	Tantalum
	595D336X0016B2T	33 µF	Case B	Tantalum
	595D336X0016C2T	33 µF	Case C	Tantalum
Kemet	T494C156K010AS	15 µF	Case C	Tantalum
	T494C226K010AS	22 µF	Case C	Tantalum
	T494C336K010AS	33 µF	Case C	Tantalum

NOTE: Case code compatibility with EIA 535BAAC and CECC30801 molded chips.

Table 4. Recommended Capacitor Manufacturers

MANUFACTURER	CAPACITOR TYPE	INTERNET SITE
Taiyo Yuden	X7R/X5R ceramic	http://www.t–yuden.com/
AVX	X7R/X5R ceramic TPS-series tantalum	http://www.avxcorp.com/
Sprague	595D-series tantalum 593D-series tantalum	http://www.vishay.com/
Kemet	T494-series tantalum	http://www.kemet.com/

power dissipation

The power dissipated in the TPS6013x depends on output current and the mode of operation (1.5x or doubler voltage conversion mode). It is described by the following equation:

$P_{DISS} = \left(\frac{1}{\eta} - 1\right) V_O \times I_O$ (Efficiency η mainly depends on V_I and also on I_O. See efficiency graphs.)

P_{DISS} must be less than that allowed by the package rating. See the absolute maximum ratings for 20-pin PWP package power-dissipation limits and deratings.

APPLICATION INFORMATION

board layout

Careful board layout is necessary due to the high transient currents and switching frequency of the converter. All capacitors should be soldered in close proximity to the IC. Connect ground and power ground pins through a short, low-impedance trace. A PCB layout proposal for a two-layer board is given in Figure 23. The bottom layer of the board carries only ground potential for best performance. The layout also provides improved thermal performance as the exposed lead frame is soldered to the PCB.

An evaluation module for the TPS60130 is available and can be ordered under product code TPS60130EVM-143. The EVM uses the layout shown in Figure 23.

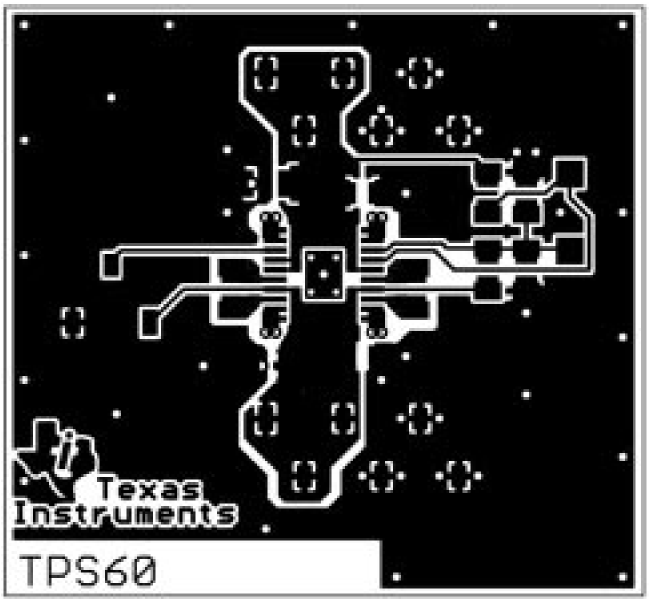


Figure 23. Recommended PCB Layout for TPS6013X

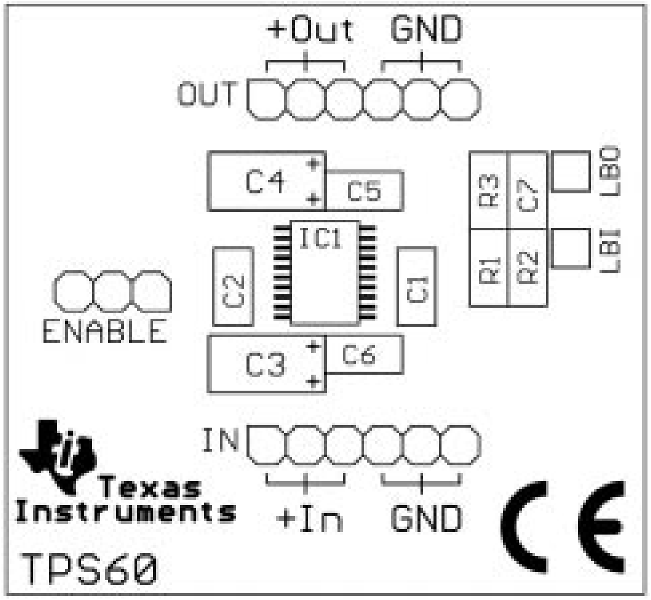


Figure 24. Component Placement for TPS6013X EVM

Table 5. Component Identification

IC1	TPS6013x
C1, C2	Flying capacitors
C3, C6	Input capacitors
C4, C5	Onput capacitors
C7	Stabilization capacitor for LBI
R1, R2	Resistive divider for LBI
R3	Pullup resistor for LBO

The best performance of the converter is achieved with the additional bypass capacitors C5 and C6 at input and output. Capacitor C7 should be included if the large line transients are expected. The capacitors are not required. They can be omitted in most applications.

APPLICATION INFORMATION

application proposals

paralleling of two TPS6013x to deliver 600 mA total output current

Two TPS60130x devices can be connected in parallel to yield higher load currents. The circuit of Figure 25 can deliver up to 600 mA at an output voltage of 5 V. The devices can share the output capacitors, but each one requires its own transfer capacitors and input capacitor. If both a TPS60130 and a TPS60131 are used, it is possible to monitor the battery voltage with the TPS60130 using the low-battery comparator function and to supervise the output voltage with the TPS60131 using the power-good comparator. Make the layout of the charge pumps as similar as possible, and position the output capacitor the same distance from both devices.

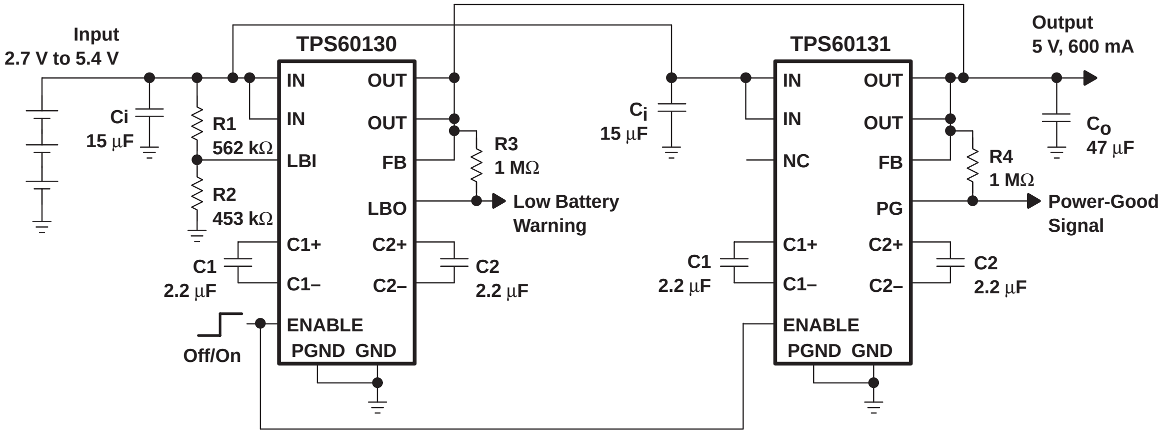


Figure 25. Paralleling of Two TPS6013x Charge Pumps

APPLICATION INFORMATION

TPS6013x operated with ultra-low quiescent current

Because the output of the TPS6013x is isolated from the input when the devices are disabled, and because the internal resistive divider is disconnected in shutdown, an ultra-low quiescent current mode can be implemented. In this mode, the output voltage is sustained because the converter is periodically enabled to refresh the output capacitor. The necessary external control signal that is applied to the ENABLE-pin is generated from a microcontroller. For a necessary supply current for the system of 1 mA and a minimum supply voltage of 4.5 V with a 33-µF output capacitor, the refresh has to be done after 9 ms. Longer refresh periods can be achieved with a larger output capacitor.

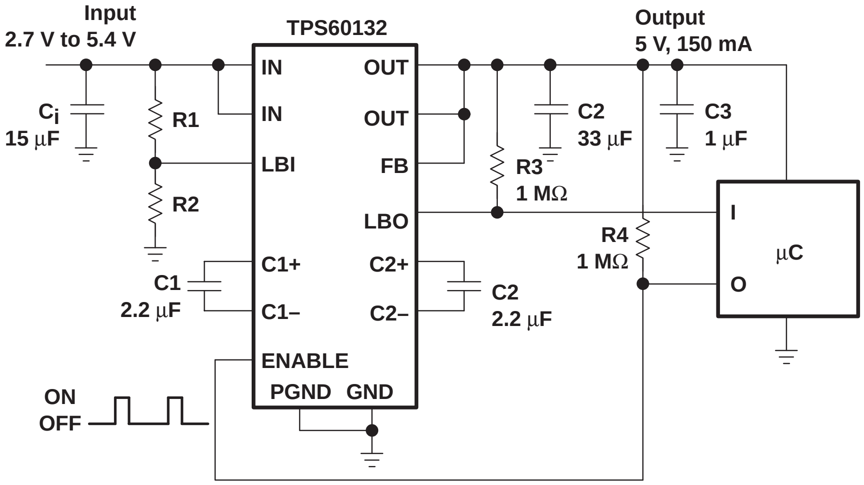


Figure 26. TPS60132 in Ultra-Low Quiescent Current Mode

regulated discharge of the output capacitors after disabling of the TPS6013x

During shutdown of the charge pump TPS6013x the output is isolated from the input. Therefore the discharging of the output capacitor depends on the load and on the leakage current of the capacitor. In certain applications it is necessary to completely remove the supply voltage from the load in shutdown mode. That means the output capacitor of the charge pump has to be actively discharged when the charge pump is disabled. Figure 10 shows one solution to this problem.

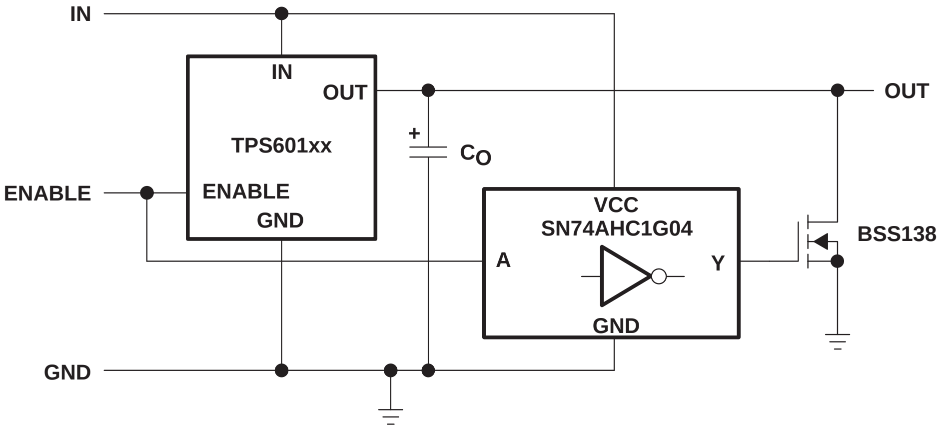


Figure 27. Block Diagram of the Regulated Discharge of the Output Capacitor

APPLICATION INFORMATION

related information

application reports

For more application information see:

- PowerPAD™ Application Report, Literature Number SLMA002
- *TPS6010x/TPS6011x Charge Pump Application Report*, Literature Number SLVA070
- Powering the TMS320C5420 Using the TPS60100, TPS76918, and the TPS3305-18, Literature Number SLVA082.

device family products

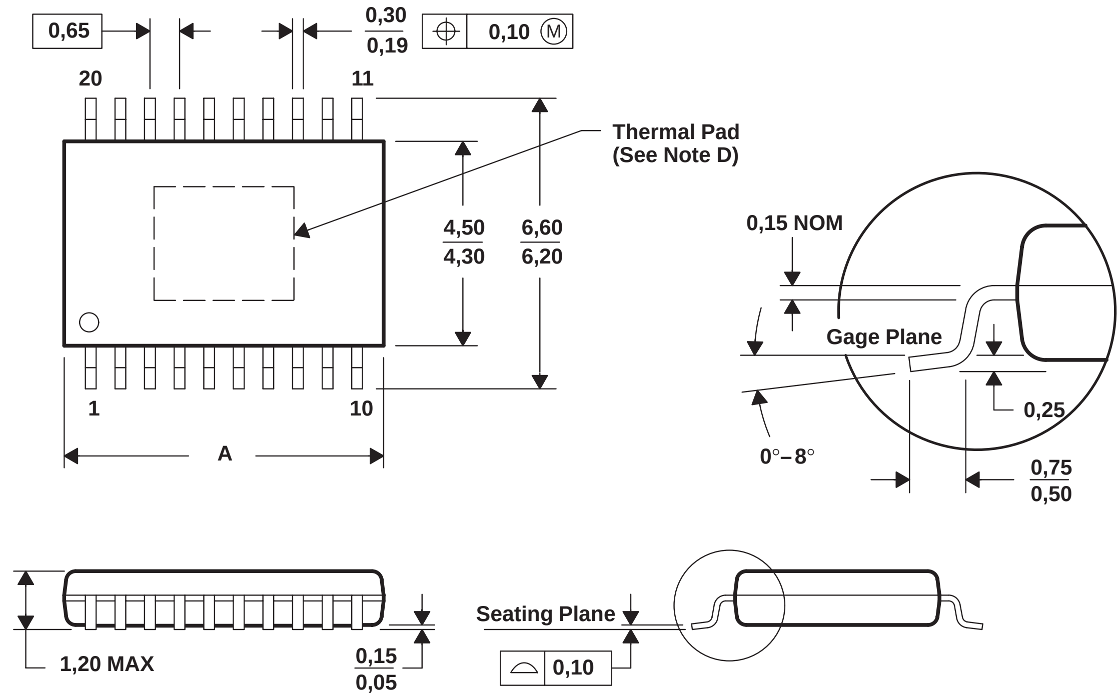
Other devices in this family are:

PART NUMBER	DATASHEET LITERATURE CODE	DESCRIPTION
TPS60100	SLVS213B	Regulated 3.3-V, 200-mA low-noise charge pump dc-dc converter
TPS60101	SLVS214A	Regulated 3.3-V, 100-mA low-noise charge pump dc-dc converter
TPS60110	SLVS215A	Regulated 5-V, 300-mA low-noise charge pump dc-dc converter
TPS60111	SLVS216A	Regulated 5-V, 150-mA low-noise charge pump dc-dc converter
TPS60120	SLVS257	Regulated 3.3-V, 200-mA high efficiency charge pump dc-dc converter with low-battery comparator
TPS60121	SLVS257	Regulated 3.3-V, 200-mA high efficiency charge pump dc-dc converter with power-good comparator
TPS60122	SLVS257	Regulated 3.3-V, 100-mA high efficiency charge pump dc-dc converter with low-battery comparator
TPS60123	SLVS257	Regulated 3.3-V, 100-mA high efficiency charge pump dc-dc converter with power-good comparator

MECHANICAL DATA

PWP (R-PDSO-G)** **PowerPAD™ PLASTIC SMALL-OUTLINE**

20 PINS SHOWN



PINS ** DIM	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/F 10/98

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusions.
- D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
- E. Falls within JEDEC MO-153

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