19-2134; Rev 2; 12/06

MAXIM

SPI-Compatible RTC in a TDFN

General Description

The MAX6902 SPI™-compatible real-time clock contains a real-time clock/calendar and 31 x 8 bits of static random-access memory (SRAM). The real-time clock/calendar provides seconds, minutes, hours, day, date, month, year, and century information. A time/date programmable polled ALARM is included in the MAX6902. The end-of-the-month date is automatically adjusted for months with fewer than 31 days, including corrections for leap year up to the year 2100. The clock operates in either the 24hr or 12hr format with an AM/PM indicator. The MAX6902 operates with a supply voltage of +2V to +5.5V, is available in the ultra-small 8-pin TDFN package, and works over the -40°C to +85°C industrial temperature range.

Applications

Point-of-Sale Equipment

Intelligent Instruments

Fax Machines

Battery-Powered Products

Portable Instruments

Features

- **Real-Time Clock Counts Seconds, Minutes, Hours, Day of Week, Date of Month, Month, Year, and Century**
- **Leap-Year Compensation Valid up to Year 2100**
- **+2V to +5.5V Wide Operating Voltage Range**
- **SPI Interface: 4MHz at 5V; 1MHz at 2V**
- **31 x 8-Bit SRAM for Scratchpad Data Storage**
- **Uses Standard 32.768kHz, 12.5pF Watch Crystal**
- **Low Timekeeping Current (400nA at 2V)**
- **Single-Byte or Multiple-Byte (Burst Mode) Data Transfer for Read or Write of Clock Registers or SRAM**
- **Ultra-Small 8-Pin 3mm x 3mm x 0.8mm TDFN Package**
- **Programmable Time/Date Polled ALARM Function**
- **No External Crystal Bias Resistors or Capacitors Required**

Ordering Information

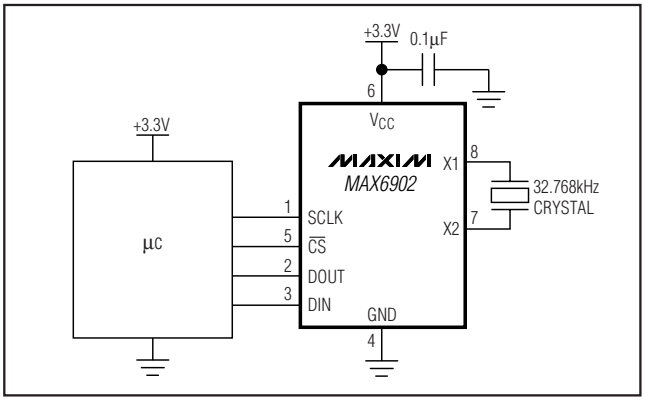
PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX6902ETA+T	-40°C to +85°C	8 TDFN	+AGT

+Denotes lead-free package.

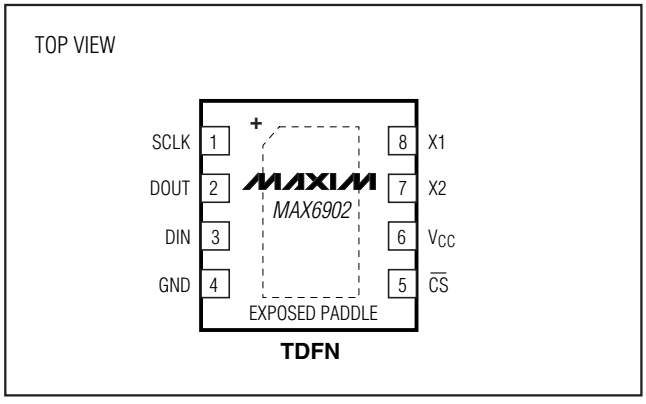
Related Real-Time Clock Products

PART	SERIAL INTERFACE	SRAM	ALARM FUNCTION	OUTPUT FREQUENCY	PIN-PACKAGE
MAX6900	I²C compatible	31 × 8	—	—	6 TDFN
MAX6901	3 Wire	31 × 8	Polled	32kHz	8 TDFN
MAX6902	SPI compatible	31 × 8	Polled	—	8 TDFN

Typical Operating Circuit



Pin Configuration



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ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +6V
All Other Pins to GND .....-0.3V to (V_{CC} + 0.3V)
Current into Any Pin.....±20mA
Rate of Rise, V_{CC} 100V/µs
Continuous Power Dissipation (T_A = +70°C)
8-Pin TDFN (derate 24.4mW/°C above +70°C) 1951.0mW
Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +150°C
ESD Protection (all pins, Human Body Model) 2000V
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.0V to +5.5V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}		2		5.5	V
Active Supply Current (Note 2)	I_{CC}	V_{CC} = +2V			0.3	mA
		V_{CC} = +5V			1.1	
Timekeeping Supply Current (Note 3)	I_{TK}	V_{CC} = +2V		0.4	0.8	µA
		V_{CC} = +5V		1.3	2.2	
SPI DIGITAL INPUTS (SCLK, DIN, $\overline{CS}$)						
Input High Voltage	V_{IH}	V_{CC} = +2V	1.4			V
		V_{CC} = +5V	2.2			
Input Low Voltage	V_{IL}	V_{CC} = +2V			0.6	V
		V_{CC} = +5V			0.8	
Input Leakage	I_{IL}	V_{IN} = 0 to V_{CC}	-10		10	nA
Input Capacitance				10		pF
SPI DIGITAL OUTPUTS (DOUT)						
Output Capacitance				15		pF
Output Low Voltage	V_{OL}	V_{CC} = +2.0V, I_{SINK} = 1.5mA			0.4	V
		V_{CC} = +5.0V, I_{SINK} = 4mA			0.4	
Output High Voltage	V_{OH}	V_{CC} = +2.0V, I_{SOURCE} = -0.4mA	1.8			V
		V_{CC} = +5.0V, I_{SOURCE} = -1mA	4.5			

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.0V to +5.5V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.) (Figure 5, Notes 1, 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OSCILLATOR						
X1 to Ground Capacitance				25		pF
X2 to Ground Capacitance				25		pF
SPI SERIAL TIMING						
Maximum Input Rise Time	t_{rIN}	DIN, SCLK, $\overline{CS}$		2		µs
Maximum Input Fall Time	t_{fIN}	DIN, SCLK, $\overline{CS}$		2		µs
Output Rise Time	t_{rOUT}	DOUT, C_{LOAD} = 100pF		10		ns
Output Fall Time	t_{fOUT}	DOUT, C_{LOAD} = 100pF		10		ns
SCLK Period	t_{CP}	V_{CC} = +2V	1000			ns
		V_{CC} = +5V	238			
SCLK High Time	t_{CH}		100			ns
SCLK Low Time	t_{CL}		100			ns
SCLK Fall to DOUT Valid	t_{DO}	C_{LOAD} = 100pF			100	ns
DIN to SCLK Setup Time	t_{DS}		100			ns
DIN to SCLK Hold Time	t_{DH}		2			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		2			ns
$\overline{CS}$ High Pulse Width	t_{CSW}		200			ns
$\overline{CS}$ High to DOUT High Impedance	t_{CSZ}				100	ns
$\overline{CS}$ to SCLK Setup Time	t_{CSS}		100			ns

Note 1: All parameters are 100% tested at T_A = +25°C. Limits over temperature are guaranteed by design and characterization and not production tested.

Note 2: I_{CC} is specified with DOUT open, $\overline{CS}$ = DIN = GND, SCLK = 4MHz at V_{CC} = +5V; SCLK = 1MHz at V_{CC} = +2.0V.

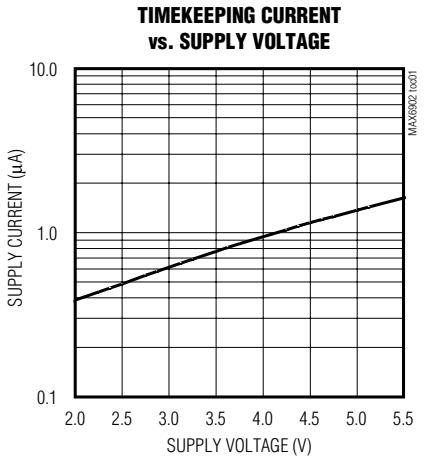
Note 3: Timekeeping current is specified with $\overline{CS}$ = V_{CC}, SCLK = DIN = GND, DOUT = 100kΩ to GND.

Note 4: All values referred to V_{IH} min and V_{IL} max levels.

SPI-Compatible RTC in a TDFN

Typical Operating Characteristic

(T_A = +25°C, unless otherwise noted.)



Pin Description

PIN	NAME	FUNCTION
1	SCLK	Serial Clock Input. SPI clock for DIN and DOUT data transfers.
2	DOUT	SPI Data Output
3	DIN	SPI Data Input
4	GND	Ground
5	$\overline{CS}$	Chip Select Input. Active low for valid data transfers.
6	V_{CC}	Power-Supply Pin. Bypass V_{CC} to GND with a 0.1µF capacitor.
7	X2	External 32.768kHz Crystal
8	X1	External 32.768kHz Crystal
—	EP	Exposed Paddle. Internally connected to GND. Connect to GND, but do not use as the sole ground connection point or leave unconnected.

Detailed Description

The MAX6902 is a real-time clock/calendar with an SPI-compatible interface and 31 x 8 bits of SRAM. It provides seconds, minutes, hours, day of the week, date of the month, month, and year information, held in seven 8-bit timekeeping registers (*Functional Diagram*). An on-chip 32.768kHz oscillator circuit requires only a single external crystal to operate. Table 1 specifies the parameters for the external crystal, and Figure 1 shows a functional schematic of the oscillator circuit. The MAX6902's register addresses and definitions are described in Figure 2 and in Table 2. Time and calendar data are stored in the registers in binary-coded decimal (BCD) format. A polled alarm function is included for scheduled timing of user-defined times or intervals.

Table 1. Acceptable Quartz Crystal Parameters

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Frequency	f		32.768		kHz
Equivalent Series Resistance (ESR)	R_S	40		60	kΩ
Parallel Load Capacitance	C_L	11.2	12.5	13.7	pF
Q Factor	Q	40,000		60,000	

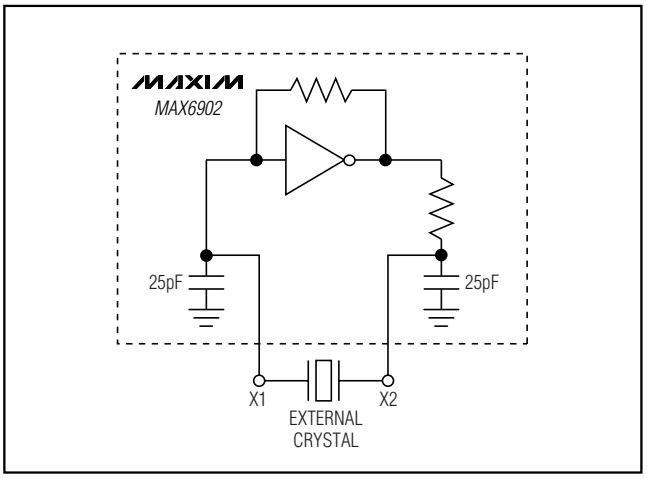


Figure 1. Crystal Oscillator Circuit Schematic

REGISTER ADDRESS									REGISTER DEFINITION								
FUNCTION CLOCK	A7	A6	A5	A4	A3	A2	A1	A0	VALUE	D7	D6	D5	D4	D3	D2	D1	D0
SECONDS	RD	0	0	0	0	0	0	1	00-59	0	10 SEC			1 SEC			
	/W								*POR STATE	0	0	0	0	0	0	0	0
MINUTES	RD	0	0	0	0	0	1	1	00-59	ALM OUT	10 MIN			1 MIN			
	/W								*POR STATE	0	0	0	0	0	0	0	0
HOURS	RD	0	0	0	0	1	0	1	00-23	12/24	0	10 HR	10 HR	1 HR			
	/W								01-12	1/0		A/P 0/1					
									*POR STATE	0	0	0	0	0	0	0	0
DATE	RD	0	0	0	0	1	1	1	01-28/29 01-30 0-31	0	0	10 DATE		1 DATE			
	/W								*POR STATE	0	0	0	0	0	0	0	1
MONTH	RD	0	0	0	1	0	0	1	01-12	0	0	0	10M	1 MONTH			
	/W								*POR STATE	0	0	0	0	0	0	0	1
DAY	RD	0	0	0	1	0	1	1	01-07	0	0	0	0	0	WEEK DAY		
	/W								*POR STATE	0	0	0	0	0	0	0	1
YEAR	RD	0	0	0	1	1	0	1	00-99	10 YEAR				1 YEAR			
	/W								*POR STATE	0	1	1	1	0	0	0	0
CONTROL	RD	0	0	0	1	1	1	1		WP	0	0	0	0	0	0	0
	/W								*POR STATE	0	0	0	0	0	0	0	0
CENTURY	RD	0	0	1	0	0	1	1	00-99	1000 YEAR				100 YEAR			
	/W								*POR STATE	0	0	0	1	1	0	0	1

Note: *POR STATE defines power-on reset state of register contents.

Figure 2. Register Address Definition (Sheet 1 of 3)

SPI-Compatible RTC in a TDFN

FUNCTION		REGISTER ADDRESS A7	A6	A5	A4	A3	A2	A1	A0	VALUE	REGISTER DEFINITION D7	D6	D5	D4	D3	D2	D1	D0
ALARM CONFIG	RD	**0**	**0**	**1**	**0**	**1**	**0**	**1**			0	YEAR	DAY	MONTH	DATE	HOUR	MINUTE	SECOND
	/W									***POR STATE**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RESERVED Do not write to this location.	RD	0	0	1	0	1	1	1			0	0	0	0	0	1	1	1
	/W									***POR STATE**	0	0	0	0	0	1	1	1
ALARM THRESHOLDS																		
SECONDS	RD	**0**	**0**	**1**	**1**	**0**	**0**	**1**		00-59	0	10 SEC			1 SEC			
	/W									***POR STATE**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
MINUTES	RD	**0**	**0**	**1**	**1**	**0**	**1**	**1**		00-59	0	10 MIN			1 MIN			
	/W									***POR STATE**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
HOURS	RD	**0**	**0**	**1**	**1**	**1**	**0**	**1**		00-23	12/24	0	10 HR	10 HR	1 HR			
	/W									01-12	1/0		A/P 0/1					
										***POR STATE**	**1**	**0**	**1**	**1**	**1**	**1**	**1**	**1**
DATE	RD	**0**	**0**	**1**	**1**	**1**	**1**	**1**		01-28/29 01-30 01-31	0	0	10 DATE		1 DATE			
	/W									***POR STATE**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**
MONTH	RD	**0**	**1**	**0**	**0**	**0**	**0**	**1**		01-12	0	0	0	10M	1 MONTH			
	/W									***POR STATE**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**
DAY	RD	**0**	**1**	**0**	**0**	**0**	**1**	**1**		01-07	0	0	0	0	0	WEEK DAY		
	/W									***POR STATE**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**
YEAR	RD	**0**	**1**	**0**	**0**	**1**	**0**	**1**		00-99	10 YEAR				1 YEAR			
	/W									***POR STATE**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
CLOCK BURST	RD	**0**	**1**	**1**	**1**	**1**	**1**	**1**										
	/W																	

Figure 2. Register Address Definition (Sheet 2 of 3)

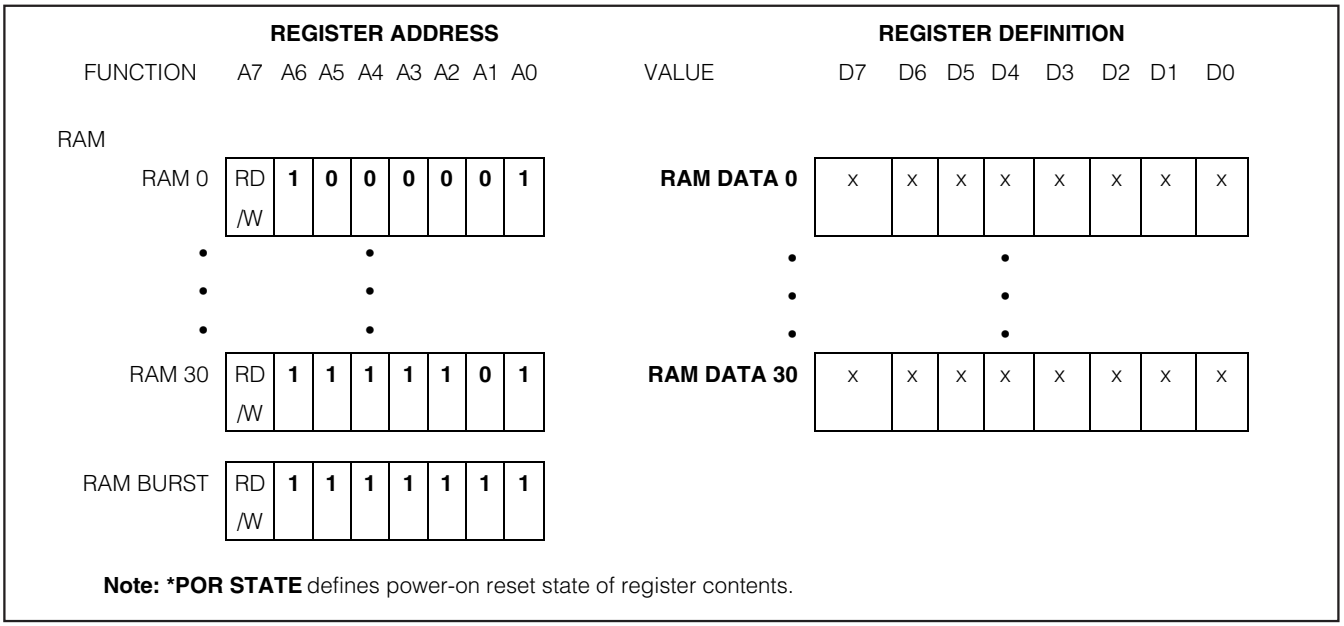


Figure 2. Register Address Definition (Sheet 3 of 3)

Table 2. Register Address and Description

WRITE (HEX)	READ (HEX)	DESCRIPTION	POR CONTENTS (HEX)
01	81	Seconds	00
03	83	Minutes	00
05	85	Hours	00
07	87	Date	01
09	89	Month	01
0B	8B	Day	01
0D	8D	Year	70
0F	8F	Control	00
13	93	Century	19
15	95	Alarm Configuration	00
17	97	Reserved	07
19	99	Seconds Alarm Threshold	7F
1B	9B	Minutes Alarm Threshold	7F
1D	9D	Hours Alarm Threshold	BF
1F	9F	Date Alarm Threshold	3F
21	A1	Month Alarm Threshold	1F
23	A3	Day Alarm Threshold	07
25	A5	Year Alarm Threshold	FF
3F	BF	Clock Burst	Not applicable

Table 2. Register Address and Description (continued)

WRITE (HEX)	READ (HEX)	DESCRIPTION	POR CONTENTS (HEX)
41	C1	RAM 0	Indeterminate
43	C3	RAM 1	Indeterminate
45	C5	RAM 2	Indeterminate
47	C7	RAM 3	Indeterminate
49	C9	RAM 4	Indeterminate
4B	CB	RAM 5	Indeterminate
4D	CD	RAM 6	Indeterminate
4F	CF	RAM 7	Indeterminate
51	D1	RAM 8	Indeterminate
53	D3	RAM 9	Indeterminate
55	D5	RAM 10	Indeterminate
57	D7	RAM 11	Indeterminate
59	D9	RAM 12	Indeterminate
5B	DB	RAM 13	Indeterminate
5D	DD	RAM 14	Indeterminate
5F	DF	RAM 15	Indeterminate
61	E1	RAM 16	Indeterminate
63	E3	RAM 17	Indeterminate
65	E5	RAM 18	Indeterminate
67	E7	RAM 19	Indeterminate
69	E9	RAM 20	Indeterminate
6B	EB	RAM 21	Indeterminate
6D	ED	RAM 22	Indeterminate
6F	EF	RAM 23	Indeterminate
71	F1	RAM 24	Indeterminate
73	F3	RAM 25	Indeterminate
75	F5	RAM 26	Indeterminate
77	F7	RAM 27	Indeterminate
79	F9	RAM 28	Indeterminate
7B	FB	RAM 29	Indeterminate
7D	FD	RAM 30	Indeterminate
7F	FF	RAM Burst	Not applicable

Command and Control

Address/Command Byte

Each data transfer into or out of the MAX6902 is initiated by an Address/Command byte. The Address/Command byte specifies which registers are to be accessed, and if the access is a read or a write. Figure 2 shows the Address/Command bytes and their associated registers, and Table 2 lists the hex codes for all read and write operations. The Address/Command bytes are input MSB (bit 7) first. Bit 7 specifies a write (logic 0) or read (logic 1). Bit 6 specifies register data (logic 0) or RAM data (logic 1). Bits 5–1 specify the designated register to be written or read. The LSB (bit 0) must be logic 1. If the LSB is a zero, writes to the MAX6902 are disabled.

Clock Burst Mode

Sending the Clock Burst Address/Command (3Fh for Write and BFh for Read), specifies burst-mode operation. In this mode, multiple bytes are read or written after a single Address/Command. The first seven clock/calendar registers (Seconds, Minutes, Hours, Date, Month, Day, and Year) and the Control register are consecutively read or written, starting with the MSB of the Seconds register. When writing to the clock registers in burst mode, all seven clock/calendar registers and the Control register must be written in order for the data to be transferred. See *Example: Setting the Clock with a Burst Write*.

RAM Burst Mode

Sending the RAM Burst Address/Command (F7h for Write, FFh for Read) specifies burst-mode operation. In this mode, the 31 RAM locations can be consecutively read or written, starting at 41h for Writes, and C1h for Reads. A Burst Read outputs all 31 bytes of RAM. When writing to RAM in burst mode, it is not necessary to write all 31 bytes for the data to transfer; each complete byte written is transferred to RAM. When reading from RAM, data are output until all 31 bytes have been read, or until $\overline{CS}$ is driven high.

Setting the Clock

Writing to the Timekeeping Registers

The time and date are set by writing to the timekeeping registers (Seconds, Minutes, Hours, Date, Month, Day, Year, and Century). During a write operation, an input buffer accepts the new time data while the timekeeping registers continue to increment normally, based on the crystal counter. The buffer also keeps the timekeeping registers from changing as the result of an incomplete write operation, and collision-detection circuitry ensures that a Time Write does not occur coincident with a Seconds register increment. The updated time data are loaded into the timekeeping registers after the rising edge of $\overline{CS}$, at the end of the SPI write operation. An incomplete write operation aborts the update procedure, and the contents of the input buffer are discarded. The timekeeping registers reflect the new time beginning with the first Seconds register increment after the rising edge of $\overline{CS}$.

Although both Single Writes and Burst Writes are possible, the best way to write to the timekeeping registers is with a Burst Write. With a Burst Write, the main timekeeping registers (Seconds, Minutes, Hours, Date, Month, Day, Year) and the Control register are written sequentially following the Address/Command byte. They must be written as a group of eight registers, with 8 bits each, for proper execution of the Burst Write function. All seven timekeeping registers are simultaneously loaded into the clock counters by the rising edge of $\overline{CS}$, at the end of the SPI write operation. For a normal burst data transfer, the worst-case error that can occur between the actual time and the written time update is 1s.

If single write operations are used to enter data into the timekeeping registers, error checking is required. If not writing to the Seconds register, begin by reading the Seconds register and save it as initial-seconds. Then write to the required timekeeping registers, and finally read the Seconds register again (final-seconds). Check to see that final-seconds is equal to initial-seconds. If not, repeat the write process. If writing to the Seconds register, update the Seconds register first, and then read it back and store its value (initial-seconds). Update the remaining timekeeping registers and then read the Seconds register again (final-seconds). Check to see that final-seconds is equal to initial-seconds. If not, repeat the write process.

Note: After writing to any time or date register, no read or write operations are allowed for 45µs.

AM/PM and 12Hr/24Hr Mode

Bit 7 of the Hours register selects 12hr or 24hr mode. When high, 12hr mode is selected. In 12hr mode, bit 5 is the AM/PM bit, logic high for PM. In 24hr mode, bit 5 is the second 10hr bit, logic high for hours 20 through 23.

Write-Protect Bit

Bit 7 of the Control register is the Write-Protect bit. When high, the Write-Protect bit prevents write operations to all registers except itself. After initial settings are written to the timekeeping registers, set the Write-Protect bit to logic 1 to prevent erroneous data from entering the registers during power glitches or interrupted serial transfers. The lower 7 bits (bits 0–6) are

unusable, and always read zero. Any data written to bits 0–6 are ignored. Bit 7 must be set to zero before a single write to the clock, before a write to RAM, or during a Burst Write to the clock.

Example: Setting the Clock with a Burst Write

To set the clock to 10:11:31PM, Thursday July 4th, 2002 with a burst write operation, write 3Fh as the Address/Command byte, followed by 8 bytes, 31h, 11h, B0h, 04h, 07h, 05h, 02h, and 00h (Figure 2). 3Fh is the Clock Burst Write Address/Command. The first byte, 31h, sets the Seconds register to 31. The second byte, 11h, sets the Minutes register to 11. The third byte, B0h, sets the Hours register to 12hr mode, and 10PM. The fourth byte, 04h, sets the Date register (day of the month) to the 4th. The fifth byte, 07h, sets the Month register to July. The sixth byte, 05h, sets the Day register (day of the week) to Thursday. The seventh byte, 02h, sets the Year register to 02. The eighth byte, 00h, clears the Write-Protect bit of the Control register to allow writing to the MAX6902. The Century register is not accessed with a Burst Write and therefore must be written to separately to set the century to 20. Note the Century register corresponds to the thousand and hundred digits of the current year and defaults to 19.

Reading the Clock

Reading the Timekeeping Registers

The main timekeeping registers (Seconds, Minutes, Hours, Date, Month, Day, Year) can be read with either Single Reads or a Burst Read. In the MAX6902, a latch buffers each clock counter's data. Clock counter data are latched by the SPI Read Command (on the falling edge of SCLK, after the Address/Command byte has been sent by the master to read a timekeeping register). Collision-detection circuitry ensures that this does not happen coincident with a Seconds counter increment to ensure accurate time data are being read. The clock counters continue to count and keep accurate time during the read operation.

The simplest way to read the timekeeping registers is to use a Burst Read. In a Burst Read, the main timekeeping registers (Seconds, Minutes, Hours, Date, Month, Day, Year), and the Control register are read sequentially, in the order listed with the Seconds register first. They are read out as a group of eight registers, with 8 bits each. All timekeeping registers (except Century) are latched upon the receipt of the Burst Read command. The worst-case error between the "actual" time and the "read" time is 1s for a normal data transfer.

The timekeeping registers may also be read using Single Reads. If Single Reads are used, it is necessary to do some error checking on the receiving end, because it is possible that the clock counters could change during the Read operations, and report inaccurate time data. The potential for error is when the Seconds register increments before all the registers are read. For example, suppose a carry of 13:59:59 to 14:00:00 occurs during single read operations. The net data read could be 14:59:59, which is erroneous. To prevent errors from occurring with single read operations, read the Seconds register first (initial-seconds) and store this value for future comparison. After the remaining timekeeping registers have been read, reread the Seconds register (final-seconds). Check that the final-seconds value equals the initial-seconds value. If not, repeat the entire Single Read process. Using Single Reads at a 100kHz serial speed, it takes under 2.5ms to read all seven of the timekeeping registers, including two reads of the Seconds register.

Example: Reading the Clock with a Burst Read

To read the time with a Burst Read, send BFh as the Address/Command byte. Then clock out 8 bytes, Seconds, Minutes, Hours, Date of the month, Month, Day of the week, Year, and finally the Control byte. All data are output MSB first. Decode the required information based on the register definitions listed in Figure 2.

Using the Alarm

A polled alarm function is available by reading the ALM OUT bit. The ALM OUT bit is D7 of the Minutes timekeeping register. A logic 1 in ALM OUT indicates the Alarm function is triggered. There are eight registers associated with the alarm function—seven programmable Alarm Threshold registers and one programmable Alarm Configuration register. The Alarm Configuration register determines which Alarm Threshold registers are compared to the timekeeping registers, and the ALM OUT bit sets if the compared registers are equal. Figure 2 shows the function of each bit of the Alarm Configuration register. Placing a logic 1 in any given bit of the Alarm Configuration register enables the respective alarm function. For example, if the Alarm Configuration register is set to 0000 0011, ALM OUT is set when both the minutes and seconds indicated in the Alarm Threshold registers match the respective timekeeping registers. Once set, ALM OUT stays high until it is cleared by reading or writing to the Alarm Configuration register, or by reading or writing to any of the Alarm Threshold registers. The Alarm Configuration register is written with address 15h, and read with address 95h.

Using the On-Board RAM

The static RAM is 31 x 8 bits addressed consecutively in the RAM Address/Command space. Table 2 details the specific hex Address/Commands for Reads and Writes to each of the 31 locations of RAM. The contents of the RAM are static and remain valid for V_{CC} down to 2V. All RAM data are lost if power is cycled. The Write-Protect Bit (bit 7 of the Control register), when high, disallows any writes to RAM.

SPI-Compatible Serial Interface

Interface the MAX6902 with a microcontroller using a serial, 4-wire, SPI interface. SPI is a synchronous bus for address and data transfer, and is used with Motorola or other microcontrollers that have an SPI port. Four connections are required for the interface: DOUT (Serial Data Out); DIN (Serial Data In); SCLK (Serial Clock); and $\overline{CS}$ (Chip Select). In an SPI application, the MAX6902 acts as a slave device and the microcontroller acts as the master. $\overline{CS}$ is asserted low by the microcontroller to initiate a transfer, and deasserted high to terminate a transfer. DIN transfers input data from the microcontroller to the MAX6902. DOUT transfers output data from the MAX6902 to the microcontroller. A shift clock, SCLK, is used to synchronize data movement between the microcontroller and the MAX6902. SCLK, which is generated by the microcontroller, is active only during address and data transfer to any device on the SPI bus. The inactive clock polarity is usually programmable on the microcontroller side of the SPI interface. In the MAX6902, input data are latched on the positive edge, and output data are shifted out on the negative edge. There is one clock cycle for each bit transferred. Address and data bits are transferred in groups of eight.

The SPI protocol allows for one of four combinations of serial clock phase and polarity from the microcontroller, through a 2-bit selection in its SPI Control register. The clock polarity is specified by the CPOL Control bit, which selects active-high or active-low clock, and has no significant effect on the transfer format. The Clock Phase Control bit, CPHA, selects one of two different transfer formats. The clock phase and polarity must be identical for the master and the slave. For the MAX6902, set the control bits to CPHA = 1 and CPOL = 1. This configures the system for data to be launched on the negative edge of SCLK and sampled on the positive edge. With CPHA equal to 1, $\overline{CS}$ can remain low between successive data byte transfers, allowing burst-mode data transfers to occur.

Address and data bytes are shifted MSB first into DIN of the MAX6902, and out of DOUT. Data are shifted out at the negative edge of SCLK, and shifted in or sampled at the positive edge of SCLK. Any transfer requires an Address/Command byte followed by one or more bytes of data. Data are transferred out of DOUT for a read operation, and into DIN for a write operation. DOUT transmits data only after an Address/Command byte specifies a read operation; otherwise, it is high impedance.

Data Transfer Write timing is shown in Figure 3. Data Transfer Read timing is shown in Figure 4. Detailed Read and Write Timing is shown in Figure 5.

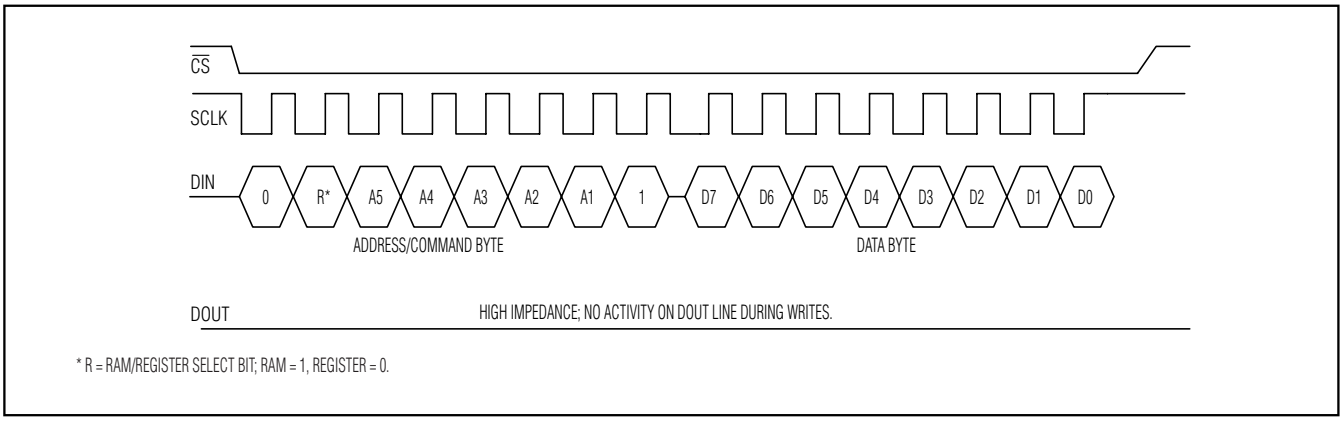


Figure 3a. Single Write

SPI-Compatible RTC in a TDFN

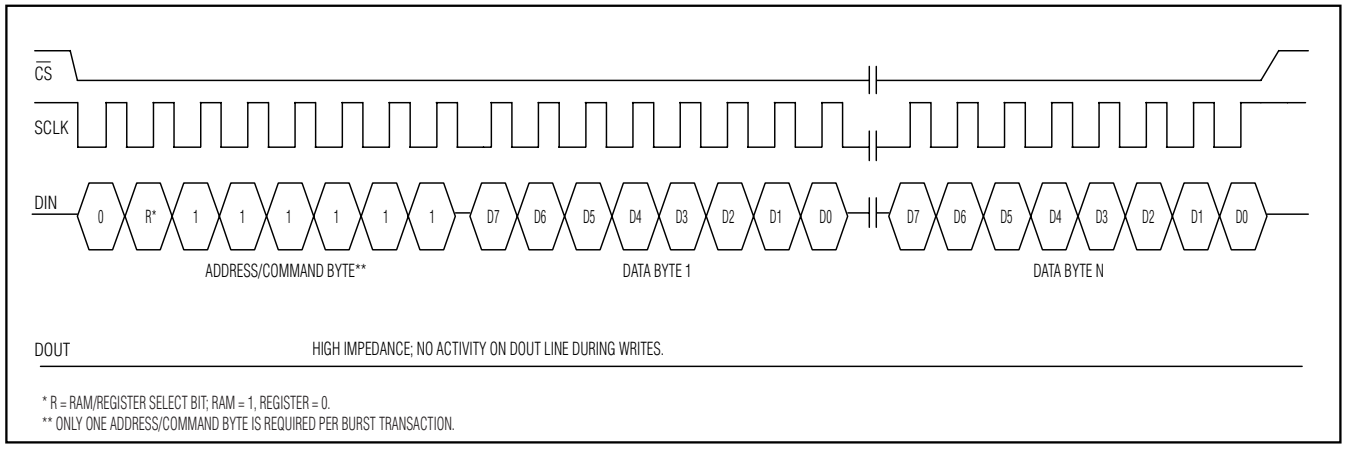


Figure 3b. Burst Write

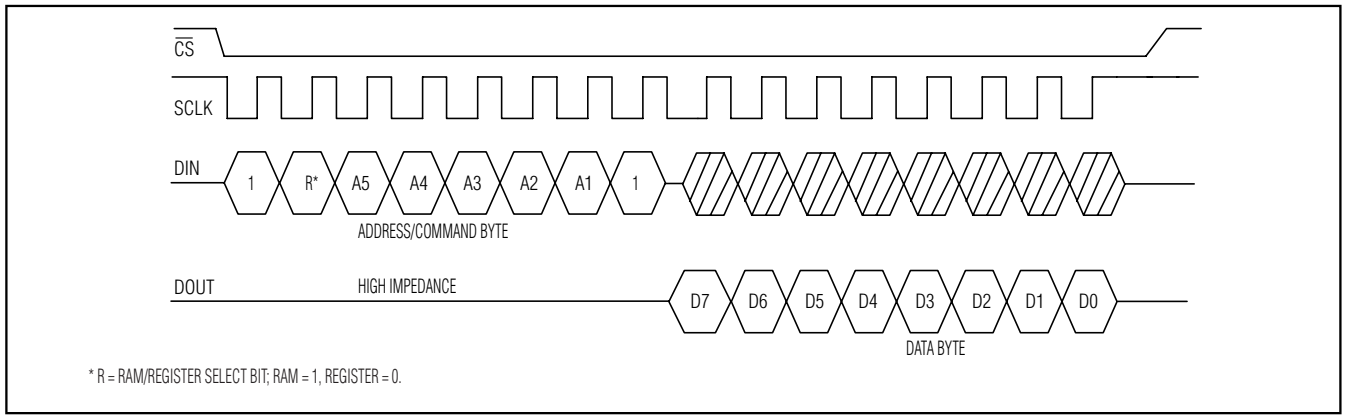


Figure 4a. Single Read

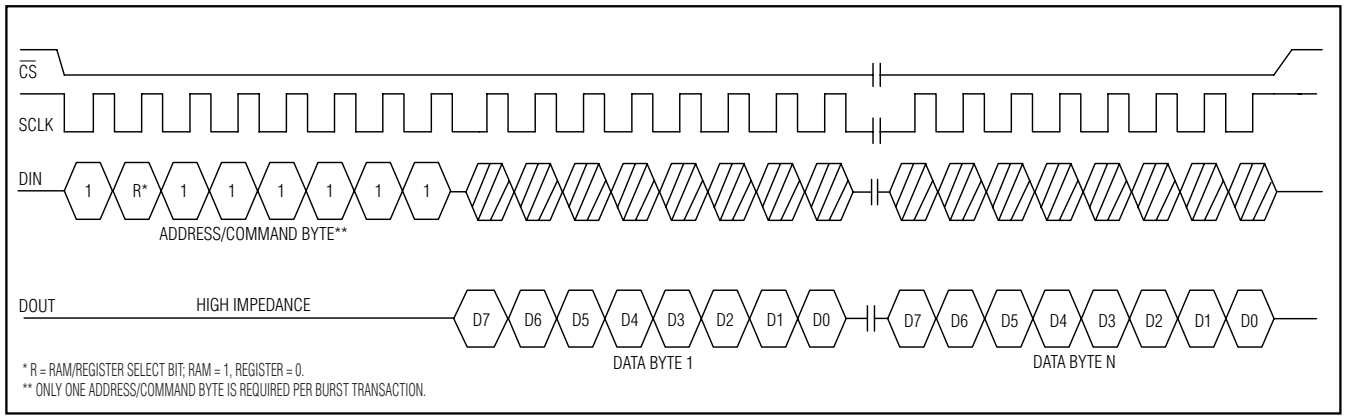


Figure 4b. Burst Read

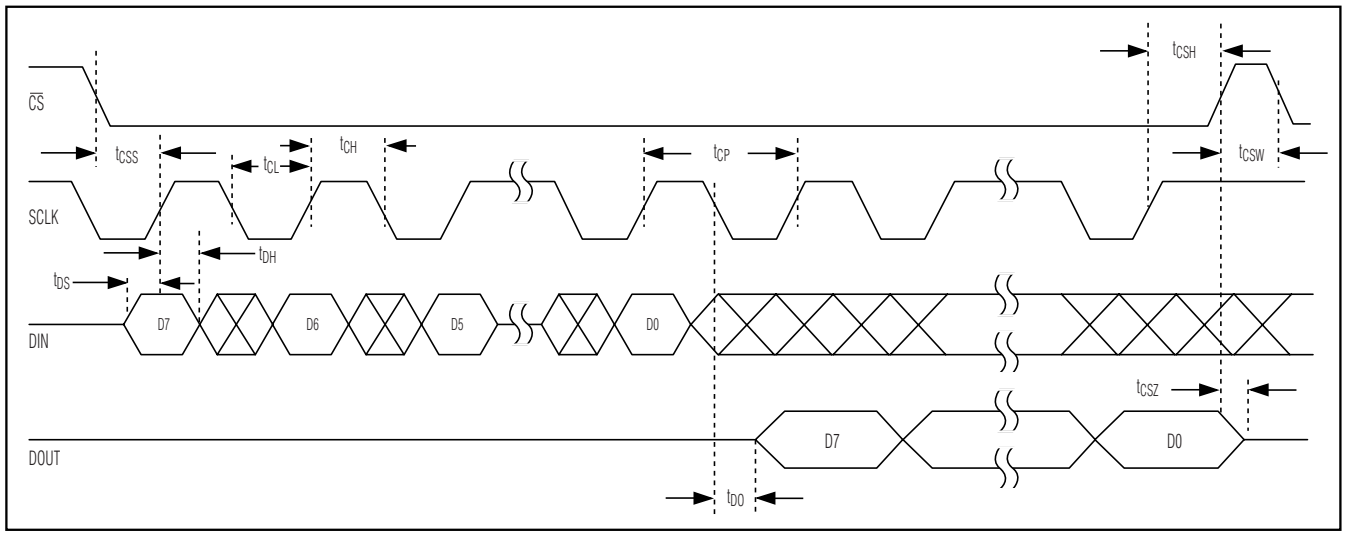


Figure 5. SPI Bus Timing Diagrams

Chip Select

$\overline{CS}$ serves two functions. First, $\overline{CS}$ turns on the control logic that allows access to the Shift register for Address/Command and data transfer. Second, $\overline{CS}$ provides a method of terminating either single-byte or multiple-byte data transfers. All data transfers are initiated by driving $\overline{CS}$ low. If $\overline{CS}$ is high, then DOUT is high impedance.

Serial Clock

A clock cycle on SCLK is a rising edge followed by a falling edge. For data input, data must be valid at DIN before the rising edge of the clock. For data outputs, bits are valid on DOUT after the falling edge of the clock.

Data Input (Single-Byte Write)

Following the eight SCLK cycles that input a Single-Byte Write Address/Command, data bits are input on the rising edges of the next eight SCLK cycles. Additional SCLK cycles are ignored. Input data MSB first.

Data Input (Burst Write)

Following the eight SCLK cycles that input a Burst-Write Address/Command, data bits are input on the rising edges of the following SCLK cycles. The number of clock cycles depends on whether the timekeeping registers or RAM are being written. A Clock Burst Write requires 1 Address/Command byte, 7 timekeeping data bytes, and 1 Control register byte. A Burst Write to RAM may be terminated after any complete data byte by driving $\overline{CS}$ high. Input data MSB first (Figure 3).

Data Output (Single-Byte Read and Burst Read)

A read from the MAX6902 is initiated by an Address/Command Write from the microcontroller (master) to the MAX6902 (slave). The Address/Command Write portion of the data transfer is clocked into the MAX6902 on rising clock edges. Following the eighth falling clock edge of SCLK, after t_{DO} (Figure 4) data begins to be output on DOUT of the MAX6902. Data bytes are output MSB first. Additional SCLK cycles transmit additional data bits, as long as $\overline{CS}$ remains low. This permits continuous burst-mode read capability.

Applications Information

Crystal Selection

The MAX6902 is designed to use a standard 32.768kHz watch crystal. Table 1 details the recommended crystal requirements. Some suggested crystals are listed in Table 3. In addition to the specified SMT devices, some of the listed manufacturers also offer other package options.

Frequency Stability and Temperature

Timekeeping accuracy of the MAX6902 is dependent on the frequency stability, of the external crystal. To determine frequency stability, use the parabolic curve in Figure 6 and the following equations:

$$\Delta f = fk(T_0 - T)^2$$

where:

Δf = change in frequency from +25°C (Hz)

f = nominal crystal frequency (Hz)

Table 3. 32.768kHz Surface-Mount Watch Crystals

MANUFACTURER	MANUFACTURER PART NO.	TEMP. RANGE	C_L (pF)	+25°C FREQUENCY TOLERANCE (ppm)
Abracon Corporation	ABS25-32.768-12.5-B-2-T	-40°C to +85°C	12.5	±20
Caliber Electronics	AWS2A-32.768KHz, AWS2B-32.768KHz	-20°C to +70°C	12.5	±20
ECS INC International	ECS-.327-12.5-17	-10°C to +60°C	12.5	±20
Fox Electronics	FSM327	-40°C to +85°C	12.5	±20
M-tron	SX2010/ SX2020	-20°C to +75°C	12.5	±20
Raltron	RSE-32.768-12.5-C-T	-10°C to +60°C	12.5	±20
SaRonix	32S12A	-40°C to +85°C	12.5	±20

k = parabolic curvature constant (-0.035 ±0.005ppm/°C^2 for 32.768kHz watch crystals)

T_0 = turnover temperature (+25°C ±5°C for 32.768kHz watch crystals)

T = temperature of interest (°C)

For example: What is the worst-case change in oscillator frequency from +25°C ambient to +45°C ambient?

$$\Delta f_{drift} = 32.768Hz \times \left(-0.04ppm/^{\circ}C^2 \times (1 \times 10^{-6})\right) \times (20^{\circ}C - 45^{\circ}C)^2 = -0.8192Hz$$

What is the worst-case timekeeping error per second? Error due to temperature drift:

$$\Delta t_{drift} = \left\{\left[1/\left[\left(f + \Delta f_{drift}\right)/32{,}768\right]\right] - 1s\right\}/1s$$

$$\Delta t_{drift} = \left\{\left[1/\left[\left(32{,}768Hz - 0.8192Hz\right)/32{,}768\right]\right] - 1s\right\}/1s = 0.000025s/s$$

Error due to 25°C initial crystal tolerance of ±20ppm:

$$\Delta t_{initial} = \left\{\left[1/\left[\left(f + \Delta f_{initial}\right)/32{,}768\right]\right] - 1s\right\}/1s$$

$$\Delta f_{initial} = 32{,}768Hz \times \left(-20ppm \times (1 \times 10^{-6})\right) = 0.65536Hz$$

Total timekeeping error per second:

$$\Delta t_{initial} = \left\{\left[1/\left[\left(32{,}768 - 0.65536\right)/32{,}768\right]\right] - 1\right\}/1s = 0.000020s/s$$

$$\Delta t_{total} = \Delta t_{drift} + \Delta t_{initial}$$

$$\Delta t_{total} = 0.000025s/s + 0.000020s/s = 0.000045s/s$$

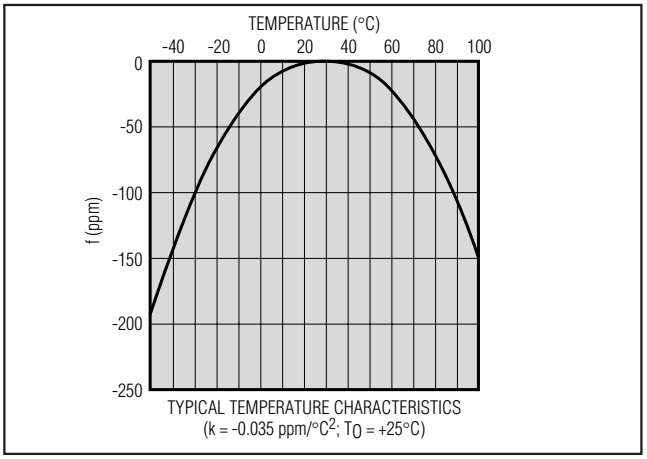


Figure 6. Typical Temperature Curve for 32.768kHz Watch Crystal

After 1 month that translates to:

$$\Delta t = \left(31day\right)\left(24\frac{hr}{day}\right)\left(60\frac{min}{hr}\right)\left(60\frac{s}{min}\right)(0.000045s/s) = 120.528s$$

Total worst-case timekeeping error at the end of 1 month at 45°C is about 120s or 2min (assumes negligible parasitic layout capacitance).

Oscillator Start Time

The MAX6902 oscillator typically takes 5s to 10s to begin oscillating. To ensure the oscillator is operating correctly, the software should validate proper timekeeping. This is accomplished by reading the Seconds register. Any reading of 1s or more from the POR value of zero seconds is a validation of proper startup.

Timekeeping Current

When DOUT is high impedance ($\overline{CS}$ = high or during a DIN transfer segment), there is a potential for increased timekeeping current (up to 100x) if DOUT is allowed to float. If minimum timekeeping current is desired, then ensure DOUT is not allowed to float. The microcontroller port pin attached to DOUT could be configured as an input with a weak pullup. An alternate solution is to use a 100kΩ, or less, pulldown or pullup resistor (for microcontroller port pins with ≤1µA input leakage).

Power-On Reset

The MAX6902 contains an integral POR circuit that ensures all registers are reset to a known state on power-up. Once V_{CC} rises above 1.6V (typ), the POR circuit releases the registers for normal operation. When V_{CC} drops to less than 1.6V (typ), the MAX6902 resets all register contents to the POR defaults (Figure 2).

RESERVED Register

Address/Command 17h is reserved for factory testing ONLY. Do not write to this register. If inadvertent writes are done to this register, cycle power to the MAX6902.

Power-Supply Considerations

For most applications, a 0.1µF capacitor from V_{CC} to GND provides adequate bypassing for the MAX6902. A series resistor can be added to the supply line for operation in extremely harsh or noisy environments.

PC Board Layout Considerations

The MAX6902 uses a very-low-current oscillator to minimize supply current. This causes the oscillator pins, X1 and X2, to be relatively high impedance. Exercise care to prevent unwanted noise pickup.

Connect the 32.768kHz crystal directly across X1 and X2 of the MAX6902. To eliminate unwanted noise pickup, design the PC board using these guidelines (Figure 7):

1) Place the crystal as close to X1 and X2 as possible and keep the trace lengths short.
2) Place a guard ring around the crystal, X1 and X2 traces (where applicable), and connect the guard ring to GND; keep all signal traces away from beneath the crystal, X1, and X2.
3) Finally, an additional local ground plane can be added under the crystal on an adjacent PC board layer. The plane should be isolated from the regular PC board ground plane, and tied to ground at the MAX6902 ground pin.
4) Restrict the plane to be no larger than the perimeter of the guard ring. Do not allow this ground plane to contribute significant capacitance between X1 and X2.

Chip Information

TRANSISTOR COUNT: 26,418

PROCESS: CMOS

SPI-Compatible RTC in a TDFN

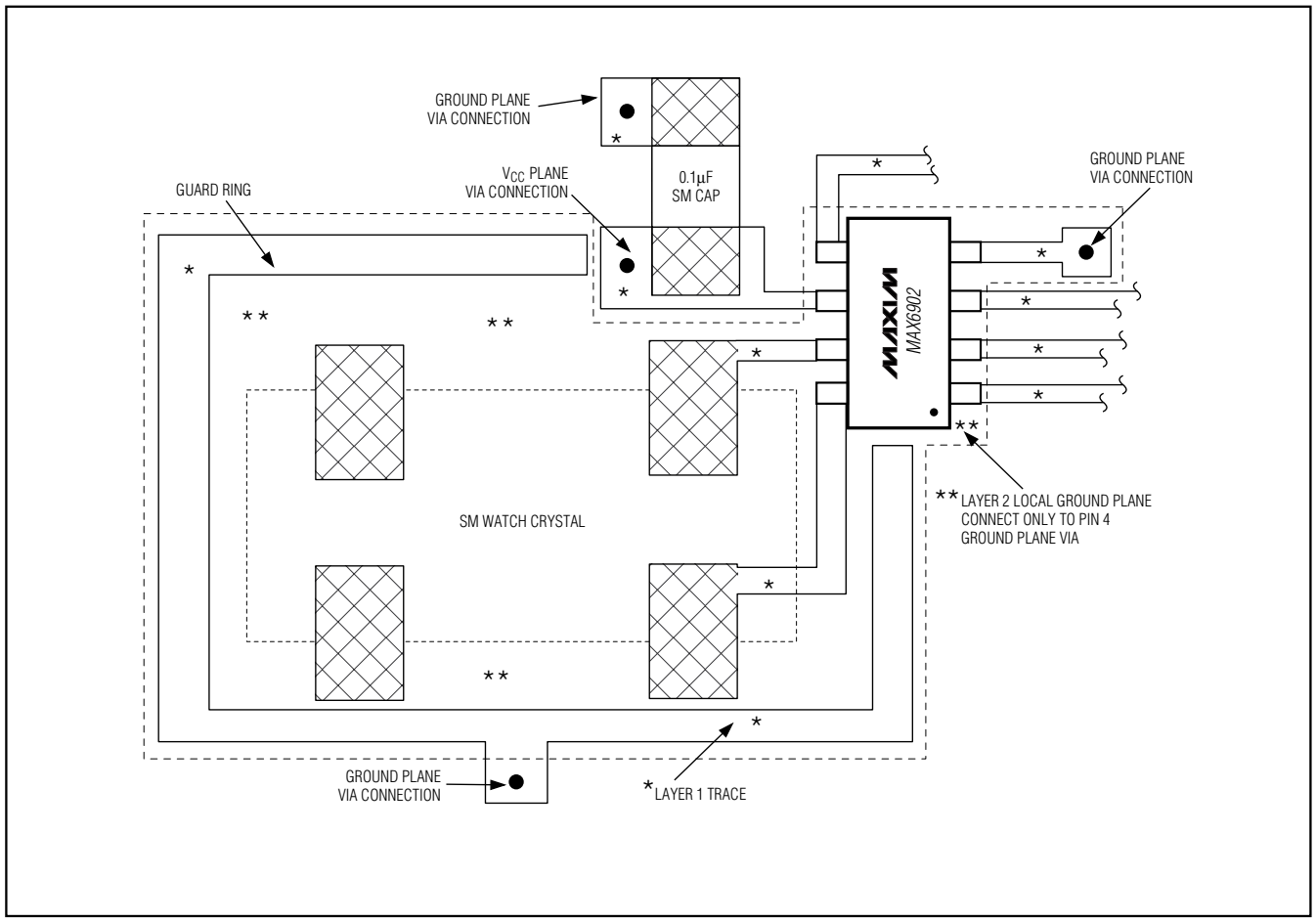
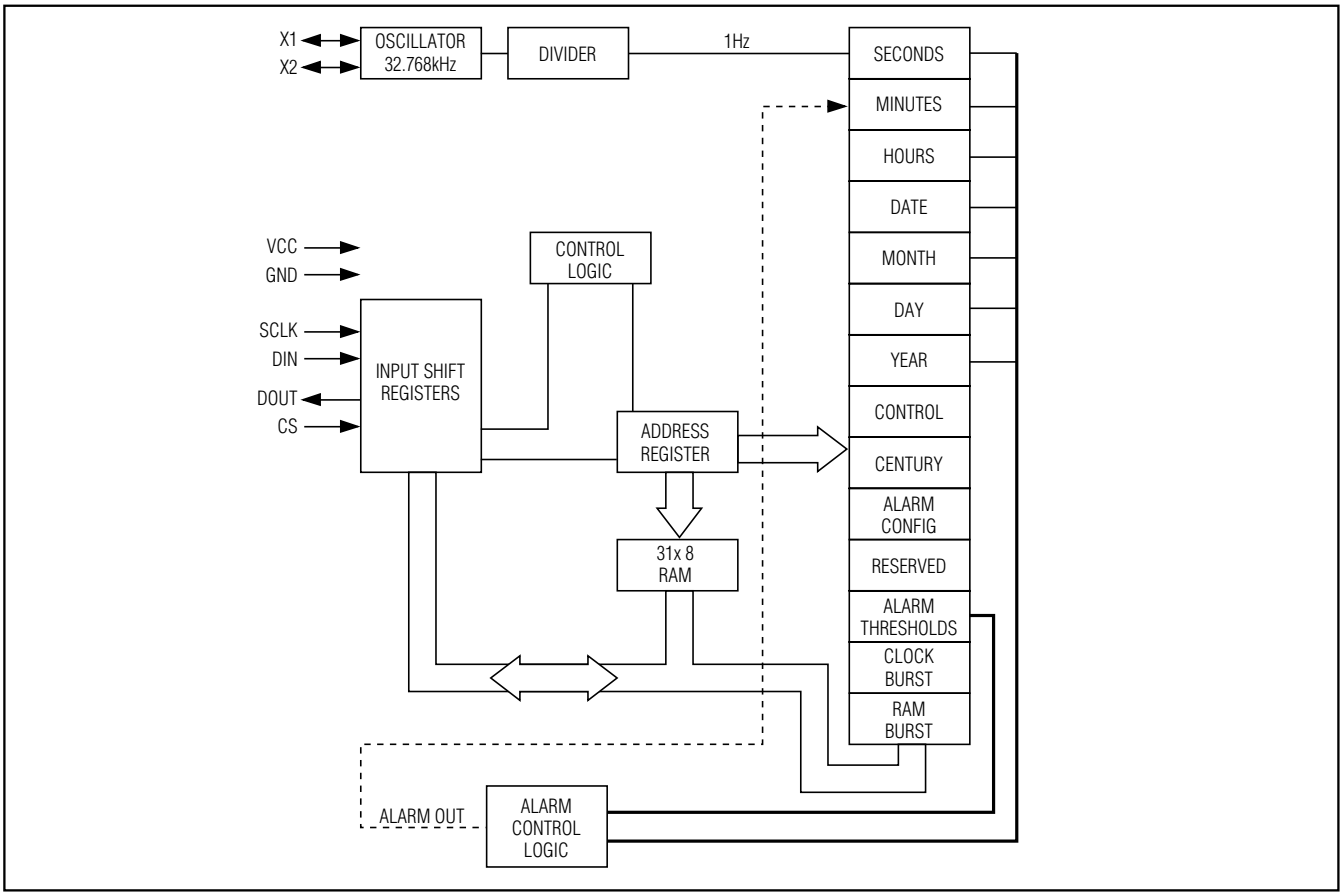


Figure 7. MAX6902 Crystal PC Board Layout

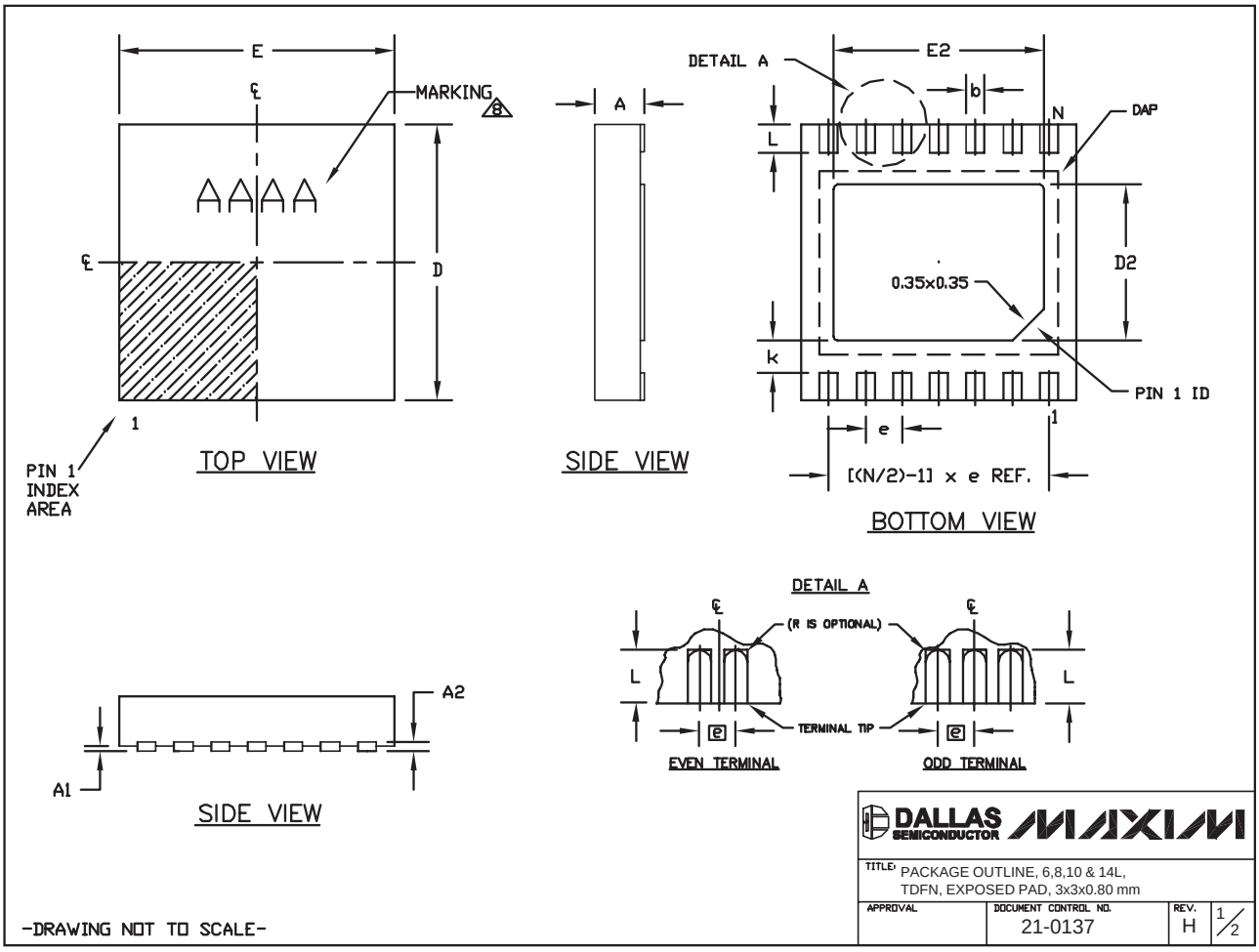
Functional Diagram



SPI-Compatible RTC in a TDFN

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-1	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T633-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T833-1	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1033-2	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 6,8,10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0137	H	2/2

Revision History

Pages changed at Rev 2: 1, 4, 15, 18, 19