The RF MOSFET Line

RF Power Field Effect Transistor

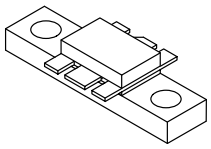
N–Channel Enhancement–Mode

MRF5015

15 W, 512 MHz, 12.5 VOLTS N–CHANNEL BROADBAND RF POWER FET

Designed for broadband commercial and industrial applications at frequencies to 520 MHz. The high gain and broadband performance of this device makes it ideal for large–signal, common source amplifier applications in 12.5 volt mobile, and base station FM equipment.

- Guaranteed Performance at 512 MHz, 12.5 Volts
  Output Power — 15 Watts
  Power Gain — 10 dB Min
  Efficiency — 50% Min
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- S–Parameter Characterization at High Bias Levels
- Excellent Thermal Stability
- All Gold Metal for Ultra Reliability
- Capable of Handling 20:1 VSWR, @ 15.5 Vdc, 512 MHz, 2 dB Overdrive
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.



CASE 319–07, STYLE 3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	36	Vdc
Drain–Gate Voltage (RGS = 1 MΩ)	V_{DGR}	36	Vdc
Gate–Source Voltage	V_{GS}	± 20	Vdc
Drain Current — Continuous	I_D	6	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.29	Watts W/°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.5	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

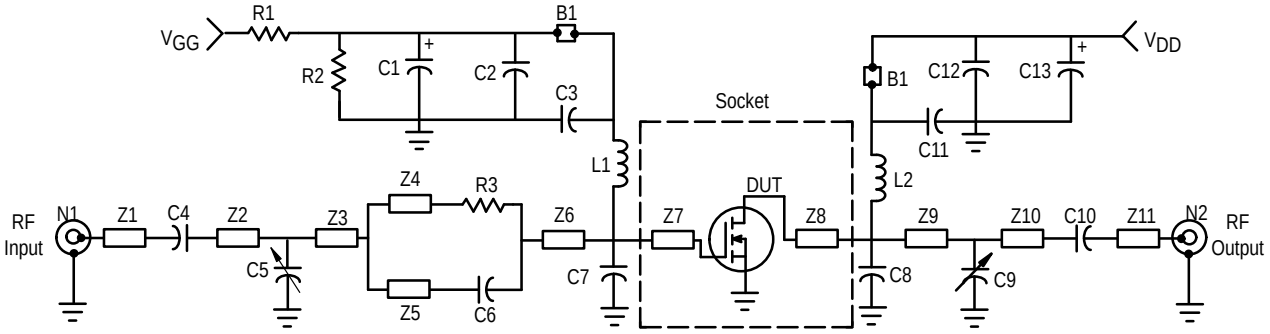
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 5 mAdc)	$V_{(BR)DSS}$	36	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 15 Vdc, V_{GS} = 0)	I_{DSS}	—	—	5	mAdc
Gate–Source Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)	I_{GSS}	—	—	2	μAdc

(continued)

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 10 mAdc)	$V_{GS(th)}$	1.25	2.3	3.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1 Adc)	$V_{DS(on)}$	—	—	0.375	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 1 Adc)	g_{fs}	1.2	—	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 12.5 Vdc, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	33	—	pF
Output Capacitance (V_{DS} = 12.5 Vdc, V_{GS} = 0, f = 1 MHz)	C_{oss}	—	74	—	pF
Reverse Transfer Capacitance (V_{DS} = 12.5 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	7	8.8	10.8	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Common–Source Amplifier Power Gain (V_{DD} = 12.5 Vdc, P_{out} = 15 W, I_{DQ} = 100 mA) f = 512 MHz f = 175 MHz	G_{ps}	10 —	11.5 15	— —	dB
Drain Efficiency (V_{DD} = 12.5 Vdc, P_{out} = 15 W, I_{DQ} = 100 mA) f = 512 MHz f = 175 MHz	η	50 —	55 55	— —	%
Load Mismatch (V_{DD} = 15.5 Vdc, 2 dB Overdrive, f = 512 MHz, Load VSWR = 20:1, All Phase Angles at Frequency of Test)	ψ	No Degradation in Output Power			



B1, B2	Ferrite Bead, Fair Rite Products	R3	160 Ω, 0.1 W Chip
C1, C13	10 µF, 50 V, Electrolytic	Z1, Z11	Transmission Line*
C2, C12	0.1 µF, Chip Capacitor	Z2	Transmission Line*
C3, C4, C10, C11	120 pF, Chip Capacitor	Z3	Transmission Line*
C5, C9	0 to 20 pF, Trimmer Capacitor	Z4	Transmission Line*
C6	36 pF, Chip Capacitor	Z5	Transmission Line*
C7	43 pF, Chip Capacitor	Z6	Transmission Line*
C8	30 pF, Chip Capacitor	Z7, Z8	Transmission Line+
L1, L2	7 Turns, 24 AWG 0.116″ ID	Z9	Transmission Line*
N1, N2	Type N Flange Mount	Z10	Transmission Line*
R1	1 kΩ, 1/4 W, Carbon	Board	Glass Teflon® 0.060″
R2	470 kΩ, 1/4 W, Carbon		+ Part of Capacitor Mount Socket
			*See Photomaster

Figure 1. 512 MHz Narrowband Test Circuit Electrical Schematic

TYPICAL CHARACTERISTICS

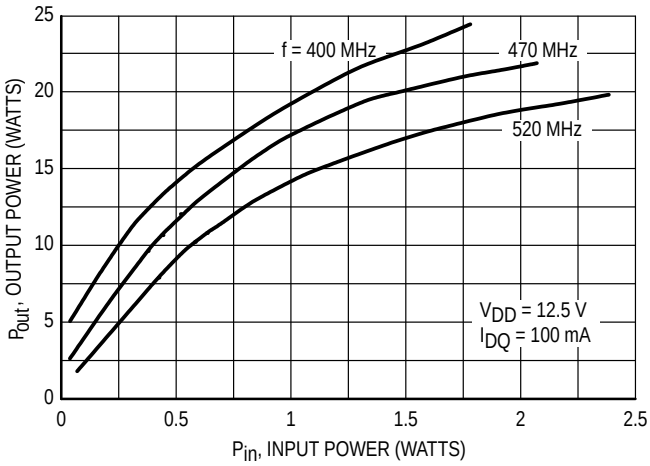


Figure 2. Output Power versus Input Power

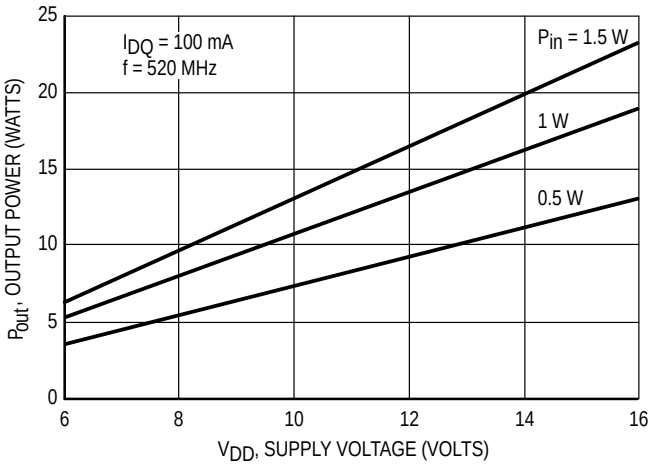


Figure 3. Output Power versus Supply Voltage

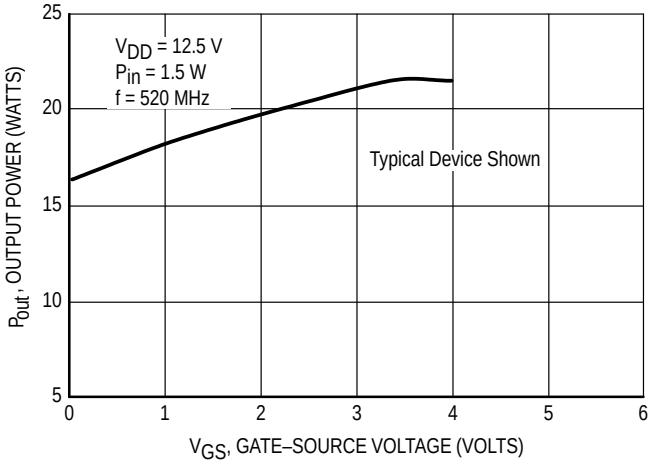


Figure 4. Output Power versus Gate Voltage

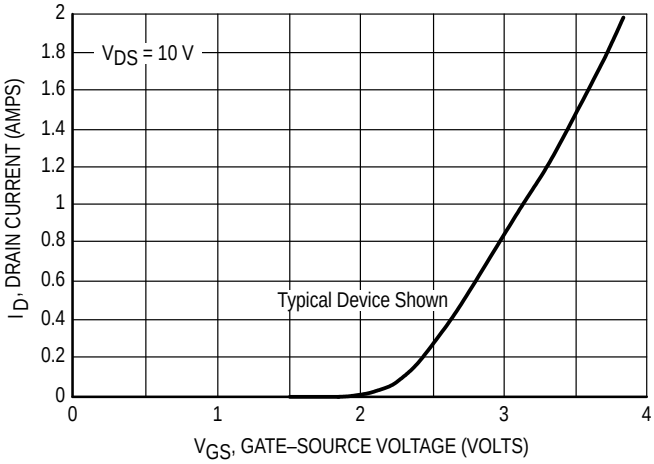


Figure 5. Drain Current versus Gate Voltage

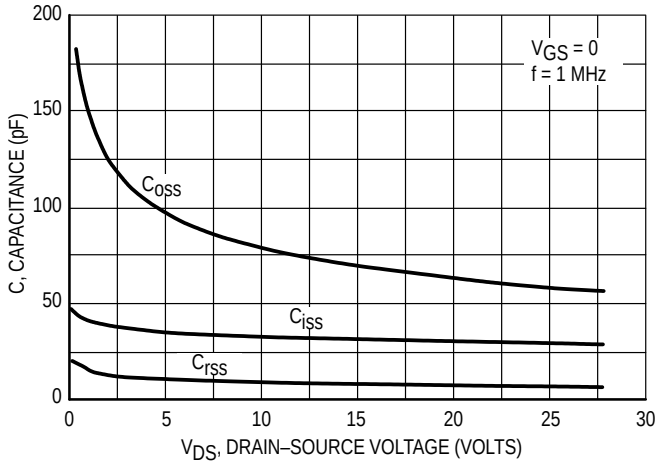


Figure 6. Capacitance versus Voltage

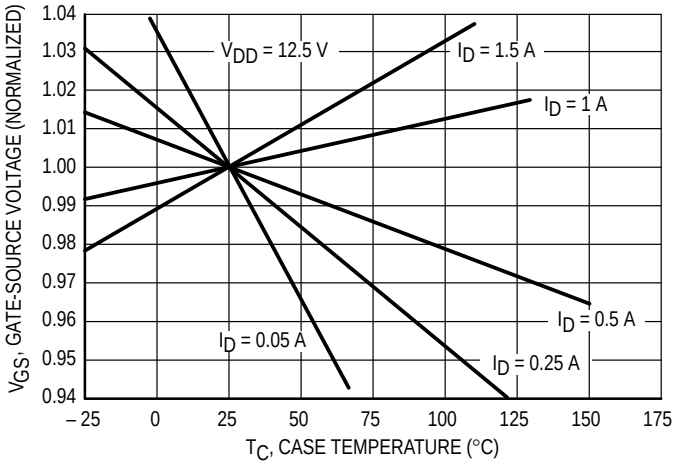


Figure 7. Gate–Source Voltage versus Case Temperature

TYPICAL CHARACTERISTICS

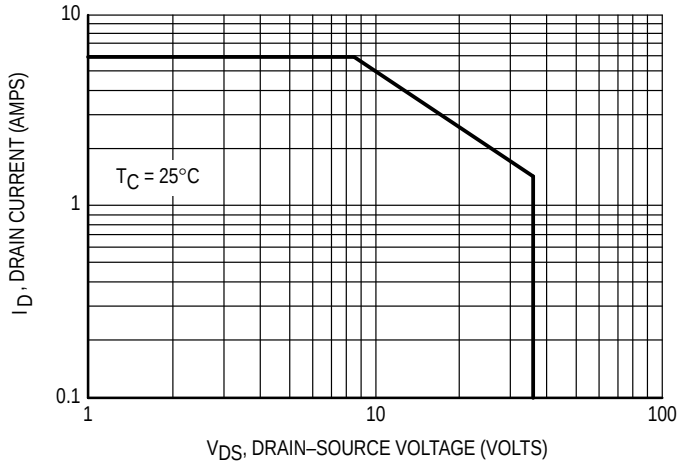
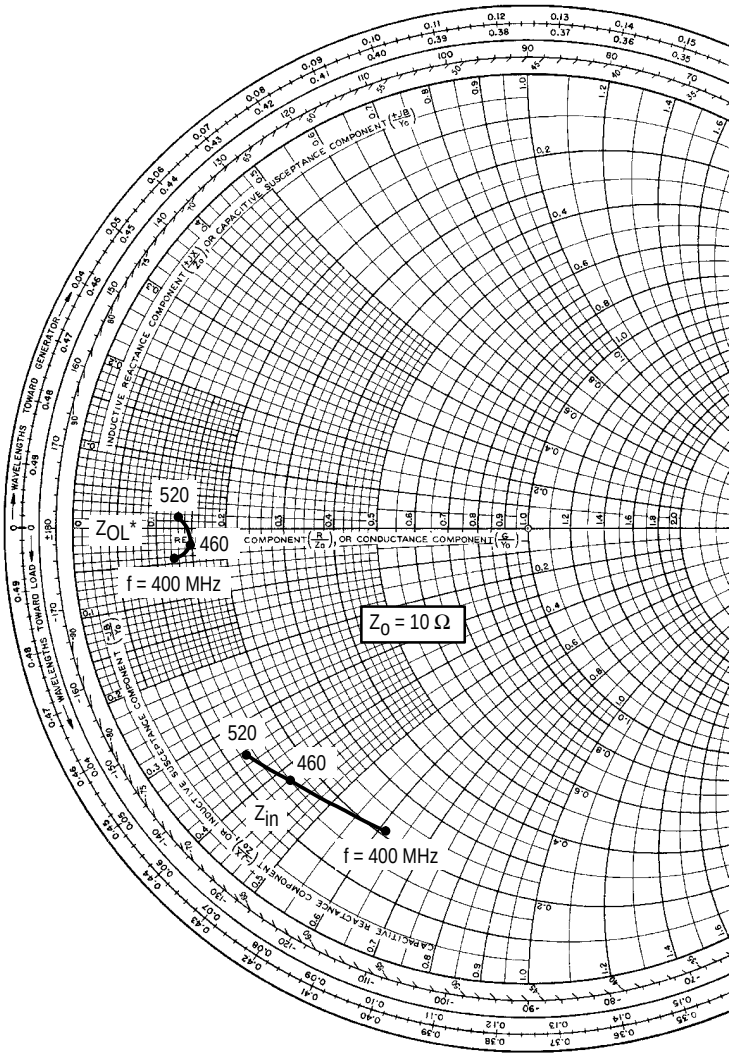


Figure 8. DC Safe Operating Area



V_{DD} = 12.5 V, I_{DQ} = 100 mA, P_{out} = 15 W

f (MHz)	Z_{in} (Ω)	Z_{OL}* (Ω)
400	2.0 – j6.1	1.3 – j0.4
420	1.8 – j5.3	1.4 – j0.4
440	1.6 – j4.7	1.5 – j0.4
460	1.5 – j4.2	1.5 – j0.3
480	1.4 – j3.8	1.5 – j0.2
500	1.3 – j3.6	1.4 – j0.1
520	1.2 – j3.5	1.3 + j0.1

Z_{in} = Conjugate of source impedance with parallel 160 Ω resistor and 36 pF capacitor in series with gate.

Z_{OL}* = Conjugate of the load impedance at given output power, voltage and frequency that produces maximum gain.

Figure 9. Series Equivalent Input and Output Impedance

Table 1. Common Source Scattering Parameters (V_{DS} = 12.5 V)

I_D = 50 mA

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
50	0.63	–123	8	100	0.063	11	0.79	–149
100	0.62	–142	4	82	0.063	– 6	0.82	–162
200	0.70	–152	1.8	61	0.056	– 23	0.86	–169
300	0.78	–157	1.1	47	0.046	– 35	0.90	–171
400	0.84	–162	0.70	36	0.037	– 42	0.93	–174
500	0.88	–165	0.49	28	0.029	– 46	0.94	–175
700	0.93	–171	0.28	17	0.016	– 45	0.97	–179
850	0.95	–175	0.20	13	0.010	– 31	0.97	179
1000	0.96	–178	0.15	10	0.007	11	0.98	178

I_D = 100 mA

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
50	0.67	–136	9.1	99	0.047	10	0.82	–158
100	0.66	–153	4.6	84	0.048	–3	0.85	–168
200	0.71	–160	2.2	66	0.043	–17	0.87	–172
300	0.77	–163	1.3	54	0.037	– 26	0.90	–174
400	0.82	–165	0.89	44	0.031	– 32	0.92	–175
500	0.86	–168	0.64	36	0.025	– 35	0.94	–177
700	0.91	–173	0.37	25	0.015	– 30	0.96	–179
850	0.93	–176	0.27	20	0.010	–11	0.97	179
1000	0.95	–179	0.20	16	0.009	25	0.98	177

I_D = 500 mA

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
50	0.81	–150	11.1	98	0.027	11	0.85	–168
100	0.81	–164	5.6	86	0.027	2	0.87	–174
200	0.82	–170	2.7	73	0.025	– 5	0.88	–176
300	0.84	–173	1.7	63	0.023	– 9	0.89	–177
400	0.86	–174	1.2	55	0.020	– 9	0.91	–178
500	0.88	–175	0.92	47	0.018	– 7	0.92	–179
700	0.91	–178	0.57	35	0.013	7	0.94	180
850	0.93	180	0.43	29	0.013	26	0.95	178
1000	0.94	178	0.33	23	0.014	44	0.96	177

I_D = 2.5 A

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
50	0.86	–144	10.1	101	0.022	15	0.85	–171
100	0.85	–161	5.2	88	0.022	5	0.87	–175
200	0.86	–170	2.5	74	0.021	–1	0.89	–177
300	0.87	–173	1.6	64	0.019	– 4	0.90	–178
400	0.89	–175	1.1	55	0.017	– 2	0.91	–178
500	0.91	–176	0.84	48	0.015	2	0.93	–179
700	0.93	–179	0.52	37	0.013	22	0.95	179
850	0.94	179	0.39	30	0.014	39	0.96	178
1000	0.95	177	0.30	26	0.016	52	0.96	176

DESIGN CONSIDERATIONS

The MRF5015 is a common–source, RF power, N–Channel enhancement mode, Metal–Oxide Semiconductor Field–Effect Transistor (MOSFET). Motorola RF MOSFETs feature a vertical structure with a planar design. Motorola Application Note AN211A, “FETs in Theory and Practice,” is suggested reading for those not familiar with the construction and characteristics of FETs.

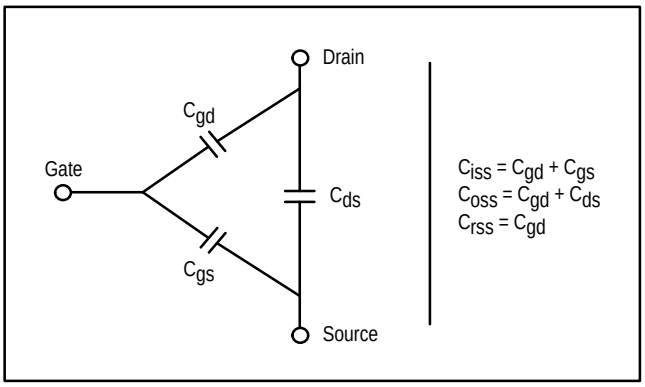
This device was designed primarily for 12.5 volt VHF and UHF power amplifier applications. The major advantages of RF power MOSFETs include high gain, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage.

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between all three terminals. The metal oxide gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during fabrication of the RF MOSFET results in a junction capacitance from drain–to–source (C_{ds}). These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate.

In the latter case, the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



DRAIN CHARACTERISTICS

One critical figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $R_{ds(on)}$, occurs in the linear region of the output characteristic and is specified at a specific gate–source voltage and drain current. The drain–source voltage under these conditions is termed $V_{ds(on)}$. For MOSFETs, $V_{ds(on)}$ has a positive temperature coefficient at high temperatures because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high, on the order of 10^9 Ω, resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage to the gate greater than the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating – Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination – The gates of these devices are essentially capacitors. Circuits that leave the gate open–circuited or floating must be avoided. These conditions can result in turn–on of the devices due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection – These devices do not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended with appropriate RF decoupling networks.

Using a resistor to keep the gate–to–source impedance low also helps dampen transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate–drain capacitance. If the gate–to–source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate–threshold voltage and turn the device on.

DC BIAS

Since the MRF5015 is an enhancement mode FET, drain current flows only when the gate is at a higher potential than the source. See Figure 5 for a typical plot of drain current versus gate voltage. RF power FETs operate optimally with a quiescent drain current (I_{DQ}), whose value is application dependent. The MRF5015 was characterized at I_{DQ} = 100 mA, which is the suggested value of bias current for typical applications. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws essentially no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of the MRF5015 may be controlled to some degree with a low power dc control signal applied to the gate, thus facilitating applications such as manual gain control, ALC/AGC and modulation systems. Figure 4 is an example of output power variation with gate–source bias voltage with P_{in} held constant. This characteristic is very dependent on frequency and load line.

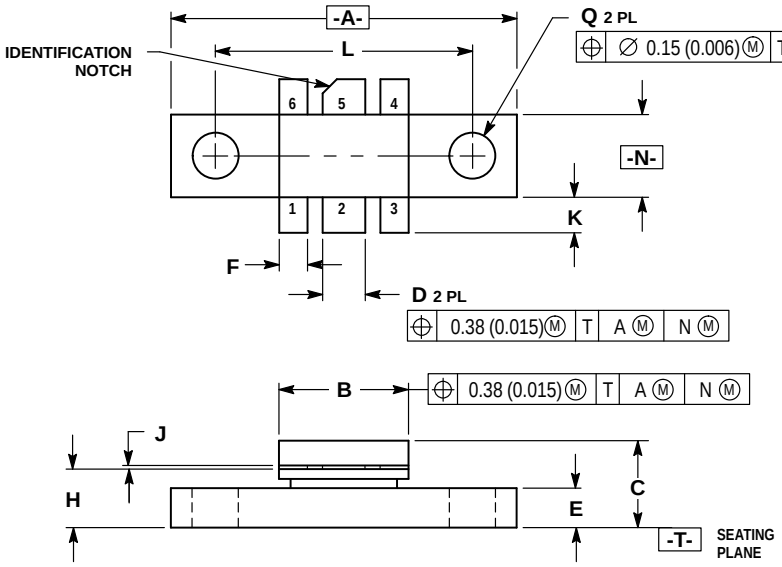
AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar transistors are suitable for the MRF5015. For examples see Motorola Application Note AN721, “Impedance Matching Networks Applied to RF Power Transistors.” Both small–signal S–parameters and large–signal impedances are provided. While the S–parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is an additional advantage of RF power MOSFETs.

Since RF power MOSFETs are triode devices, they are not unilateral. This coupled with the very high gain of MRF5015 yield a device quite capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. Different stabilizing techniques may be required depending on the desired gain and bandwidth of the application. The RF test fixture implements a parallel resistor and capacitor in series with the gate to improve stability and input impedance Q.

Two port stability analysis with the MRF5015 S–parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN215A, “RF Small–Signal Design Using Two–Port Parameters,” for a discussion of two port network theory and stability.

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETER	
DIM	MIN	MAX	MIN	MAX
A	0.965	0.985	24.52	25.01
B	0.355	0.375	9.02	9.52
C	0.230	0.260	5.85	6.60
D	0.115	0.125	2.93	3.17
E	0.102	0.114	2.59	2.90
F	0.075	0.085	1.91	2.15
H	0.160	0.170	4.07	4.31
J	0.004	0.006	0.11	0.15
K	0.090	0.110	2.29	2.79
L	0.725 BSC		18.42 BSC	
N	0.225	0.241	5.72	6.12
Q	0.125	0.135	3.18	3.42

STYLE 3:
PIN 1. SOURCE (COMMON)
2. GATE (INPUT)
3. SOURCE (COMMON)
4. SOURCE (COMMON)
5. DRAIN (OUTPUT)
6. SOURCE (COMMON)

CASE 319–07
ISSUE M

How to reach us:
USA / EUROPE: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE (602) 244–6609
INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, Toshikatsu Otsuki,
6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–3521–8315

HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298