

General Description

The EC9219 include a high-performance step-up regulator, and high-current operational amplifiers for active-matrix thin-film transistor (TFT) liquid-crystal displays (LCDs).

The step-up DC-DC converter provides the regulated supply voltage for the panel source driver ICs. The converter is a high-frequency (1.2MHz or 640KHZ) current-mode regulator with an integrated 18V n-channel MOSFET that allows the use of ultra-small inductors and ceramic capacitors. It provides fast transient response to pulsed loads while achieving efficiencies over 85%.

The EC9219 includes one operational amplifier. These amplifiers are designed to drive the LCD backplane (VCOM) and/or the gamma-correction divider string. The devices feature high output current ($\pm 150\text{mA}$), fast slew rate ($17\text{V}/\mu\text{s}$), wide bandwidth (12MHz), and rail-to-rail inputs and outputs

The EC9219 are available in 14- pin thin TSOP packages with a maximum thickness of 1mm for ultra-thin LCD panels.

Features

- 2.6V to 5.5V Input Supply Range
- 1.2MHz or 640KHZ Current-Mode Step-Up Regulator
- Fast Transient Response to Pulsed Load
- High-Accuracy Output Voltage (2%)
- Built-In 18V, 1.6A, 0.16 Ω N-Channel MOSFET
- High Efficiency (90%)
- High-Performance Operational Amplifiers
- 17V/ μs Slew Rate
- 12MHz, -3dB Bandwidth
- Rail-to-Rail Inputs/Outputs
- Thermal-Overload Protection

Applications

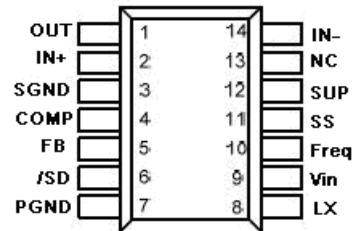
- Notebook Computer Displays ,
- LCD Monitor Panels ,
- Automotive Displays

Ordering information

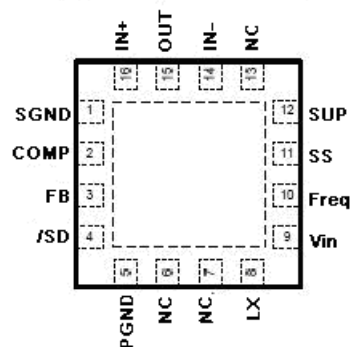
PART NO	MARKING	PACKAGE
EC9219I-G	EC9219-G	TSSOP14 Green Package
EC9219G-G	EC9219G	TQFN16 Green Package

Pin Assignments

TS Package (TSSOP-14)



WQ Package (TQFN-16 4mm×4mm)



NAME	Function
OUT	Operational-Amplifier Output
IN +	Operational-Amplifier Non-inverting Input
SGND	Analog ground.
Comp	Compensation pin. Output of the internal error amplifier. Capacitor and resistor from COMP pin to ground.
FB	Voltage feedback pin. Internal reference is 1.228V nominal. Connect a resistor divider from VOUT. $V_{OUT} = 1.228V (1 + R_3 / R_8)$. See Typical Application Circuit.
/SD	Shutdown control pin. Pull SHDN low to turn off the device, and Soft-start Internal reference voltage control pin, Connect RC Delay circuit.
PGND	Power ground.
LX	Switch Pin. Connect the inductor/catch diode to LX and minimize the trace area for lowest EMI.
Vin	Analog power supply input pin.
Freq	Frequency Select Input. When FREQ is low, the oscillator frequency is set to 640kHz. When FREQ is high the frequency is 1.2MHz.
SS	Soft-start control pin. Connect a capacitor to control the converter start-up.
SUP	Operational-Amplifier Power Input. Positive supply rail for the operational amplifiers. Typically connected to DC-DC converter Output. Bypass SUP to SGND with a 0.1μF capacitor.
NC	
IN -	Operational-Amplifier Inverting Input

Absolute Maximum rating ($T_A = 25^{\circ}\text{C}$)

V_{IN} to SGND	-0.3V to +6V	RMS LX Pin Current	1.6A
Comp, FB, $\overline{SD}$, Freq to SGND	-0.3V to +6V	Operating Ambient Temperature	-40 $^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$
PGND to SGND	$\pm 0.3\text{V}$	Operating Junction Temperature	+125 $^{\circ}\text{C}$
LX to PGND	-0.3V to +18V	Storage temperature	-65 $^{\circ}\text{C}$ to +150 $^{\circ}\text{C}$
SUP, IN+, IN- to SGND	-0.3V to +18V	Lead Temperature	+260 $^{\circ}\text{C}$
Out Maximum Continuous Output Current	$\pm 150\text{mA}$		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

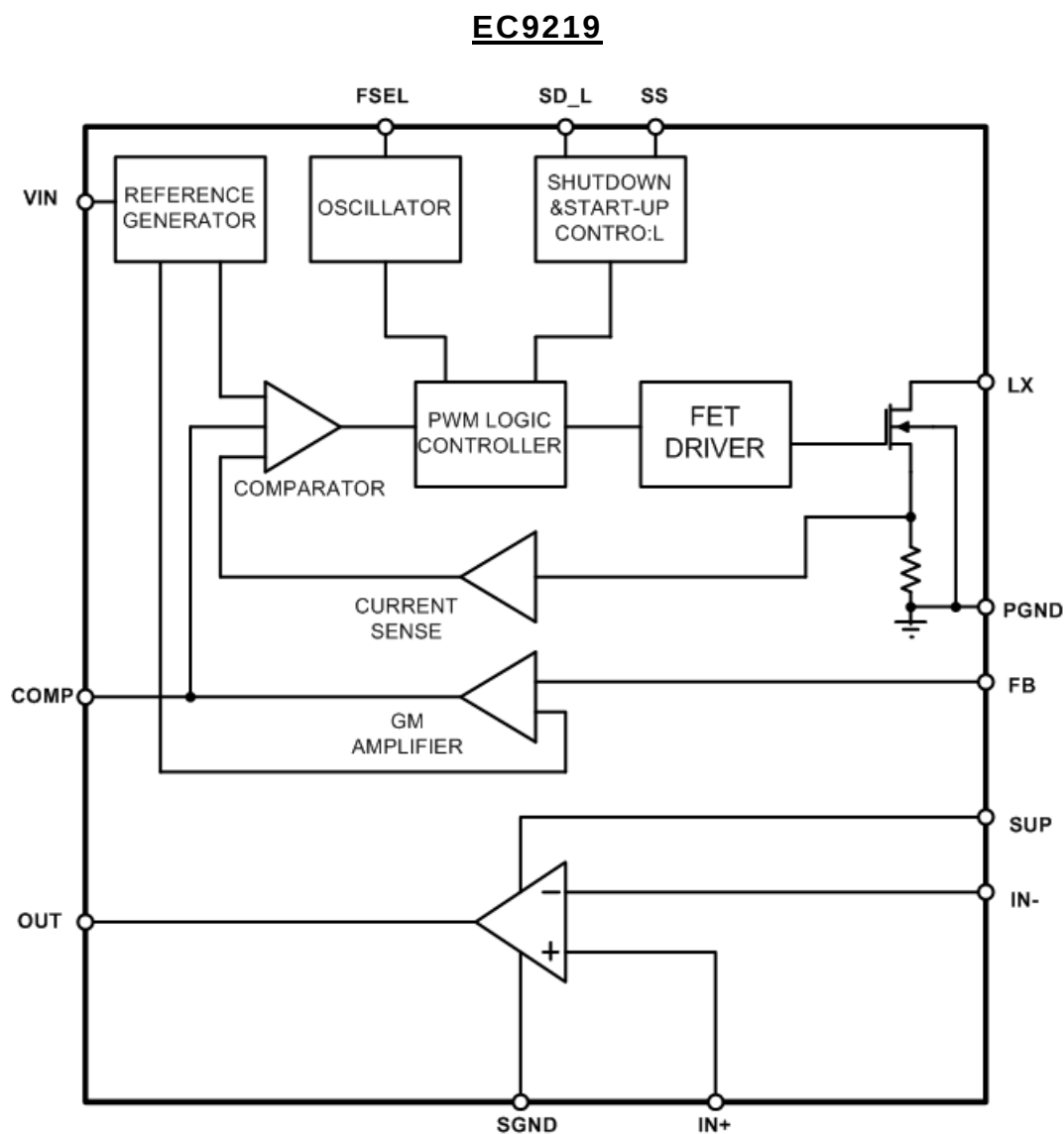
Electrical Specifications

$V_{IN} = 3\text{V}$, $V_{SUP} = 10\text{V}$, FSEL = GND, $T_A = 25^{\circ}\text{C}$ unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
V _{IN} Supply Range	V _{IN}		2.6		5.5	V
V _{IN} Under voltage-Lockout Threshold	V _{UVLO}	V _{IN} rising ,typical hysteresis = 40mV	2.25	2.38	2.52	V
Quiescent Current	I _{IN}	$\overline{SD}$ = V _{IN} ,V _{FB} =1.3, not switching		0.4	1	mA
		$\overline{SD}$ = V _{IN} ,V _{FB} =COMP, switching		4	5	mA
Shutdown Supply Current	I _{IN}	$\overline{SD}$ = SGND include OP.		0.1	1	uA
Input Low Level	V _{IL}	$\overline{SD}$, Freq ;V _{IN} = 3 V to 5.5V			0.3V _{IN}	V
Input High Level	V _{IH}	$\overline{SD}$, Freq ;V _{IN} = 3 V to 5.5V	0.7V _{IN}			V
Hysteresis		$\overline{SD}$, Freq ;V _{IN} = 3 V to 5.5V		0.1V _{IN}		V
Freq Input Current		Freq =V _{IN}		1		nA
$\overline{SD}$ Input Current		$\overline{SD}$ =V _{IN}		1		nA
Thermal Shutdown		Temperature rising		130		°C
		Hysteresis		30		°C
Main STEP-UP REGULATOR						
Output Voltage Range	V _{main}		V _{IN}		18	V
Frequency	f _{osc}	Freq=GND	500	640	750	kHz
		Freq= V _{IN} ,	1000	1200	1500	kHz
Maximum Duty Cycle	D	Freq=GND	85	90	95	%
		Freq= V _{IN} ,	85	90	95	%
FB Regulation Voltage	V _{FB}	load=50mA	1.222	1.24	1.258	V
FB Line Regulation		V _{IN} =2.6V to 5.5V			0.5	%
FB Input Bias Current		V _{FB} =1.4		1		nA
Voltage Gain	A _v	FB to Comp		1000		V/V
Swich On-Resistance	R _{ds(on)}			160	250	mΩ
LX Leakage Current	I _{LX}	V _{LX} =18V		1.8		uA
LX Current Limit				2		A
Current-Sense Tran conductance	R _{cs}			0.047		V/A
OPEATIONAL AMPLIFIERS						
SUP Supply Range	V _{sup}		4.5		18	V
SUP Supply Current	I _{sup}	Buffer configuration ,no load OUT=4V,V _{sup} =8V		2.8	4	mA
Input Offset Voltage	V _{OS}	OUT= V _{sup} /2			20	mV
Input Bias Current	I _{BIAS}	OUT= V _{sup} /2		2	50	nA
Input Common-Mode Range	V _{CM}		0		V _{sup}	V
Common-Mode Rejection Ratio	CMRR		50	70		dB
Open-Loop Gain	A _v		75	100		dB
Output Voltage Swing ,High	V _{OH}	I _{OUT} =5mA	V _{sup} -150	V _{sup} -80		mV
Output Voltage Swing ,Low	V _{OL}	I _{OUT} =-5mA		70	150	mV
Power-Supply Rejection Ratio	PSRR		60	70		dB

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Slew Rate	SR	$V_{in}=4V, V_{IN+}=6V, R_L=2k\Omega, C_L=100\text{ pF}$ buffer configuration	10	17		V/ μ s
-3dB Bandwidth		$R_L=2k\Omega, C_L=100\text{ pF}$ buffer configuration		12		MHz
Gain-Bandwidth Product	GBP	$R_L=2k\Omega, C_L=100\text{pF}$ buffer configuration		8		MHz

Block Diagram



Typical Application Circuit

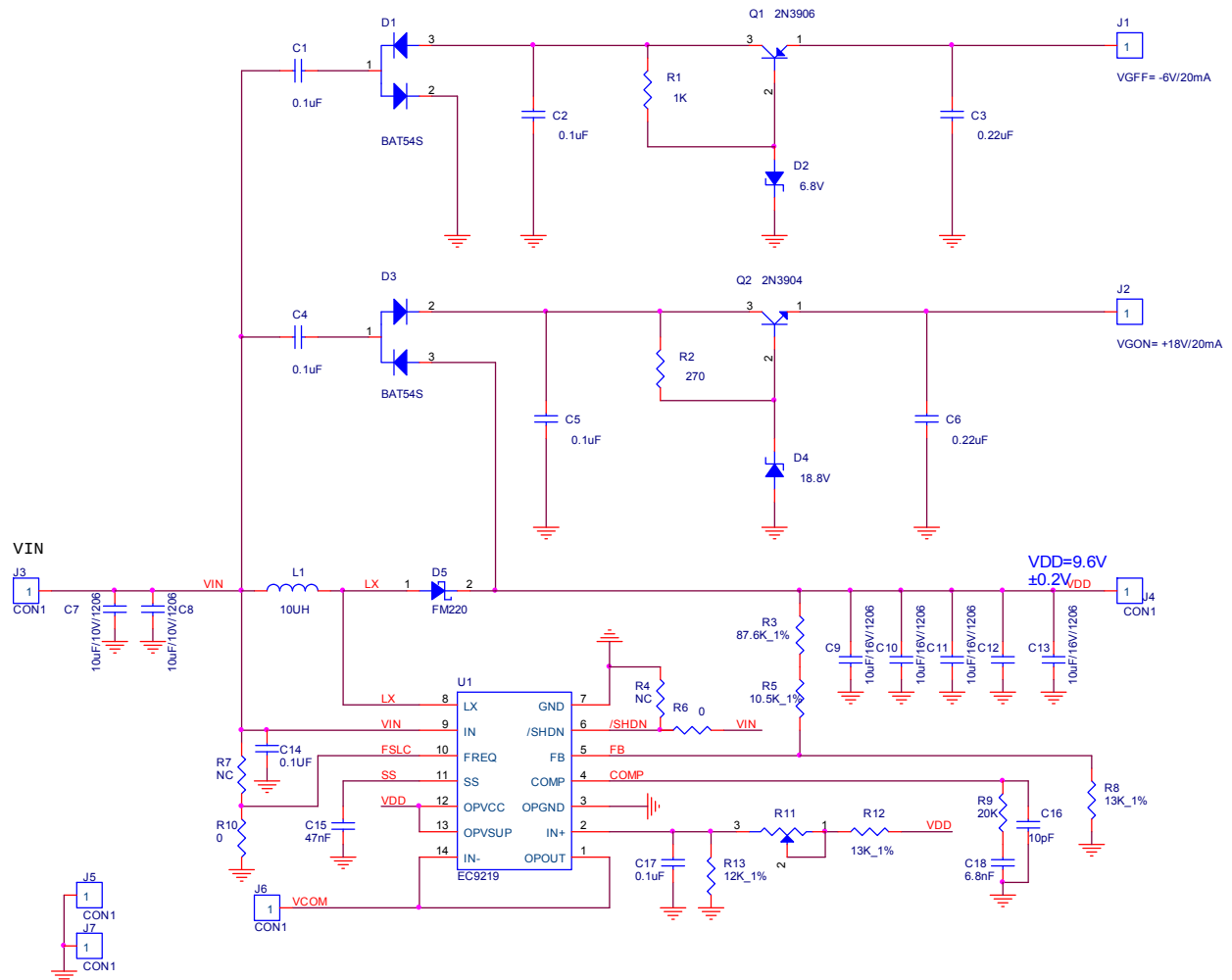
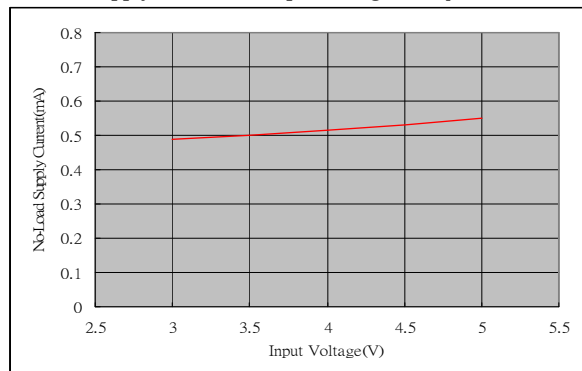


Figure 2

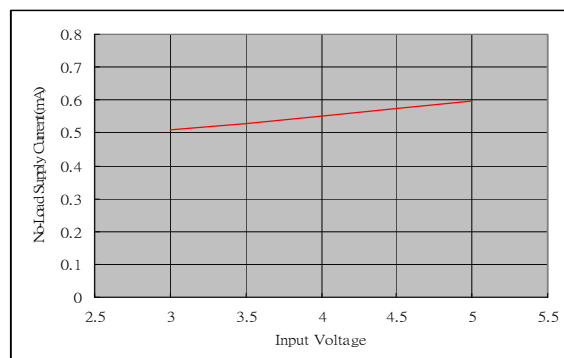
Typical operating Characteristics

Typical Application Circuit, $V_{in}=3.3V$, $V_{MAIN}=9.6$, $V_{GON}=18V$, $V_{GOFF}=-6V$, $OUT=6V$, $Freq=V_{in}$ $T_A=25^{\circ}C$ unless otherwise noted.)

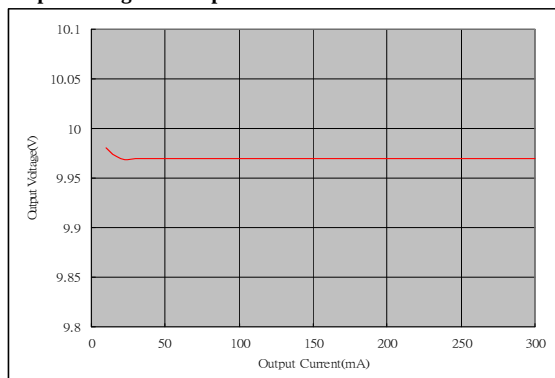
No-Load Supply Current vs. Input Voltage Freq=640kHz



No-Load Supply Current vs. Input Voltage Freq=1.2MHz

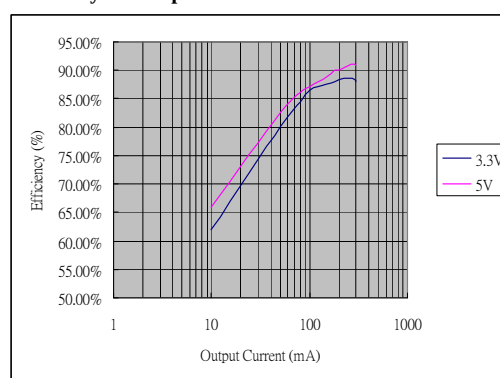


Output Voltage vs. Output Current



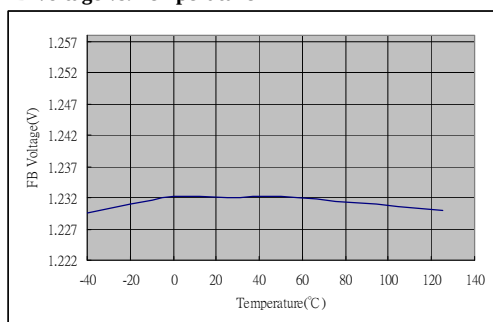
$V_{out}=10V, V_{in}=3.3V, L=10\mu H, Freq=640KHz$

Efficiency vs. Output Current

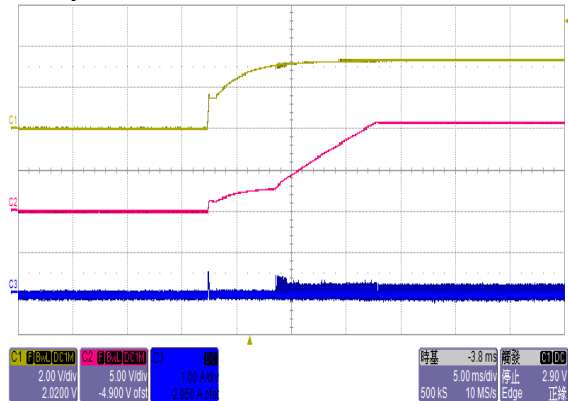


$V_{out}=9.6V, L=10\mu H, Freq=640kHz$

FB Voltage vs. Temperature



Start-up Waveform with Soft-start



CH1: Vin

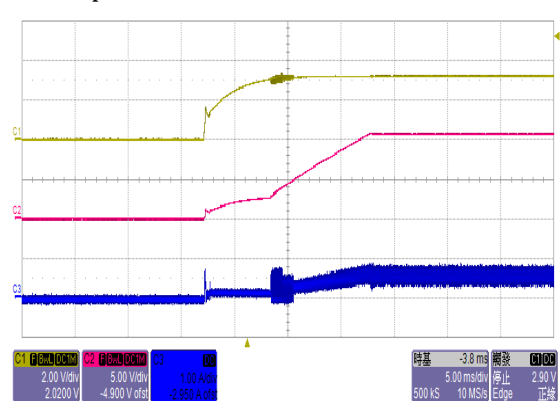
CH2: Output Voltage

CH3: Inductor Current

Vin=3.3V, Iout=10mA, Freq=640KHz,

Vout=10.6V, Cout=30uF

Start-up Waveform with Soft-start



CH1: Vin

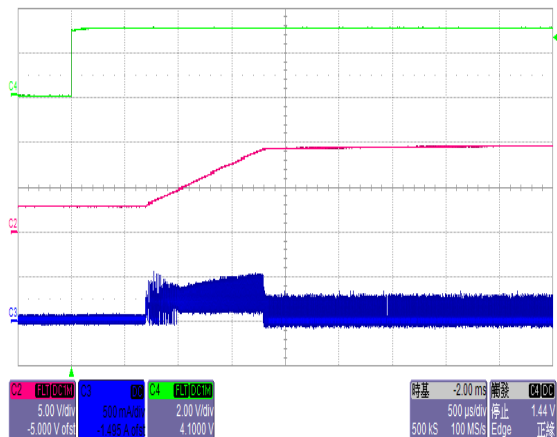
CH2: Output Voltage

CH3: Inductor Current

Vin=3.3V, Iout=200mA, Freq=640KHz,

Vout=10.6V, Cout=30uF

Start-up Waveform with Soft-start



CH4: SHDN

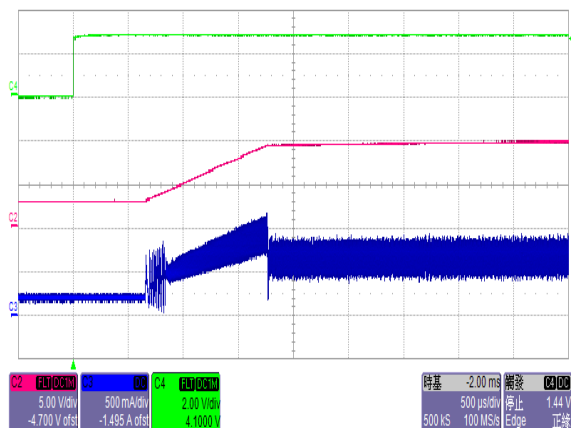
CH2: Output Voltage

CH3: Inductor Current

Vin=3.3V, Iout=10mA, Freq=640KHz,

Vout=9.6V, Cout=30uF

Start-up Waveform with Soft-start



CH1: SHDN

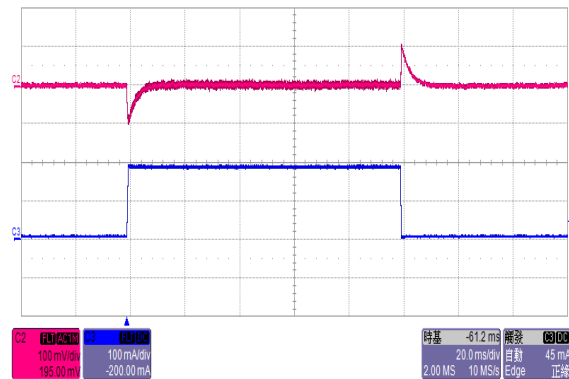
CH2: Output Voltage

CH3: Inductor Current

Vin=3.3V, Iout=200mA, Freq=640KHz,

Vout=9.6V, Cout=30uF

Load-Transient Response



CH2: Output Voltage,AC-Coupled

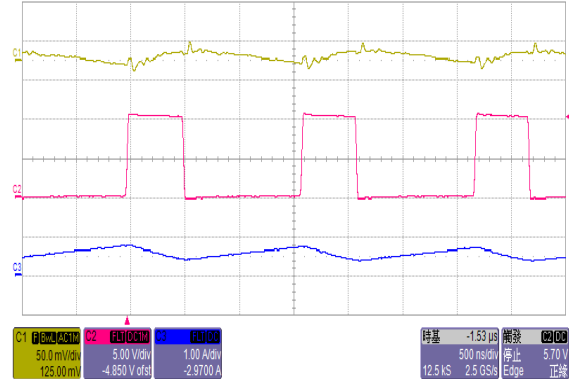
CH3:Load Current

Vin=3.3V,Vout=10V,Freq=640KHz

Figure 7. Start-up Waveform with Soft-start

Vin=3.3V,Vout=10V,Iout=200mA,Freq=640KHz,L=10uH

SWITCHING WAVEFORM

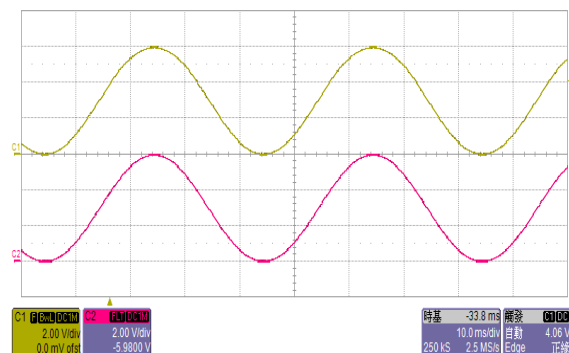


CH1:Output Voltage,AC-Coupled

Ch3:Inductor Current

Ch2:LX Switching Waveform

Operational-Amplifier RAIL-TO-RAIL INPUT/OUTPUT

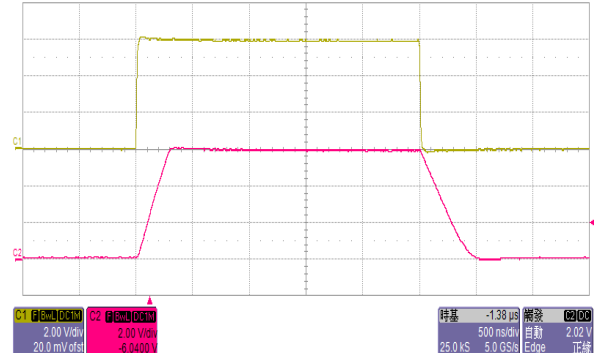


CH1: Input signal

CH2:Output signal

VSUP:12V,RL:2K,CL:100P

Operational-Amplifier Large-Signal Step Response



CH1: Input signal

CH2:Output signal

VSUP:12V,RL:2K,CL:100P

Typical Operating Circuit

The EC9219 Typical Operating Circuit (Figure 2) is a complete power-supply system for TFT LCDs. The circuit generates a +9.6V source-driver supply and +18V and -6V gate-driver supplies. The input voltage range for the IC is from +2.6V to +5.5V. The listed load currents in Figure 1 are available from a +4.5V to +5.5V supply. Typical Operating Circuit recommended components,.

Applications Information

The EC9219 is a high frequency, high efficiency boost regulator operated at constant frequency PWM mode. The boost converter stores energy from an input voltage source and deliver it to a higher output voltage. The input voltage range is 2.6V to 5.5V and output voltage range is 5V to 18V The switching frequency is selectable between 640KHz and 1.2MHz allowing smaller inductors and faster transient response. An external compensation pin gives the user greater flexibility in setting output transient response and tighter load regulation. The converter soft-start characteristic can also be controlled by external C08 capacitor. The SHDN pin allows the user to completely shut-down the device.

Main Step-Up Regulator

The main step-up regulator employs a current-mode, fixed-frequency PWM architecture to maximize loop bandwidth and provide fast transient response to pulsed loads typical of TFT-LCD panel source drivers. The 1.2MHz switching frequency allows the use of low profile inductors and ceramic capacitors to minimize the thickness of LCD panel designs. The integrated high-efficiency MOSFET and soft-start function controls inrush currents. The output voltage can be set from VIN to 13V with an external resistive voltage-divider. The regulator controls the output voltage and the power delivered to the output by modulating the duty cycle (D) of the internal power MOSFET in each switching cycle. The duty cycle of the MOSFET is approximated by:

$$D = \frac{V_{MAIN} - V_{IN}}{V_{MAIN}}$$

Figure 1 shows the *Functional Diagram* of the step-up regulator. An error amplifier compares the signal at FB to 1.228V and changes the COMP output. The voltage at COMP sets the peak inductor current. As the load varies, the error amplifier sources or sinks current to the COMP output accordingly to produce the inductor peak current necessary to service the load. To maintain stability at high duty cycles, a slope-compensation signal is summed with the current-sense signal. On the rising edge of the internal clock, the controller sets a flip-flop, turning on the n-channel MOSFET and applying the input voltage across the inductor. The current through the inductor ramps up linearly, storing energy in its magnetic field. Once the sum of the current-feedback signal and the slope compensation exceeds the COMP voltage, the controller resets the flip-flop and turns off the MOSFET. Since the inductor current is continuous, a transverse potential develops across the inductor that turns on the diode (D1). The voltage across the inductor then becomes the difference between the output voltage and the input voltage. This discharge condition forces the current through the inductor to ramp back down, transferring the energy stored in the magnetic field to the output capacitor and the load. The MOSFET remains off for the rest of the clock cycle.

Operational Amplifiers

The EC9219 has one operational amplifier. The operational amplifiers are typically used to drive the LCD backplane (VCOM) or the gamma-correction divider string. They feature 150mA output current, 17V/ μ s slew rate, and 12MHz bandwidth. The rail-to-rail input and output capability maximizes system flexibility.

Frequency Selection

The EC9219's frequency can be user selected to operate at either 640kHz or 1.2MHz. Tie FREQ to GND for 640kHz operation. For a 1.2MHz switching frequency, tie FREQ to VIN.

Under voltage Lockout (UVLO)

The under voltage-lockout (UVLO) circuit compares the input voltage at VIN with the UVLO threshold to ensure the input voltage is high enough for reliable operation. The 100mV (typ) hysteresis prevents supply transients from causing a restart. Once the input voltage exceeds the UVLO rising threshold, startup begins. When the input voltage falls below the UVLO falling threshold, the controller turns off the main step-up regulator, turns off the outputs, and disables the switch control block; the operational amplifier outputs are high impedance.

Thermal-Overload Protection

Thermal-overload protection prevents excessive power dissipation from overheating the EC9219. When the junction temperature exceeds $T_J = +135^{\circ}\text{C}$, a thermal sensor immediately activates the fault protection, which shuts down all outputs except the reference, allowing the device to cool down. Once the device cools down by approximately 30°C , and reactivate the device. The thermal-overload protection protects the controller in the event of fault conditions. For continuous operation, do not exceed the absolute maximum junction temperature rating of $T_J = +125^{\circ}\text{C}$.

Design Procedure Main Step-Up Regulator Inductor Selection

The minimum inductance value, peak current rating, and series resistance are factors to consider when selecting the inductor. These factors influence the converter's efficiency, maximum output load capability, transient-response time, and output voltage ripple. Size and cost are also important factors to consider. The maximum output current, input voltage, output voltage, and switching frequency determine the inductor value. Very high inductance values minimize the current ripple and therefore reduce the peak current, which decreases core losses in the inductor and RL losses in the entire power path. However, large inductor values also require more energy storage and more turns of wire, which increases size and can increase winding resistance losses in the inductor. Low inductance values decrease the size but increase the current ripple and peak current. Finding the best inductor involves choosing the best compromise between circuit efficiency, inductor size, and cost. The equations used here include a constant ICR(Inductor current ripple rate), which is the ratio of the inductor peak-to-peak ripple current to the average DC inductor current at the full load current. The best trade-off between inductor size and circuit efficiency for step-up regulators generally has an ICR between 0.3 and 0.5. However, depending on the AC characteristics of the inductor core material and ratio of inductor resistance to other power-path resistances, the best ICR can shift up or down. If the inductor resistance is relatively high, more ripple can be accepted to reduce the number of turns required and increase the wire diameter. If the inductor resistance is relatively low, increasing inductance to lower the peak current can decrease losses throughout the power path. If extremely thin high-resistance inductors are used, as is common for LCD-panel applications, the best ICR can increase to between 0.5 and 1.0. Once a physical inductor is chosen, higher and lower values of the inductor should be evaluated for efficiency improvements in typical operating regions. Calculate the approximate inductor value using the typical input voltage (VIN), the maximum output current (IMAIN(MAX)), the expected efficiency (η TYP) taken from an appropriate curve in the Typical Operating Characteristics section, and an estimate of ICR based on the above discussion:

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$$L = \left(\frac{V_{IN}}{V_{MAIN}} \right)^2 \left(\frac{V_{MAIN} - V_{IN}}{I_{MAIN(MAX)} \times f_{OSC}} \right) \left(\frac{\eta_{TYP}}{ICR} \right)$$

Choose an available inductor value from an appropriate inductor family. Calculate the maximum DC input current at the minimum input voltage ($V_{IN(MIN)}$) using conservation of energy and the expected efficiency at that operating point (η_{MIN}) taken from the appropriate curve in the *Typical Operating Characteristics*:

$$I_{IN(DC,MAX)} = \frac{I_{MAIN(MAX)} \times V_{MAIN}}{V_{IN(MIN)} \times \eta_{MIN}}$$

Calculate the ripple current at that operating point and the peak current required for the inductor:

$$I_{RIPPLE} = \frac{V_{IN(MIN)} \times (V_{MAIN} - V_{IN(MIN)})}{L \times V_{MAIN} \times f_{OSC}}$$

$$I_{PEAK} = I_{IN(DC,MAX)} + \frac{I_{RIPPLE}}{2}$$

The inductor's saturation current rating and the EC9219s' LX current limit (I_{LIM}) should exceed I_{PEAK} , and the inductor's DC current rating should exceed $I_{IN(DC,MAX)}$. For good efficiency, choose an inductor with less than 0.1 Ω series resistance. Considering the *Typical Operating Circuit*, the maximum load current ($I_{MAIN(MAX)}$) is 500mA with a 13V output and a typical input voltage of 5V. Choosing an ICR of 0.5 and estimating efficiency of 85% at this operating point:

$$L = \left(\frac{5V}{13V} \right)^2 \left(\frac{13V - 5V}{0.5A \times 1.2MHz} \right) \left(\frac{0.85}{0.5} \right) \approx 3.3\mu H$$

Using the circuit's minimum input voltage (4.5V) and estimating efficiency of 80% at that operating point:

$$I_{IN(DC,MAX)} = \frac{0.5A \times 13V}{4.5V \times 0.8} \approx 1.8A$$

The ripple current and the peak current are:

$$I_{RIPPLE} = \frac{4.5V \times (13V - 4.5V)}{3.3\mu H \times 13V \times 1.2MHz} \approx 0.74A$$

$$I_{PEAK} = 1.8A + \frac{0.74A}{2} \approx 2.2A$$

Output-Capacitor Selection

The total output voltage ripple has two components: the capacitive ripple caused by the charging and discharging of the output capacitance, and the ohmic ripple due to the capacitor's equivalent series resistance (ESR).

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)}$$

$$V_{RIPPLE(C)} \approx \frac{I_{MAIN}}{C_{OUT}} \left(\frac{V_{MAIN} - V_{IN}}{V_{MAIN} f_{OSC}} \right), \text{ and}$$

$$V_{RIPPLE(ESR)} \approx I_{PEAK} R_{ESR(COUT)}$$

where I_{PEAK} is the peak inductor current (see the *Inductor Selection* section). For ceramic capacitors, the output voltage ripple is typically dominated by $V_{RIPPLE(C)}$. The voltage rating and temperature characteristics of the output capacitor must also be considered.

Input-Capacitor Selection

The input capacitor (CIN) reduces the current peaks drawn from the input supply and reduces noise injection into the IC. A 10μF ceramic capacitor is used in the *Typical Applications Circuit* (Figure 2) because of the high source impedance seen in typical lab setups. Actual applications usually have much lower source impedance since the step-up regulator often runs directly from the output of another regulated supply. Typically, CIN can be reduced below the values used in the *Typical Applications Circuit*. Ensure a low-noise supply at VIN by using adequate CIN. Alternately, greater voltage variation can be tolerated on CIN if VIN is decoupled from CIN using an RC low-pass filter.

Rectifier Diode

The EC9219s' high switching frequency demands a high-speed rectifier. Schottky diodes are recommended for most applications because of their fast recovery time and low forward voltage. In general, a 2A Schottky diode complements the internal MOSFET well.

Output-Voltage Selection

The output voltage of the main step-up regulator can be adjusted by connecting a resistive voltage-divider from the output (VMAIN) to AGND with the center tap connected to FB (see Figure 2). Select R2 in the 10kΩ to 50kΩ range. Calculate R1 with the following equation:

$$R3 = R8 \times \left(\frac{V_{\text{main}}}{V_{\text{FB}}} - 1 \right)$$

where VFB, the step-up regulator's feedback set point, is 1.228V. Place R3 and R8 close to the IC.

Loop Compensation

The EC9219 incorporates an trans conductance amplifier in its feedback path to allow the user some adjustment on the transient response and better regulation. The EC9219 uses current mode control architecture which has a fast current sense loop and a slow voltage feedback loop. The fast current feedback loop does not require any compensation. The slow voltage loop must be compensated for stable operation. The compensation network is a series RC network from COMP pin to ground. The resistor sets the high frequency integrator gain for fast transient response and the capacitor sets the integrator zero to ensure loop stability. For most applications, the compensation resistor in the range of 10K to 100K and the compensation capacitor in the range of 1nF to 0.22μF.

PC Board Layout and Grounding

Careful PC board layout is important for proper operation. Use the following guidelines for good PC board layout:

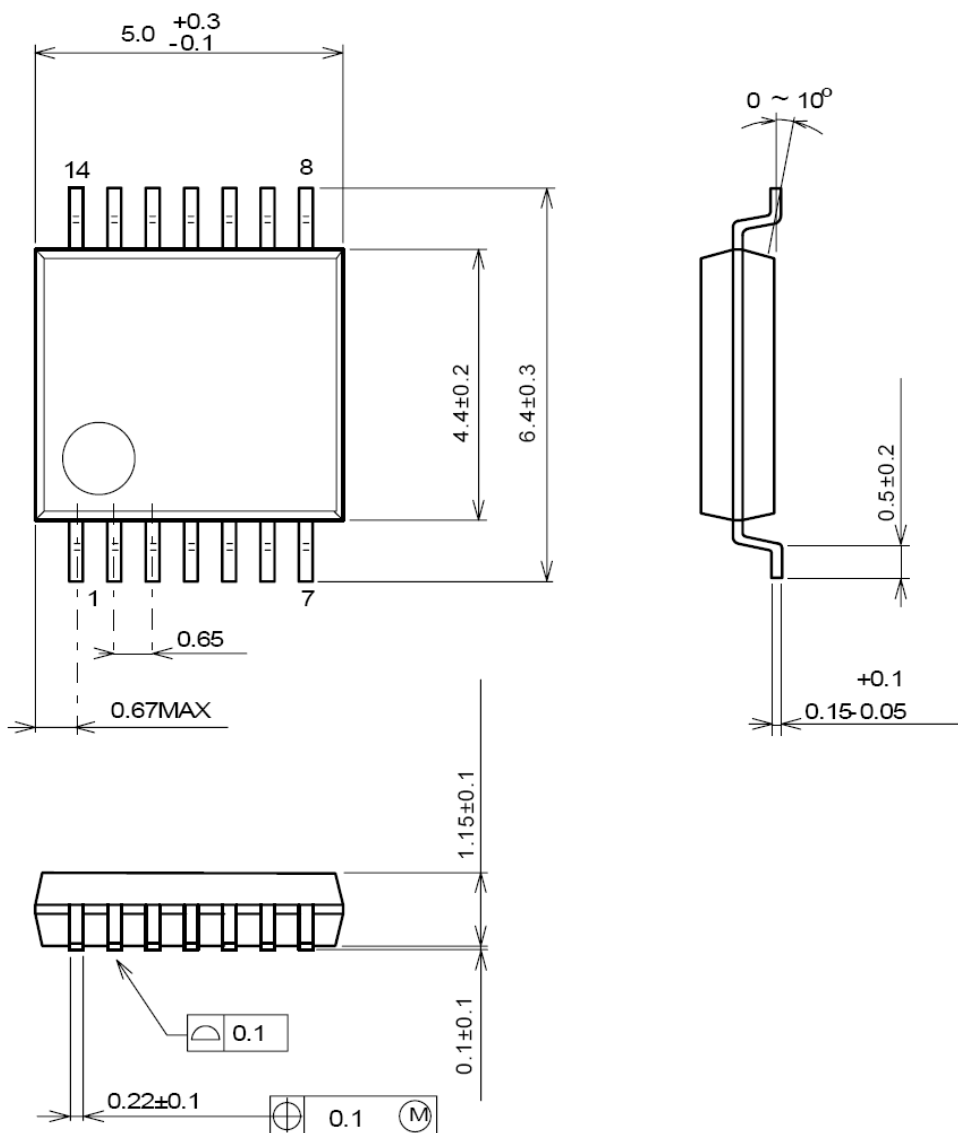
- Minimize the area of high-current loops by placing the inductor, the output diode, and the output capacitors near the input capacitors and near the LX and PGND pins. The high-current input loop goes from the positive terminal of the input capacitor to the inductor, to the IC's LX pin, out of PGND, and to the input capacitor's negative terminal. The high-current output loop is from the positive terminal of the input capacitor to the inductor, to the output diode (D5), and to the positive terminal of the output capacitors, reconnecting between the output capacitor and input capacitor ground terminals. Connect these loop components with short, wide connections. Avoid using vias in the high-current paths. If vias are unavoidable, use many vias in parallel to reduce resistance and inductance.
- Create a power-ground island (PGND) consisting of the input and output capacitor grounds, PGND pin, and any charge-pump components. Connect all of these together with short, wide traces or a small ground plane. Maximizing the width of the power-ground traces improves efficiency and reduces output voltage ripple and noise spikes. Create an analog ground plane (SGND) consisting of the SGND pin, all the feedback-divider ground connections, the COMP and SS capacitor ground connections. Connect the SGND and PGND islands. Make no other connections between these separate ground planes.

- Place all feedback voltage-divider resistors as close to their respective feedback pins as possible. The divider's center trace should be kept short. Placing the resistors far away causes their FB traces to become antennas that can pick up switching noise. Take care to avoid running any feedback trace near LX or the switching nodes in the charge pumps.
- Place the VIN pin bypass capacitors as close to the device as possible. The ground connection of the VIN bypass capacitor should be connected directly to the SGND pin with a wide trace.
- Minimize the length and maximize the width of the traces between the output capacitors and the load for best transient responses.
- Minimize the size of the LX node while keeping it wide and short. Keep the LX node away from feedback nodes (FB) and analog ground. Use DC traces to shield if necessary.

Refer to the EC9219 DEMO BOARD for an example of proper PC board layout.

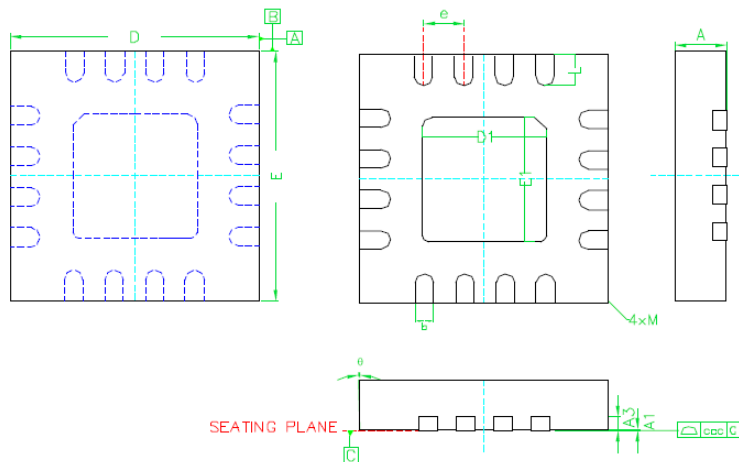
Package Dimension

TSSOP-14



Unit:mm

TQFN-16



SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.010	0.030
A3	—	0.20REF.	—
b	0.25	0.30	0.35
D	3.95	4.00	4.03
D1	—	2.60BSC	—
E	3.95	4.00	4.03
E1	—	2.60BSC	—
e	—	0.65BSC	—
L	0.35	0.40	0.45
θ	-12	—	0
ccc	—	0.08	—
M	—	—	0.05
Burr	0	0.030	0.060

For informational purpose only and is subject to change without notice