15 MHz Rail-to-Rail Operational Amplifiers

OP162/OP262/OP462

FEATURES

Wide bandwidth: 15 MHz
Low offset voltage: 325 µV max
Low noise: 9.5 nV/√Hz @ 1 kHz
Single-supply operation: 2.7 V to 12 V
Rail-to-rail output swing
Low TCV_{OS}: 1 µV/°C typ
High slew rate: 13 V/µs
No phase inversion
Unity-gain stable

APPLICATIONS

Portable instrumentation
Sampling ADC amplifier
Wireless LANs
Direct access arrangement
Office automation

GENERAL DESCRIPTION

The OP162 (single), OP262 (dual), and OP462 (quad) rail-to-rail 15 MHz amplifiers feature the extra speed new designs require, with the benefits of precision and low power operation. With their incredibly low offset voltage of 45 µV (typical) and low noise, they are perfectly suited for precision filter applications and instrumentation. The low supply current of 500 µA (typical) is critical for portable or densely packed designs. In addition, the rail-to-rail output swing provides greater dynamic range and control than standard video amplifiers.

These products operate from single supplies as low as 2.7 V to dual supplies of ±6 V. The fast settling times and wide output swings recommend them for buffers to sampling A/D converters. The output drive of 30 mA (sink and source) is needed for many audio and display applications; more output current can be supplied for limited durations. The OPx62 family is specified over the extended industrial temperature range (–40°C to +125°C). The single OP162 amplifiers are available in 8-lead SOIC, MSOP, and TSSOP packages. The dual OP262 amplifiers are available in 8-lead SOIC and TSSOP packages. The quad OP462 amplifiers are available in 14-lead, narrow-body SOIC and TSSOP packages.

PIN CONFIGURATIONS

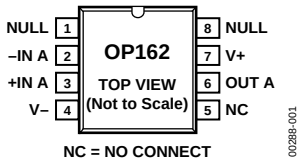

Figure 1. 8-Lead Narrow-Body SOIC (S Suffix)

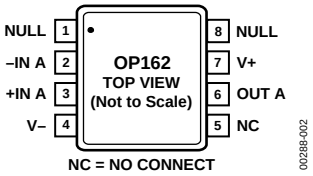

Figure 2. 8-Lead TSSOP (RU Suffix)
8-Lead MSOP (RM Suffix)

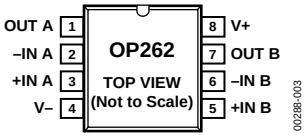

Figure 3. 8-Lead Narrow-Body SOIC (S Suffix)

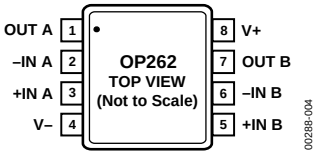

Figure 4. 8-Lead TSSOP (RU Suffix)

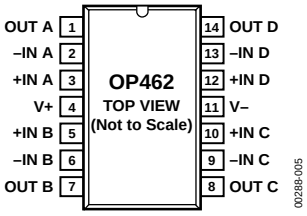

Figure 5. 14-Lead Narrow-Body SOIC (S Suffix)

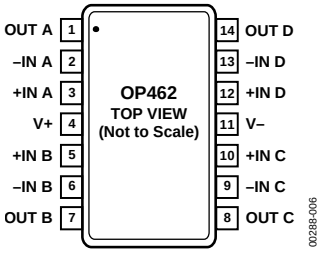

Figure 6. 14-Lead TSSOP (RU Suffix)

Rev. F

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REVISION HISTORY

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12/04—Rev. D to Rev. E

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SPECIFICATIONS

@ V_S = 5.0 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 1. Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	OP162G, OP262G, OP462G		45	325	µV
		−40°C ≤ T_A ≤ +125°C			800	µV
		H grade, −40°C ≤ T_A ≤ +125°C			1	mV
		D grade		0.8	3	mV
		−40°C ≤ T_A ≤ +125°C			5	mV
Input Bias Current	I_B			360	600	nA
		−40°C ≤ T_A ≤ +125°C			650	nA
Input Offset Current	I_{OS}			±2.5	±25	nA
		−40°C ≤ T_A ≤ +125°C			±40	nA
Input Voltage Range	V_{CM}		0		4	V
Common-Mode Rejection	CMRR	0 V ≤ V_{CM} ≤ 4.0 V, −40°C ≤ T_A ≤ +125°C	70	110		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, 0.5 ≤ V_{OUT} ≤ 4.5 V		30		V/mV
		R_L = 10 kΩ, 0.5 ≤ V_{OUT} ≤ 4.5 V	65	88		V/mV
		R_L = 10 kΩ, −40°C ≤ T_A ≤ +125°C	40			V/mV
Long-Term Offset Voltage[1]	V_{OS}	G grade			600	µV
Offset Voltage Drift[2]	$\Delta V_{OS}/\Delta T$			1		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			250		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing High	V_{OH}	I_L = 250 µA, −40°C ≤ T_A ≤ +125°C	4.95	4.99		V
		I_L = 5 mA	4.85	4.94		V
Output Voltage Swing Low	V_{OL}	I_L = 250 µA, −40°C ≤T_A ≤ +125°C		14	50	mV
		I_L = 5 mA		65	150	mV
Short-Circuit Current	I_{SC}	Short to ground		±80		mA
Maximum Output Current	I_{OUT}			±30		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 7 V		120		dB
		−40°C ≤ T_A ≤ +125°C	90			dB
Supply Current/Amplifier	I_{SY}	OP162, V_{OUT} = 2.5 V		600	750	µA
		−40°C ≤ T_A ≤ +125°C			1	mA
		OP262, OP462, V_{OUT} = 2.5 V		500	700	µA
		−40°C ≤ T_A ≤ +125°C			850	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	1 V < V_{OUT} < 4 V, R_L = 10 kΩ		10		V/µs
Settling Time	t_S	To 0.1%, A_V = −1, V_O = 2 V step		540		ns
Gain Bandwidth Product	GBP			15		MHz
Phase Margin	φ_m			61		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.5		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		9.5		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.4		pA/√Hz

[1] Long-term offset voltage is guaranteed by a 1000 hour life test performed on three independent lots at 125°C, with an LTPD of 1.3.
[2] Offset voltage drift is the average of the −40°C to +25°C delta and the +25°C to +125°C delta.

@ V_S = 3.0 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 2. Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	OP162G, OP262G, OP462G		50	325	µV
		G, H grades, –40°C ≤ T_A ≤ +125°C			1	mV
		D grade		0.8	3	mV
		–40°C ≤ T_A ≤ +125°C			5	mV
Input Bias Current	I_B			360	600	nA
Input Offset Current	I_{OS}			±2.5	±25	nA
Input Voltage Range	V_{CM}		0		2	V
Common-Mode Rejection	CMRR	0 V ≤ V_{CM} ≤ 2.0 V, –40°C ≤ T_A ≤ +125°C	70	110		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, 0.5 V ≤ V_{OUT} ≤ 2.5 V		20		V/mV
		R_L = 10 kΩ, 0.5 V ≤ V_{OUT} ≤ 2.5 V	20	30		V/mV
Long-Term Offset Voltage[1]	V_{OS}	G grade			600	µV
OUTPUT CHARACTERISTICS						
Output Voltage Swing High	V_{OH}	I_L = 250 µA	2.95	2.99		V
		I_L= 5 mA	2.85	2.93		V
Output Voltage Swing Low	V_{OL}	I_L = 250 µA		14	50	mV
		I_L= 5 mA		66	150	mV
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 7 V,				
		–40°C ≤ T_A ≤ +125°C	60	110		dB
Supply Current/Amplifier	I_{SY}	OP162, V_{OUT} = 1.5 V		600	700	µA
		–40°C ≤ T_A ≤ +125°C			1	mA
		OP262, OP462, V_{OUT} = 1.5 V		500	650	µA
		–40°C ≤ T_A ≤ +125°C			850	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ		10		V/µs
Settling Time	t_S	To 0.1%, A_V = –1, V_O = 2 V step		575		ns
Gain Bandwidth Product	GBP			15		MHz
Phase Margin	φ_m			59		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.5		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		9.5		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.4		pA/√Hz

[1] Long-term offset voltage is guaranteed by a 1000 hour life test performed on three independent lots at 125°C, with an LTPD of 1.3.

@ V_S = ±5.0 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 3. Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	OP162G, OP262G, OP462G		25	325	µV
		−40°C ≤ T_A ≤ +125°C			800	µV
		H grade, −40°C ≤ T_A ≤ +125°C			1	mV
		D grade		0.8	3	mV
		−40°C ≤ T_A ≤ +125°C			5	mV
Input Bias Current	I_B			260	500	nA
		−40°C ≤ T_A ≤ +125°C			650	nA
Input Offset Current	I_{OS}			±2.5	±25	nA
		−40°C ≤ T_A ≤ +125°C			±40	nA
Input Voltage Range	V_{CM}		−5		+4	V
Common-Mode Rejection	CMRR	−4.9 V ≤ V_{CM} ≤ +4.0 V, −40°C ≤ T_A ≤ +125°C	70	110		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, −4.5 V ≤ V_{OUT} ≤ +4.5 V		35		V/mV
		R_L = 10 kΩ, −4.5 V ≤ V_{OUT} ≤ +4.5 V	75	120		V/mV
		−40°C ≤ T_A ≤ +125°C	25			V/mV
Long-Term Offset Voltage[1]	V_{OS}	G grade			600	µV
Offset Voltage Drift[2]	$\Delta V_{OS}/\Delta T$			1		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			250		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing High	V_{OH}	I_L = 250 µA, −40°C ≤ T_A ≤ +125°C	4.95	4.99		V
		I_L= 5 mA	4.85	4.94		V
Output Voltage Swing Low	V_{OL}	I_L = 250 µA, −40°C ≤ T_A ≤ +125°C		−4.99	−4.95	V
		I_L= 5 mA		−4.94	−4.85	V
Short-Circuit Current	I_{SC}	Short to ground		±80		mA
Maximum Output Current	I_{OUT}			±30		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±1.35 V to ±6 V,				
		−40°C ≤ T_A ≤ +125°C	60	110		dB
Supply Current/Amplifier	I_{SY}	OP162, V_{OUT} = 0 V		650	800	µA
		−40°C ≤ T_A ≤ +125°C			1.15	mA
		OP262, OP462, V_{OUT} = 0 V		550	775	µA
		−40°C ≤ T_A ≤ +125°C			1	mA
Supply Voltage Range	V_S		3.0 (±1.5)		12 (±6)	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	−4 V < V_{OUT} < 4 V, R_L = 10 kΩ		13		V/µs
Settling Time	t_S	To 0.1%, A_V = −1, V_O = 2 V step		475		ns
Gain Bandwidth Product	GBP			15		MHz
Phase Margin	φ_m			64		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.5		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		9.5		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.4		pA/√Hz

[1] Long-term offset voltage is guaranteed by a 1000 hour life test performed on three independent lots at +125°C, with an LTPD of 1.3.
[2] Offset voltage drift is the average of the −40°C to +25°C delta and the +25°C to +125°C delta.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Min
Supply Voltage	±6 V
Input Voltage[1]	±6 V
Differential Input Voltage[2]	±0.6 V

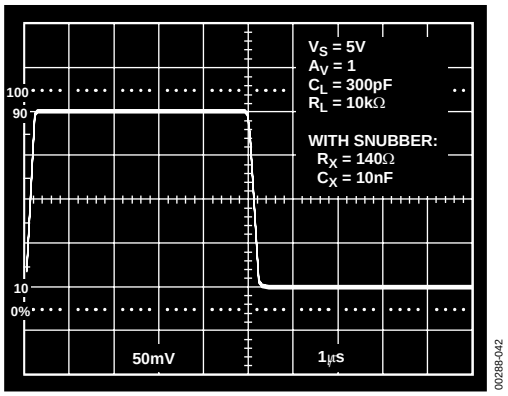


Figure 42. A Photo of a Nice Square Wave at the Output

The network operates in parallel with the load capacitor, C_L, and provides compensation for the added phase lag. The actual values of the network resistor and capacitor are empirically determined to minimize overshoot and maximize unity-gain bandwidth. Table 6 shows a few sample snubber networks for large load capacitors.

Table 6. Snubber Networks for Large Capacitive Loads

C_{LOAD}	R_X	C_X
< 300 pF	140 Ω	10 nF
500 pF	100 Ω	10 nF
1 nF	80 Ω	10 nF
10 nF	10 Ω	47 nF

Higher load capacitance will reduce the unity-gain bandwidth of the device. Figure 43 shows unity-gain bandwidth vs. capacitive load. The snubber network does not provide any increase in bandwidth, but it substantially reduces ringing and overshoot, as shown between Figure 41 and Figure 42.

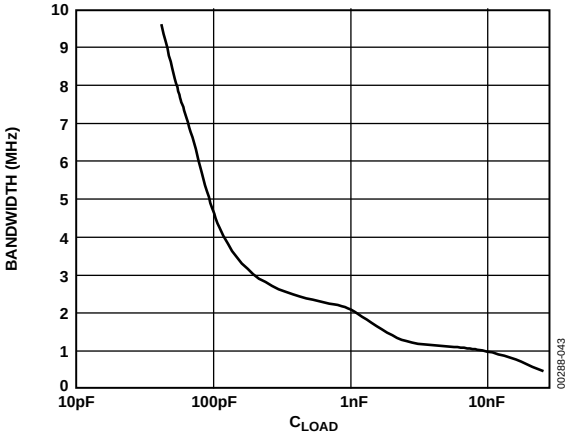


Figure 43. Unity-Gain Bandwidth vs. C_{LOAD}

TOTAL HARMONIC DISTORTION AND CROSSTALK

The OPx62 device family offers low total harmonic distortion making it an excellent choice for audio applications. Figure 44 shows a graph of THD plus noise figures at 0.001% for the OP462.

Figure 45 shows the worst case crosstalk between two amplifiers in the OP462. A 1 V rms signal is applied to one amplifier while measuring the output of an adjacent amplifier. Both amplifiers are configured for unity gain and supplied with ±2.5 V.

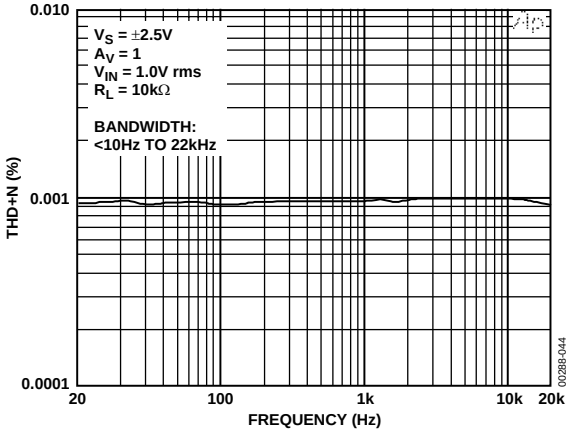


Figure 44. THD + N vs. Frequency

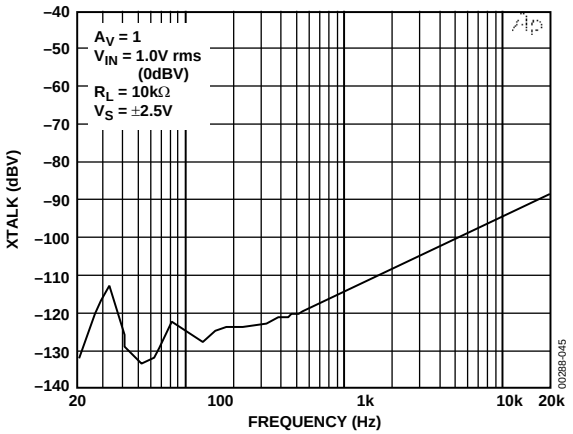


Figure 45. Crosstalk vs. Frequency

PCB LAYOUT CONSIDERATIONS

Because the OP162/OP262/OP462 can provide gains at high frequency, careful attention to board layout and component selection is recommended. As with any high speed application, a good ground plane is essential to achieve the optimum performance. This can significantly reduce the undesirable effects of ground loops and I × R losses by providing a low impedance reference point. Best results are obtained with a multilayer board design with one layer assigned to ground plane.

Use chip capacitors for supply bypassing, with one end of the capacitor connected to the ground plane and the other end connected within 1/8 inch of each power pin. An additional large tantalum electrolytic capacitor (4.7 µF to 10 µF) should be connected in parallel. This capacitor provides current for fast, large-signal changes at the device's output; therefore, it does not need to be placed as close to the supply pins.

APPLICATION CIRCUITS

SINGLE-SUPPLY STEREO HEADPHONE DRIVER

Figure 46 shows a stereo headphone output amplifier that can operate from a single 5 V supply. The reference voltage is derived by dividing the supply voltage down with two 100 kΩ resistors. A 10 µF capacitor prevents power supply noise from contaminating the audio signal and establishes an ac ground for the volume control potentiometers.

The audio signal is ac-coupled to each noninverting input through a 10 µF capacitor. The gain of the amplifier is controlled by the feedback resistors and is (R2/R1) + 1. For this example, the gain is 6. By removing R1, the amplifier would have unity gain. To short-circuit protect the output of the device, a 169 Ω resistor is placed at the output in the feedback network. This prevents any damage to the device if the headphone output becomes shorted. A 270 µF capacitor is used at the output to couple the amplifier to the headphone. This value is much larger than that used for the input because of the low impedance of headphones, which can range from 32 Ω to 600 Ω or more.

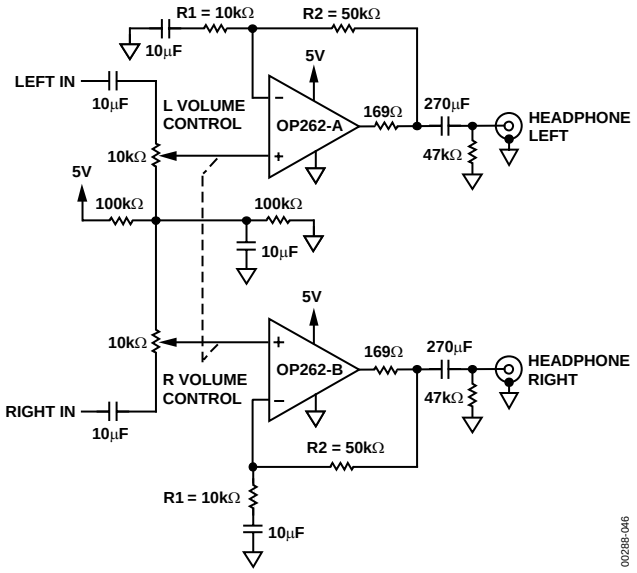


Figure 46. Headphone Output Amplifier

INSTRUMENTATION AMPLIFIER

Because of their high speed, low offset voltages, and low noise characteristics, the OP162/OP262/OP462 can be used in a wide variety of high speed applications, including precision instrumentation amplifiers. Figure 47 shows an example of such an application.

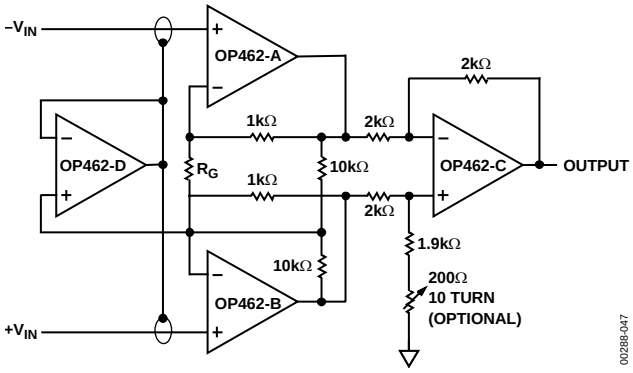


Figure 47. High Speed Instrumentation Amplifier

The differential gain of the circuit is determined by R_G, where

$$A_{DIFF} = 1 + \frac{2}{R_G}$$

with the R_G resistor value in kΩ. Removing R_G sets the circuit gain to unity.

The fourth op amp, OP462-D, is optional and is used to improve CMRR by reducing any input capacitance to the amplifier. By shielding the input signal leads and driving the shield with the common-mode voltage, input capacitance is eliminated at common-mode voltages. This voltage is derived from the midpoint of the outputs of OP462-A and OP462-B by using two 10 kΩ resistors followed by OP462-D as a unity-gain buffer.

It is important to use 1% or better tolerance components for the 2 kΩ resistors, as the common-mode rejection is dependent on their ratios being exact. A potentiometer should also be connected in series with the OP462-C noninverting input resistor to ground to optimize common-mode rejection.

The circuit in Figure 47 was implemented to test its settling time. The instrumentation amp was powered with −5 V, so the input step voltage went from −5 V to +4 V to keep the OP462 within its input range. Therefore, the 0.05% settling range is when the output is within 4.5 mV. Figure 48 shows the positive slope settling time to be 1.8 µs, and Figure 49 shows a settling time of 3.9 µs for the negative slope.

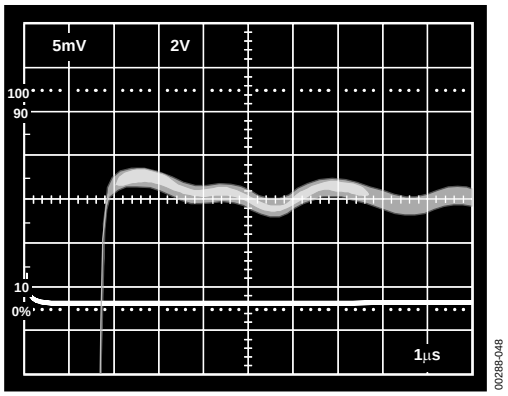


Figure 48. Positive Slope Settling Time

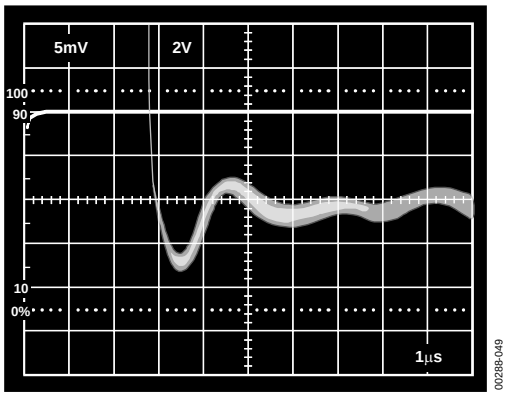


Figure 49. Negative Slope Settling Time

DIRECT ACCESS ARRANGEMENT

Figure 50 shows a schematic for a 5 V single-supply transmit/receive telephone line interface for 600 Ω transmission systems. It allows full-duplex transmission of signals on a transformer-coupled 600 Ω line. Amplifier A1 provides gain that can be adjusted to meet the modem output drive requirements. Both A1 and A2 are configured to apply the largest possible differential signal to the transformer. The largest signal available on a single 5 V supply is approximately 4.0 V p-p into a 600 Ω transmission system. Amplifier A3 is configured as a difference amplifier to extract the receive information from the transmission line for amplification by A4. A3 also prevents the transmit signal from interfering with the receive signal. The gain of A4 can be adjusted in the same manner as A1 to meet the modem's input signal requirements. Standard resistor values permit the use of SIP (single in-line package) format resistor arrays. Couple this with the OP462 14-lead SOIC or TSSOP package and this circuit offers a compact solution.

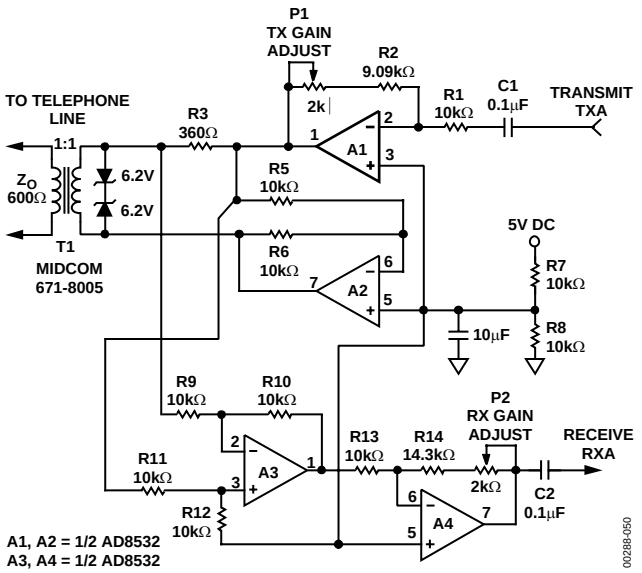
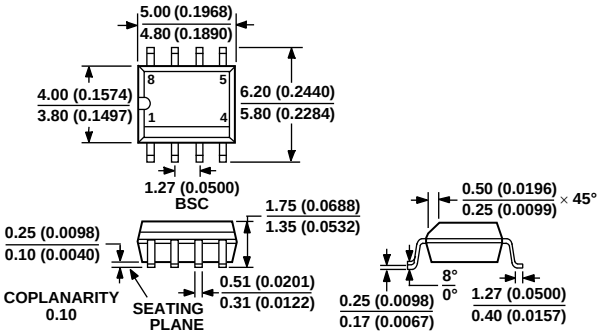


Figure 50. Single-Supply Direct Access Arrangement for Modems

SPICE MACRO-MODEL

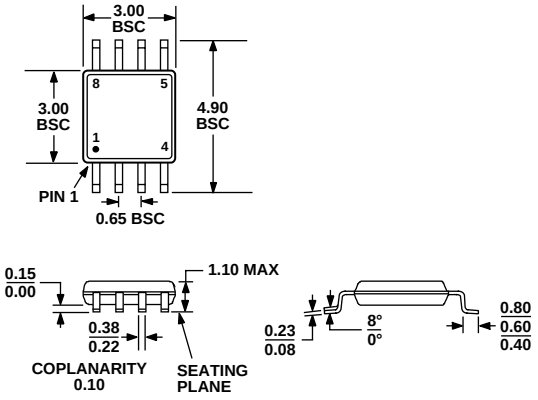
```
* OP162/OP262/OP462 SPICE Macro-model
* 7/96, Ver. 1
* Troy Murphy / ADSC
*
* Copyright 1996 by Analog Devices
*
* Refer to "README.DOC" file for License Statement. Use of this model
* indicates your acceptance of the terms and provisions in the License
* Statement
*
* Node Assignments
*               noninverting input
*               |       inverting input
*               |       |       positive supply
*               |       |       |       negative supply
*               |       |       |       |       output
*               |       |       |       |       |
*               |       |       |       |       |
.SUBCKT OP162 1       2       99      50      45
*
*INPUT STAGE
*
Q1  5  7  3  PIX 5
Q2  6  2  4  PIX 5
Ios 1  2  1.25E-9
I1  99 15 85E-6
EOS 7  1  POLY(1) (14, 20) 45E-6 1
RC1 5  50 3.035E+3
RC2 6  50 3.035E+3
RE1 3  15 607
RE2 4  15 607
C1  5  6  600E-15
D1  3  8  DX
D2  4  9  DX
V1  99 8  DC 1
V2  99 9  DC 1
*
* 1st GAIN STAGE
*
EREF 98 0  (20, 0) 1
G1   98 10 (5, 6)  10.5
R1   10 98 1
C2   10 98 3.3E-9
*
* COMMON-MODE STAGE WITH ZERO AT 4kHz
*
ECM 13 98 POLY (2) (1, 98) (2, 98) 0 0.5 0.5
R2  13 14 1E+6
R3  14 98 70
C3  13 14 80E-12
*
* POLE AT 1.5MHz, ZERO AT 3MHz
*
G2 21 98 (10, 98) .588E-6
R4 21 98 1.7E6
R5 21 22 1.7E6
C4 22 98 31.21E-15
*
* POLE AT 6MHz, ZERO AT 3MHz
*
E1 23 98 (21, 98) 2
R6 23 24 53E+3
R7 24 98 53E+3
C5 23 24 1E-12
*
* SECOND GAIN STAGE
*
G3 25 98 (24, 98) 40E-6
R8 25 98 1.65E+6
D3 25 99 DX
D4 50 25 DX
*
* OUTPUT STAGE
*
GSY 99 50 POLY (1) (99, 50) 277.5E-6 7.5E-6
R9  99 20 100E3
R10 20 50 100E3
Q3  45 41 99 POUT 4
Q4  45 43 50 NOUT 2
EB1 99 40 POLY (1) (98, 25) 0.70366 1
EB2 42 50 POLY (1) (25, 98) 0.73419 1
RB1 40 41 500
RB2 42 43 500
CF  45 25 11E-12
D5  46 99 DX
D6  47 43 DX
V3  46 41 0.7
V4  47 50 0.7
.
MODEL  PIX  PNP (Bf=117.7)
.MODEL POUT PNP (BF=119, IS=2.782E-17, VAF=28, KF=3E-7)
.MODEL NOUT NPN (BF=110, IS=1.786E-17, VAF=90, KF=3E-7)
.MODEL DX   D()
.ENDS
```

OUTLINE DIMENSIONS



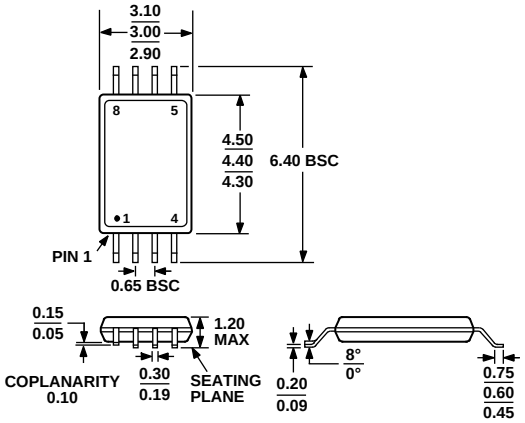
COMPLIANT TO JEDEC STANDARDS MS-012AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 51. 8-Lead Standard Small Outline Package [SOIC] Narrow Body S-Suffix (R-8)
Dimensions shown in millimeters and (inches)



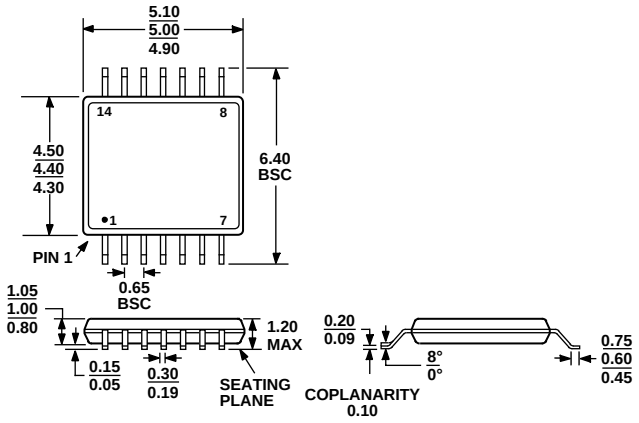
COMPLIANT TO JEDEC STANDARDS MO-187AA

Figure 52. 8-Lead Mini Small Outline Package [MSOP] (RM-8)
Dimensions shown in millimeters



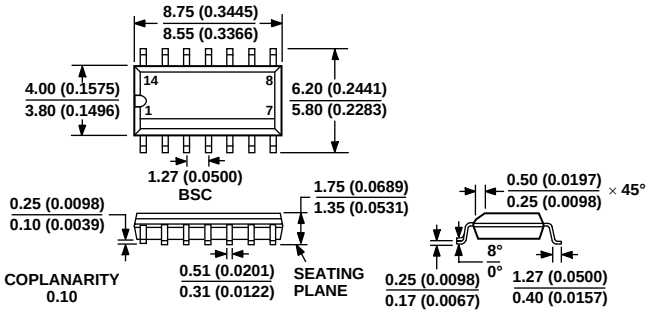
COMPLIANT TO JEDEC STANDARDS MO-153AA

Figure 53. 8-Lead Thin Shrink Small Outline Package [TSSOP] (RU-8)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153AB-1

Figure 54. 14-Lead Thin Shrink Small Outline Package [TSSOP] (RU-14)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012AB
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 55. 14-Lead Standard Small Outline Package [SOIC] Narrow Body S-Suffix (R-14)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
OP162GS	−40°C to +125°C	8-Lead SOIC	S-Suffix (R-8)	
OP162GS-REEL	−40°C to +125°C	8-Lead SOIC	S-Suffix (R-8)	
OP162GS-REEL7	−40°C to +125°C	8-Lead SOIC	S-Suffix (R-8)	
OP162GSZ[1]	−40°C to +125°C	8-Lead SOIC	S-Suffix (R-8)	
OP162GSZ-REEL[1]	−40°C to +125°C	8-Lead SOIC	S-Suffix (R-8)	
OP162GSZ-REEL7[1]	−40°C to +125°C	8-Lead SOIC	S-Suffix (R-8)	
OP162DRU-REEL	−40°C to +125°C	8-Lead TSSOP	RU-8	
OP162DRUZ-REEL[1]	−40°C to +125°C	8-Lead TSSOP	RU-8	
OP162HRU-REEL	−40°C to +125°C	8-Lead TSSOP	RU-8	
OP162HRUZ-REEL[1]	−40°C to +125°C	8-Lead TSSOP	RU-8	
OP162DRM-REEL	−40°C to +125°C	8-Lead MSOP	RM-8	AND
OP162DRMZ-REEL[1]	−40°C to +125°C	8-Lead MSOP	RM-8	AOJ
OP262DRU-REEL	−40°C to +125°C	8-Lead TSSOP	RU-8	
OP262DRUZ-REEL[1]	−40°C to +125°C	8-Lead TSSOP	RU-8	
OP262GS	−40°C to +125°C	8-Lead SOIC	S-Suffix (R-8)	
OP262GS-REEL	−40°C to +125°C	8-Lead SOIC	S-Suffix (R-8)	
OP262GS-REEL7	−40°C to +125°C	8-Lead SOIC	S-Suffix (R-8)	
OP262GSZ[1]	−40°C to +125°C	8-Lead SOIC	S-Suffix (R-8)	
OP262GSZ-REEL[1]	−40°C to +125°C	8-Lead SOIC	S-Suffix (R-8)	
OP262GSZ-REEL7[1]	−40°C to +125°C	8-Lead SOIC	S-Suffix (R-8)	
OP262HRU-REEL	−40°C to +125°C	8-Lead TSSOP	RU-8	
OP262HRUZ-REEL[1]	−40°C to +125°C	8-Lead TSSOP	RU-8	
OP462DRU-REEL	−40°C to +125°C	14-Lead TSSOP	RU-14	
OP462DRUZ-REEL[1]	−40°C to +125°C	14-Lead TSSOP	RU-14	
OP462DS	−40°C to +125°C	14-Lead SOIC	S-Suffix (R-14)	
OP462DS-REEL	−40°C to +125°C	14-Lead SOIC	S-Suffix (R-14)	
OP462DS-REEL7	−40°C to +125°C	14-Lead SOIC	S-Suffix (R-14)	
OP462DSZ[1]	−40°C to +125°C	14-Lead SOIC	S-Suffix (R-14)	
OP462DSZ-REEL[1]	−40°C to +125°C	14-Lead SOIC	S-Suffix (R-14)	
OP462DSZ-REEL7[1]	−40°C to +125°C	14-Lead SOIC	S-Suffix (R-14)	
OP462GS	−40°C to +125°C	14-Lead SOIC	S-Suffix (R-14)	
OP462GS-REEL	−40°C to +125°C	14-Lead SOIC	S-Suffix (R-14)	
OP462GS-REEL7	−40°C to +125°C	14-Lead SOIC	S-Suffix (R-14)	
OP462GSZ[1]	−40°C to +125°C	14-Lead SOIC	S-Suffix (R-14)	
OP462GSZ-REEL[1]	−40°C to +125°C	14-Lead SOIC	S-Suffix (R-14)	
OP462GSZ-REEL7[1]	−40°C to +125°C	14-Lead SOIC	S-Suffix (R-14)	
OP462HRU-REEL	−40°C to +125°C	14-Lead TSSOP	RU-14	
OP462HRUZ-REEL[1]	−40°C to +125°C	14-Lead TSSOP	RU-14	

[1] Z = Pb-free part.

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