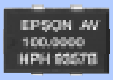
## CRYSTAL OSCILLATOR
### HIGH-STABILITY

# HG - 8002JA series

- Frequency range : 1 MHz to 125 MHz
- Supply voltage : 3.3 V or 5.0 V
- Frequency tolerance : ±20×10$^{-6}$ / -20 °C to +70 °C
- Function : Output enable(OE) or Standby( $\overline{ST}$ )
- Thickness : 4.7 mm Max.
  Package and pin compatible with SG-615.

Actual size

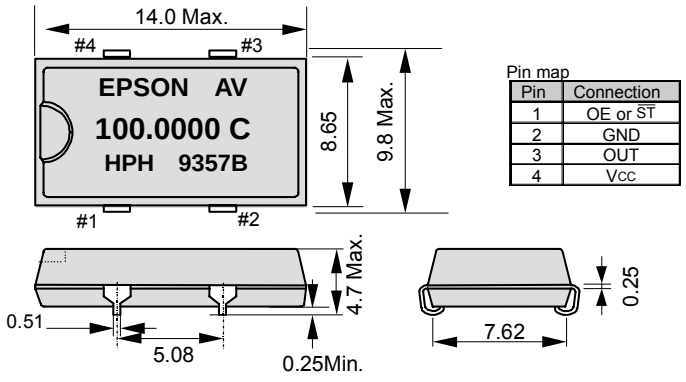


## Specifications (characteristics)

| Item | | Symbol | Specifications | | | Remarks |
|---|---|---|---|---|---|---|
| | | | PT / ST | PH / SH | PC / SC | |
| Output frequency range | | $f_0$ | 1.000 MHz to 125.000 MHz | | | |
| Supply voltage | | $V_{CC}$ | 5.0 V±0.25 V | | 3.3 V±0.165 V | |
| Temperature range | Storage temperature | T_stg | -55 °C to +125 °C | | | Store as bare product after unpacking |
| | Operating temperature | T_use | -20 °C to +70 °C<br>(-40 °C to +85 °C) | | -40 °C to +85 °C | |
| Frequency tolerance | | F_tol(osc) | AV: ±20 × 10$^{-6}$ ,BV: ±25 × 10$^{-6}$ | | | -20 °C to +70 °C |
| | | | CX: ±30 × 10$^{-6}$ | | | -40 °C to +85 °C *1 |
| Current consumption | | $I_{CC}$ | 45 mA Max. | | 28 mA Max. | No load condition, Max. frequency |
| Output disable current | | I_dis | 30 mA Max. | | 16 mA Max. | OE=GND (PT,PH,PC) |
| Stand-by current | | I_std | 50 µA Max. | | | $\overline{ST}$ =GND (ST,SH,SC) |
| Symmetry | | SYM | — | 40 % to 60 % | | CMOS load:50%$V_{CC}$ level, Max. load condition |
| | | | 40 % to 60 % | — | | TTL load: 1.4V level, Max. load condition |
| High output voltage | | $V_{OH}$ | $V_{CC}$-0.4 V Min. | | | $I_{OH}$=-16 mA(PT,ST,PH,SH),-8 mA(PC,SC) |
| Low output voltage | | $V_{OL}$ | 0.4 V Max. | | | $I_{OL}$= 16 mA(PT,ST,PH,SH), 8 mA(PC,SC) |
| Output load condition (TTL) | | L_TTL | 2 TTL Max. | — | | Max. frequency |
| Output load condition (CMOS) | | L_CMOS | 15 pF Max. | | | Max. supply voltage |
| Output enable / disable input voltage | | $V_{IH}$ | 2.0 V Min. | | 70 % $V_{CC}$ Min. | $\overline{ST}$ , OE terminal |
| | | $V_{IL}$ | 0.8 V Max. | | 20 % $V_{CC}$ Max. | $\overline{ST}$ , OE terminal |
| Output rise and fall time | | $t_r$ / $t_f$ | — | 3 ns Max. | | CMOS load: 20 % $V_{CC}$ to 80 % $V_{CC}$ level |
| | | | 4 ns Max. | — | | TTL load: 0.4 V to 2.4 V level |
| Oscillation start up time | | $t_{OSC}$ | 10 ms Max. | | | Time at minimum supply voltage to be 0 s |
| Frequency aging | | F_aging | ±2 × 10$^{-6}$ / year Max. | | | +25 °C, $V_{CC}$=5.0 V/ 3.3 V (PC / SC) |

PLL-PLL connection & Jitter specification, please refer to Page 40.
*1 PT, ST and PH , SH for “CX” tolerance will be available up to 55 MHz.

## External dimensions (Unit:mm)




Pin map

| Pin | Connection |
|---|---|
| 1 | OE or $\overline{ST}$ |
| 2 | GND |
| 3 | OUT |
| 4 | $V_{CC}$ |

Note.
OE Pin (PT, PH, PC)
OE pin = "H" or "open" : Specified frequency output.
OE pin = "L" : Output is high impedance.

$\overline{ST}$ pin (ST, SH, SC)
$\overline{ST}$ pin - "H" or "open" : Specified frequency output.
$\overline{ST}$ pin - "L" : Output is low level (weak pull - down), oscillation stops.

## Footprint (Recommended) (Unit:mm)