SIEMENS

ICs for Communications

Octal Transceiver for DASL Compatible Interfaces OCTAT-P

PEB 2096 Version 2.1

Addendum 05.98 to the Data Sheet 01.96

PEB 2096 **Revision History:**		**Current Version: 05.98**
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1 Overview

The Octal Transceiver for DASL compatible interfaces, OCTAT-P, PEB 2096, implements the two-wire DASL compatible interface used to link voice/data digital terminals to PBX subscriber lines. The OCTAT-P is an optimized device for LT applications and can handle up to eight DASL compatible interfaces simultaneously.

The OCTAT-P is a CMOS device offered in a P-MQFP-44 package.

2 Functional Description

The PEB 2096, OCTAT-P, performs the layer-1 functions of the ISDN basic access for eight DASL compatible interfaces at the LT side of the PBX.

2.1 Device Architecture

The OCTAT-P contains the following functional blocks:

- Eight line transceivers for the DASL compatible interfaces
- One IOM-2 interface
- Frame structure converter between the IOM-2 interface and the DASL compatible interfaces
- JTAG Boundary scan interface
- Clocking, reset and initialization block

2.2 Interfaces

2.2.1 General Principle of the DASL Compatible Interface

A frame transmitted by the exchange (LT) is received by the terminal equipment (TE) after a given propagation delay (t_d). Refer to **figure 1**. The terminal equipment waits a guard time of six bits (t_g = 15.6 µs) while the line clears. It then transmits a frame to the exchange. The exchange begins a transmission every 250 µs (known as the burst repetition period). However, the time between the reception of a frame from the TE and the beginning of transmission of the next frame by the LT must be greater than the minimum guard time. Communication between an LT and a PT (Private Termination) follows exactly the same procedure.

Note that the guard time in TE is always defined with respect to the last D-bit.

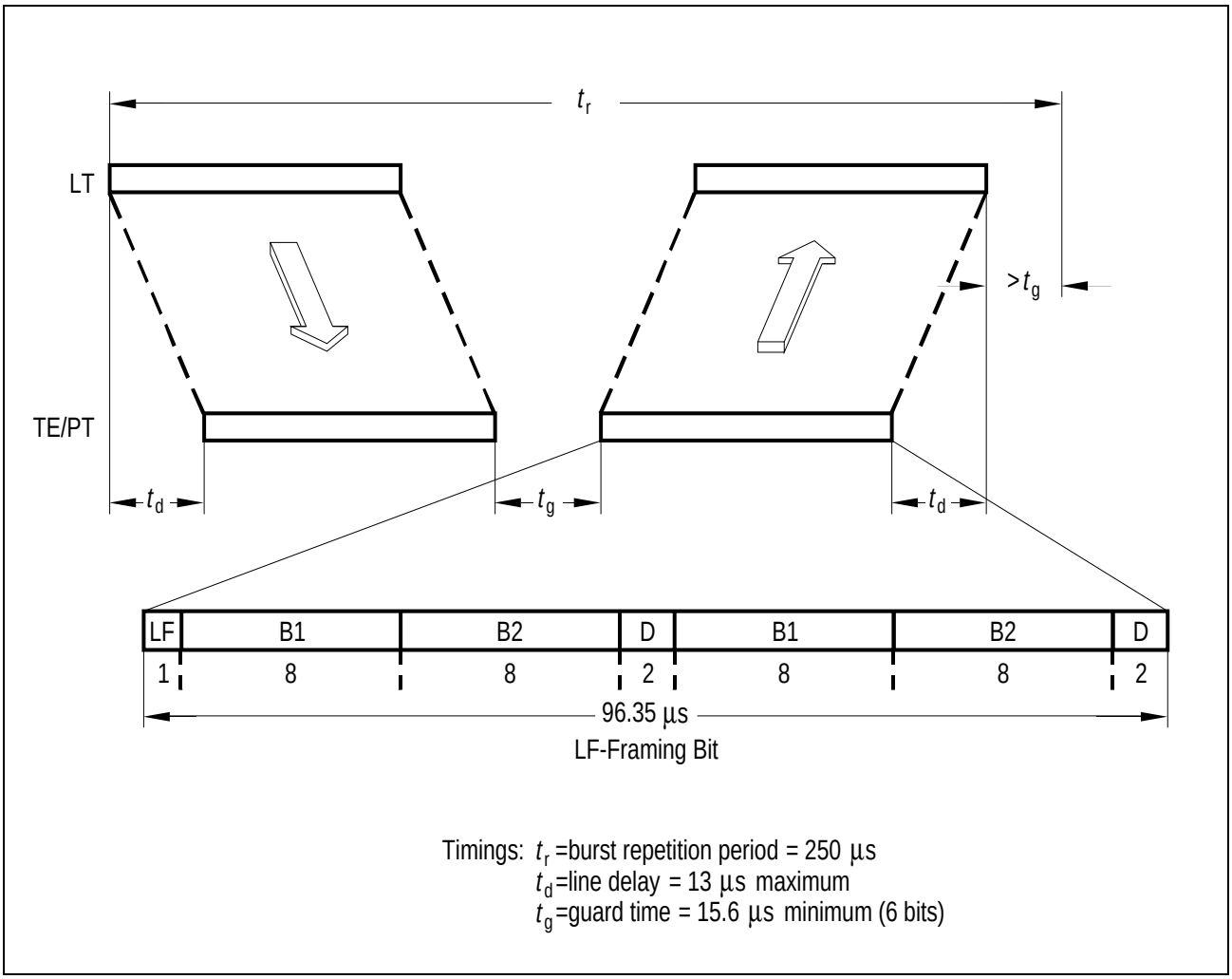

Figure 1
DASL Compatible Interface Frame Structure

Within a burst, the data rate is 384 kbit/s. The 37-bit frame structure is as shown in **figure 1**. The framing bit (LF) is always logical ‘1’. The frame also contains the user channels (2B + D).

It can readily be seen that in the 250 µs burst repetition period, 4 D bits, 16 B1 bits and 16 B2 bits are transferred in each direction. This results in an effective full duplex data rate of 16 kbit/s for the D channel and 64 kbit/s for each B channel.

The OCTAT-P scrambles B- and D-channel data on the DASL compatible interface in order to ensure that the downstream receiver gets enough pulses for a reliable clock extraction (flat continuous power density spectrum is provided) and no periodic patterns appear on the line.

The scrambling polynomial is: $x^9 + x^5 + 1$.

The coding technique used on the U interface is a AMI code. A logical ‘0’ corresponds to a neutral level, logical ‘1’ are coded as alternate positive and negative pulses.

See **figure 2**. The AMI coding includes always the data bits going on the DASL compatible interface in one direction. Thus there is a separate AMI coding unit for data downstream and one for data upstream.

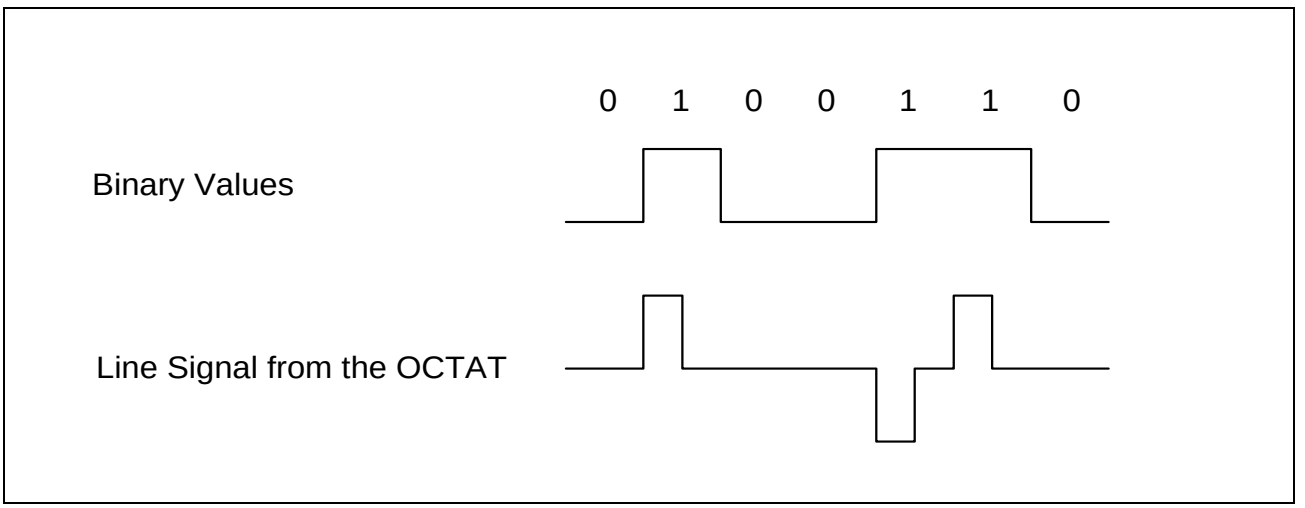

Figure 2
AMI Coding on the DASL compatible Interface

2.2.2 IOM-2 System Interface

Unchanged

2.2.3 JTAG Boundary Scan Test Interface

IDCODE

The 32-bit identification register is serially read out via TDO. It contains the version number (4 bits), the device code (16 bits) and the manufacture code (11 bits). The LSB is fixed to “1”.

Version	Device Code	Manufacture Code		Output
0XXX	0000 0000 0001 0100	0000 1000 001	1	--> TDO
0010	Version 1.3			
0011	Version 2.1			

Note: In the state “test logic reset” the code “0011” is loaded into the instruction code register.

2.3 Individual Functions

2.3.1 Transceiver, Analog Connections

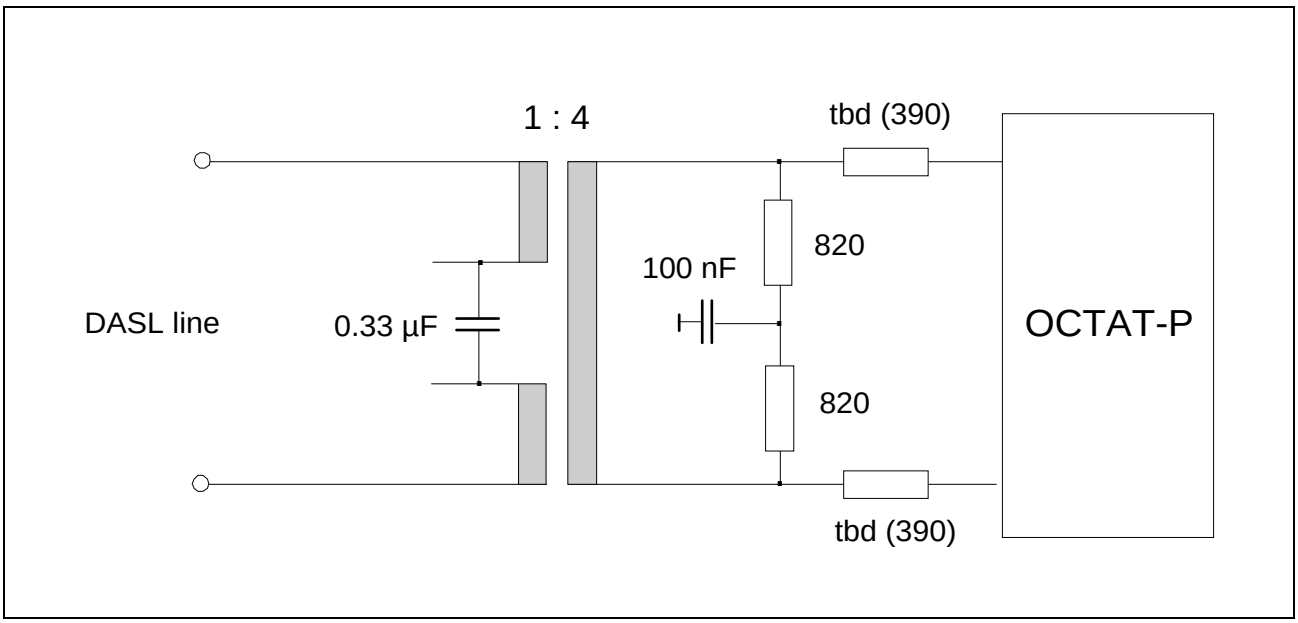

Figure 3
External Circuitry for DASL Compatible Interface

The PEB 2096, OCTAT-P, covers the electrical requirements of the DASL compatible interface for loop lengths depending on the used transformer and the cable quality:

Transformer	Cable	Loop Length
4:1	AWG 24	5.5 kfeet

*Note: The actual values of the external resistors depend on the selected transformer. The resistor values in **figures 3** are tbd.*

2.3.2 Diagnostic Functions

Loop 2 is no longer supported.

3 Operational Description

3.1 General

All procedures required for data transmission over the DASL compatible interface are implemented. These comprise the DASL compatible interface frame synchronization, activation/deactivation procedure, and timing requirements such as bit rate and jitter.

3.2 Clocking, Reset and Initialization

Unchanged

3.3 Push – Pull Sensing on Pin DU

Unchanged

3.4 Transmit Delay on DASL Compatible Interface with respect to IOM®-2 Interface

The OCTAT-P causes delays of B- and on D-channels with respect to the IOM channel number. **Figure 4** shows this delay at a data rate of 2.048 Mbit/s.

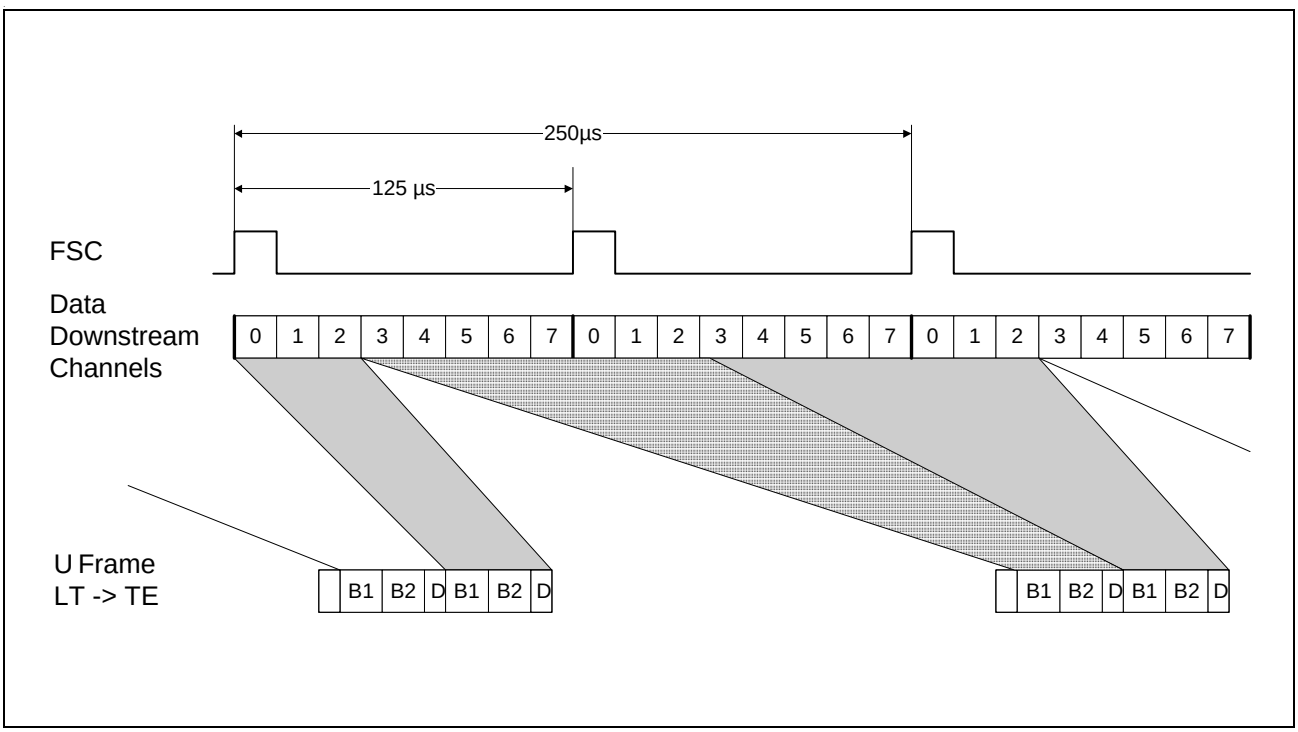

Figure 4
Transmit Delay of B- and D-Channels

3.5 DASL Compatible Frame Synchronization

There are two possibilities how to synchronize the DASL compatible frame to the IOM-2 frame: With a short FSC or with $\overline{\text{SSYNC}}$.

3.5.1 Synchronization with a Short FSC

The short FSC pulse has a width of one DCL clock (in normal use the FSC is at least 2 DCL wide). The $\overline{\text{SSYNC}}$ input must be set to 1. The period of the short FSC pulses must be a multiple of 250 µs. The DASL compatible transmit frame starts in the IOM channel 0 which follows the short FSC pulse. Refer to **figure 5**.

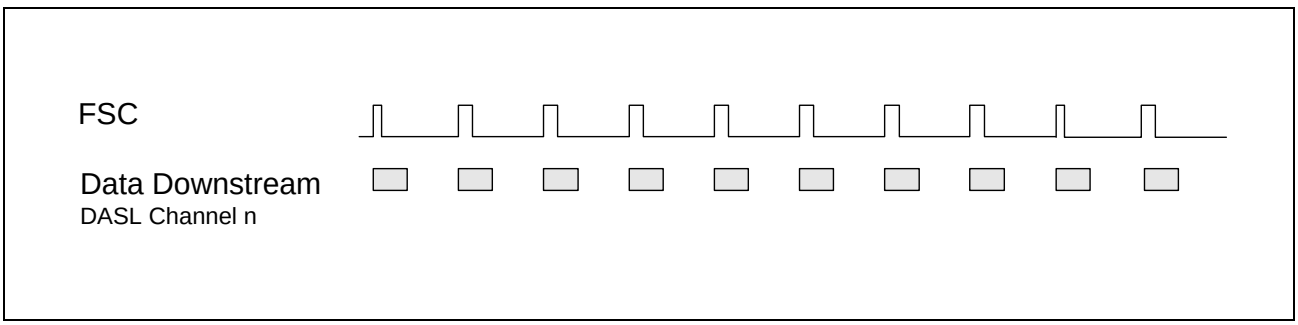

Figure 5
Synchronization with a short FSC

3.5.2 Synchronization using $\overline{\text{SSYNC}}$ (for DECT)

A zero pulse on the $\overline{\text{SSYNC}}$ input forces the OCTAT-P to start a frame at the beginning of this IOM frame. Refer to **figure 6**.

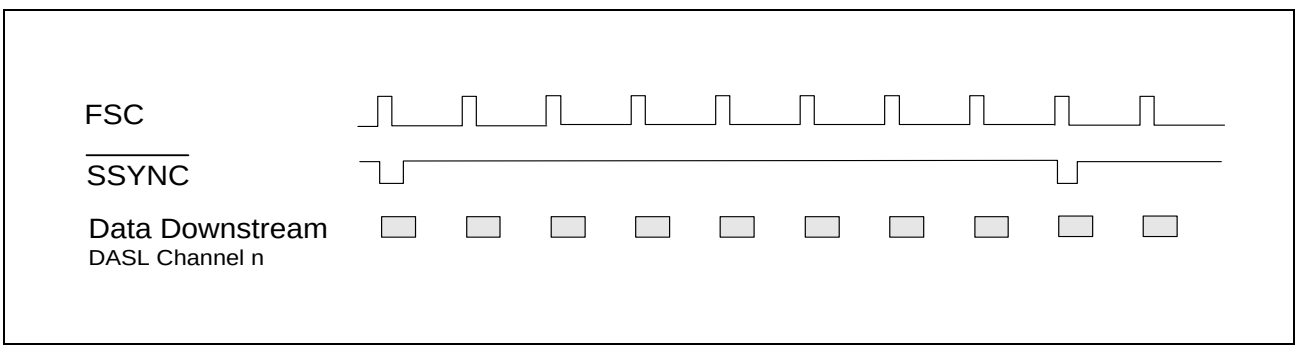

Figure 6
Synchronization with $\overline{\text{SSYNC}}$

While using $\overline{\text{SSYNC}}$ for DASL compatible frame synchronization the short FSC signal is not allowed. If not used, the $\overline{\text{SSYNC}}$ input must be connected to V_{DD}.

3.6 D-Channel Handling

The arbiter function of the line card D-channel handler is not supportet.

3.7 IOM®-2 Interface Monitor Channel

Unchanged

3.8 Command / Indicate Channel

The C/I channel is used for communication between the OCTAT-P and a layer-2 device (or ELIC), to control and monitor layer-1 functions. The layer-2 device monitors the layer-1 indication continuously and indicates a change if a new code is found to be valid in two consecutive IOM frames (double last look criterion).

Table 1
Commands

Command (downstream)	Abbr.	Code	Remarks
Deactivate request	DR	0000	
Reset	RES	0001	
Test mode 2	TM2	0010	Transmission of pseudo-ternary pulses at 2 kHz frequency
Test mode 1	TM1	0011	Transmission of pseudo-ternary pulses at 192 kHz frequency
Activate request	AR	1000 1100 1010	Transmission of INFO 2 or INFO 4.
Activate request local test loop	ARL	1001	Transmission of INFO 2, switching of loop 1 (on DASL compatible interface)
Deactivate confirmation	DC	1111	Deactivation acknowledgment, quiescent state

Table 2
Indications

Indication (upstream)	Abbr.	Code	Remarks
Timing required (to activate IOM-2)	TIM	0000	Deactivated state, activation from the line not possible
Resynchronization (loss of framing)	RSY	0100	Receiver is not synchronous
Activate request	AR	1000	Info 1w received
U only activation indication	UAI	0111	Info 1 received synchronous receiver
Activate indication	AI	1100	Layer-1 fully activated
Deactivate indication	DI	1111	Info 0 or DC received after deactivation request

3.9 Activation and Deactivation, State Machine

3.9.1 States Description

OCTAT-P state machine enters two different kind of states:

Unconditional and conditional states, **figure 7.**

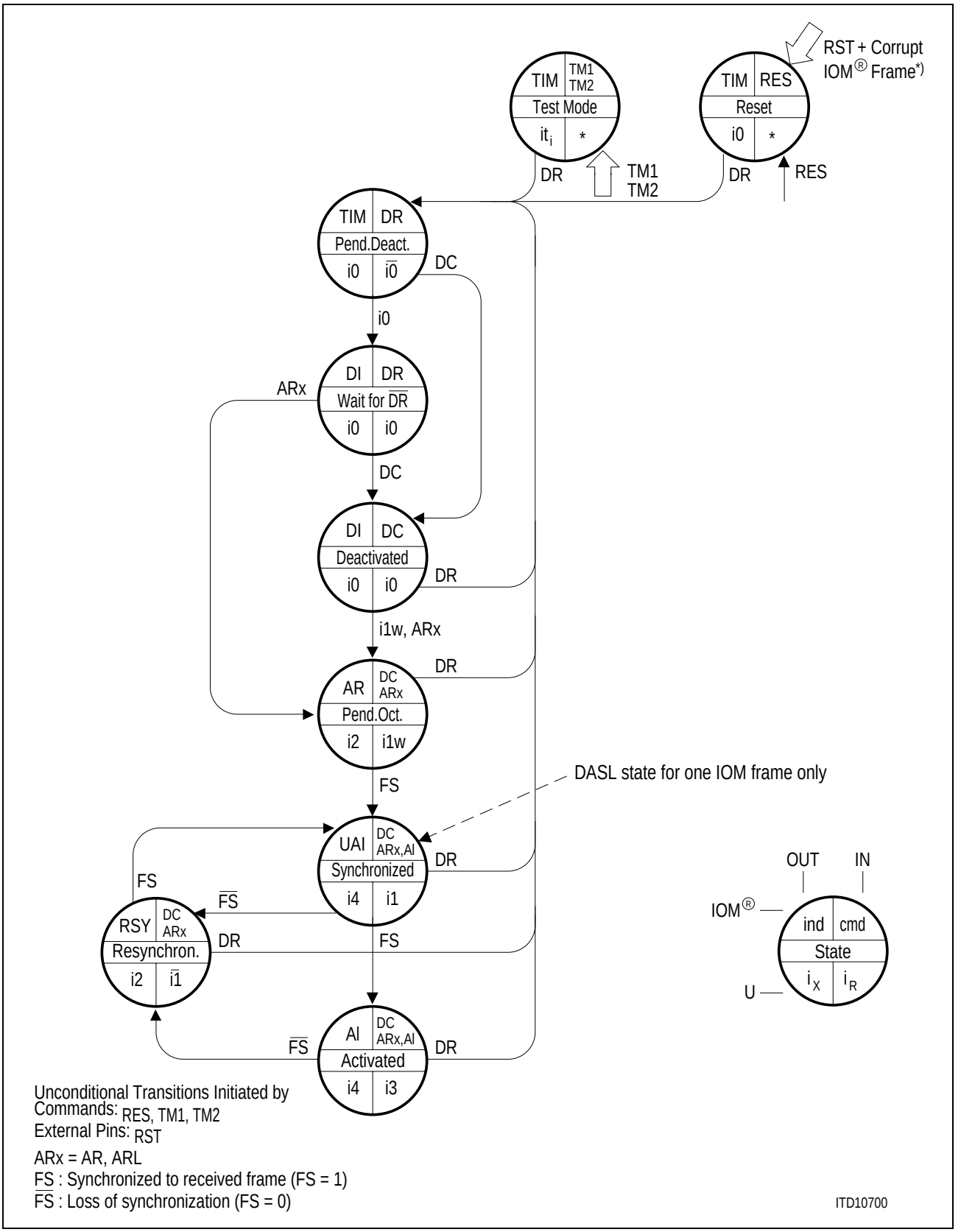

Figure 7
OCTAT-P State Diagram

Conditional States

Deactivated

This is the power down state of the physical protocol. The awake detection is active and the device will respond to any signal on the line (wake signal) by initiating activation.

Pending Activation

This state results from a request for activation of the line, either from the terminal (INFO 1w) or from the layer-2 device (AR or ARL). Info 2 is then transmitted and the OCTAT-P waits for the responding INFO 1 from the remote device.

Synchronized

Upon receipt of INFO 1 the OCTAT-P must synchronize itself to the signal (FS = 1). Synchronization is achieved after the detection of at least 4 consecutive valid frames. This process takes at most 10 ms

Note: This state is a "drop through" state and appears for one IOM frame before entering the state "Activated".

Activated

The line is activated; the OCTAT-P sends INFO 4 to the remote, the remote sends INFO 3 to the OCTAT-P.

Resynchronization

If the OCTAT-P looses synchronization (FS = 0), for whatever reason, it will attempt to resynchronize. Synchronization is lost after the detection of at least 4 consecutive invalid frames. Entering this state it will output INFO 2. This is similar to the original synchronization procedure in the pending activation state (the indication given to layer 2 is different). However as before, recognition of a valid frame (FS = 1) leads to the synchronized state.

Refer to OCTAT-P state diagram in **figure 7**.

3.9.2 Info Structure on the DASL Compatible Interface

Signals controlling and indicating the internal state of all DASL compatible transceiver state machines are called INFOs. Four different INFOs (INFO 0, 1W, 1/2 and 3/4) can be sent over the interface depending on the actual state (Synchronized, Activated, Pending Activation, Test Mode, Deactivated, Reset,...) of the connected transceivers. When the line is deactivated INFO 0 is exchanged by the transceivers at either end of the line. Info 0 indicates that there is no signal on the line; in either direction.

When the line is activated INFO 3 (in upstream direction) and INFO 4 (in downstream direction) are continually sent. Info 3 and 4 contain the transmitted data (B1, B2, D).

Info 1w and 1/2 are used for initialization. The form of each INFO is shown in the following table:

Name	Direction	Description
Info 0	Upstream Downstream	No signal on the line
Info 1W	Upstream	Asynchronous wake signal 2 kHz burst rate F=1, B and D channels contain scrambled ”1”
Info 1	Upstream	4 kHz burst rate F=1, B and D channels contain scrambled ”1”
Info 2	Downstream	4 kHz burst rate F=1, B and D channels contain scrambled ”1”
Info 3	Upstream	4 kHz burst rate F=1, B and D channels contain scrambled data
Info 4	Downstream	4 kHz burst rate F=1, B and D channels contain scrambled data

Note: F = Framing bit

3.9.3 Example of Activation and Deactivation

The activation and deactivation procedure between an OCTAT-P and a DASL compatible terminal device is shown in **figure 8**. It illustrates how the state machines of the respective modes interwork to facilitate activation and deactivation. In this case activation was initiated by an AR request at the terminal side and deactivation by a DR command at the LT side. Activation could also be initialized at the LT side using an AR request.

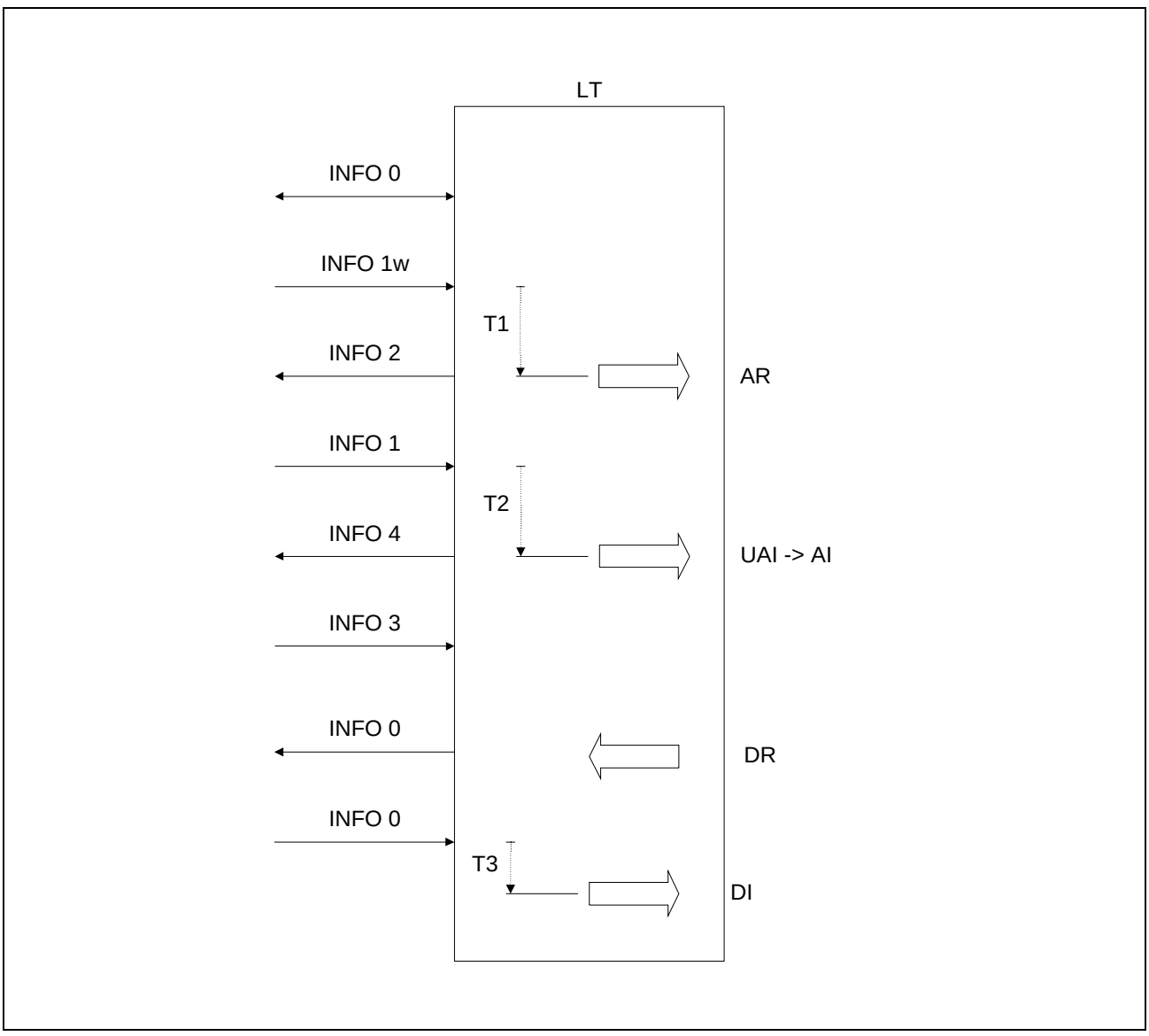

Figure 8
Example for OCTAT-P Activation and Deactivation

Note: T1: < 250 µs time for error free level detection
T2: < 10 ms time for synchronization
T3: 2 ms time for error free detection of INFO 0

4 Registers Description

4.1 Identification Register – (Read)

Unchanged

4.2 General Configuration Register – (Write)

Unchanged

4.3 Bit Error Register – (Read)

Address: 1_H

Format:

bit 7							bit 0
BEO7	BEO6	BEO5	BEO4	BEO3	BEO2	BEO1	BEO0

Initial Value: 00_H

Description: **BEOn** = 1: Bit error occurred on DASL compatible interface in ch. n
Code violation detected.
The Bit Error Register is reset after reading the register

4.4 Configuration Register for DASL compatible Line Interfaces – (Write)

Address: 2_H

Format:

bit 7							bit 0
0	0	EQUDIS	0	0	0	0	0

Initial Value: 00_H if the MODE pin is connected to V_{DD} or
20_H if the MODE pin is connected to V_{SS}

Description: **EQUDIS**: Disables the Equalizer when set to 1

4.5 Test Registers – (Read/Write)

Test registers are implemented in the address range of 8_H to A_H;
they are not for customer use.

4.6 Mode Register – (Write)

Address: B_H

Format:

bit 7							bit 0
DASL	0	0	0	0	0	0	0

Initial Value: 00_H

Description: **DASL** "1" enables DASL compatible behavior