Dual/Quad Single Supply Operational Amplifier

OP292/OP492

FEATURES

Single Supply Operation: 4.5 V to 33 V
Input Common Mode Includes Ground
Output Swings to Ground
High Slew Rate: 3 V/μs
High Gain Bandwidth: 4 MHz
Low Input Offset Voltage
High Open-Loop Gain
No Phase Inversion
Low Cost

APPLICATIONS

Disk Drives
Mobile Phones
Servo Controls
Modems and Fax Machines
Pagers
Power Supply Monitors and Controls
Battery Operated Instrumentation

GENERAL DESCRIPTION

The OP292/OP492 are low cost general purpose dual and quad operational amplifiers designed for single supply applications and are ideal for +5 volt systems.

Fabricated on Analog Devices' CBCMOS process, the OP292/OP492 series has a PNP input stage that allows the input voltage range to include ground. A BiCMOS output stage enables the output to swing to ground while sinking current.

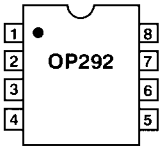
The OP292/OP492 series is unity-gain stable and features an outstanding combination of speed and performance for single or dual supply operation. The OP292/OP492 provide high slew rate, high bandwidth, with open-loop gain exceeding 40,000 and offset voltage under 800 μV (OP292) and 1 mV (OP492). With these combinations of features and low supply current, the OP292/OP492 series is an excellent choice for battery operated applications.

The OP292/OP492 series performance is specified for single or dual supply voltage operation over the extended industrial temperature range (−40°C to +125°C).

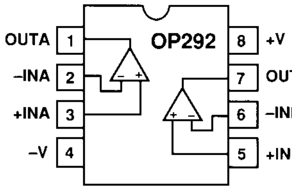
Package options for the OP292 and OP492 include plastic DIP, SO-8 (OP292) and SO-14.

PIN CONNECTIONS

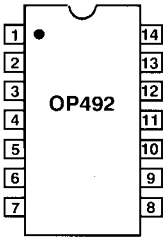
8-Lead Narrow-Body SO
(S Suffix)



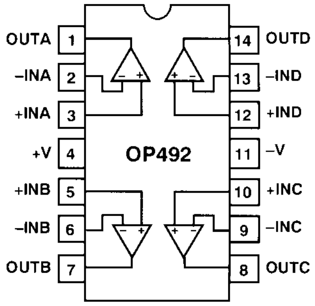
8-Lead Epoxy DIP
(P Suffix)



14-Lead Narrow-Body SO
(S Suffix)



14-Lead Epoxy DIP
(P Suffix)



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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703

OP292/OP492—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = +5 V, V_{CM} = 0 V, V_O = +2 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}					
OP292				0.1	0.8	mV
		−40°C ≤ T_A ≤ +85°C		0.3	1.2	mV
		−40°C ≤ T_A ≤ +125°C		0.5	2.5	mV
OP492	V_{OS}			0.1	1	mV
		−40°C ≤ T_A ≤ +85°C		0.3	1.5	mV
		−40°C ≤ T_A ≤ +125°C		0.5	2.5	mV
Input Bias Current	I_B			450	700	nA
		−40°C ≤ T_A ≤ +85°C		0.75	2.5	µA
		−40°C ≤ T_A ≤ +125°C		3.0	5.0	µA
Input Offset Current	I_{OS}			7	50	nA
		−40°C ≤ T_A ≤ +85°C		100	700	nA
		−40°C ≤ T_A ≤ +125°C		0.4	1.2	µA
Input Voltage Range			0		4.0	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 4.0 V	75	95		dB
		−40°C ≤ T_A ≤ +85°C	70	93		dB
		−40°C ≤ T_A ≤ +125°C	65	90		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O = 0.1 V to 4 V	25	200		V/mV
		−40°C ≤ T_A ≤ +85°C	10	100		V/mV
		−40°C ≤ T_A ≤ +125°C	5	50		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		2	10	µV/°C
Long Term V_{OS} Drift	$\Delta V_{OS}/\Delta t$	Note 1		1		µV/Month
Bias Current Drift	$\Delta I_B/\Delta T$	−40°C ≤ T_A ≤ +85°C		6		pA/°C
		−40°C ≤ T_A ≤ +125°C		400		pA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$	−40°C ≤ T_A ≤ +85°C		1.5		pA/°C
		−40°C ≤ T_A ≤ +125°C		2		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing						
High	V_{OUT}	R_L = 100 kΩ to GND				
		−40°C ≤ T_A ≤ +125°C	4.0	4.3		V
		R_L = 2 kΩ to GND	3.8	4.1		V
		−40°C ≤ T_A ≤ +125°C	3.7	3.9		V
Low	V_{OUT}	R_L = 100 kΩ to V+		8	20	mV
		−40°C ≤ T_A ≤ +125°C		12	20	mV
		R_L = 2 kΩ to V+		280	450	mV
		−40°C ≤ T_A ≤ +125°C		300	550	mV
Short Circuit Current Limit	I_{SC}		5	8		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 4.5 V to +30 V, V_O = 2 V	75	95		dB
		−40°C ≤ T_A ≤ +125°C	70	90		dB
Supply Current Per Amp	I_{SY}	V_O = 2 V				
OP292, OP492				0.8	1.2	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ		3		V/µs
		−40°C ≤ T_A ≤ +125°C	1	2		V/µs
Gain Bandwidth Product	GBP			4		MHz
Phase Margin	ϕ_m			75		Degrees
Channel Separation	CS	f_O = 1 kHz		100		dB
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		25		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		15		nV/√Hz
Current Noise Density	i_n			0.7		pA/√Hz

NOTES

[1] Long term offset voltage drift is guaranteed by 1000 hours life test performed on three independent wafer lots at +125°C with LTPD of 1.3.

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ $V_S = \pm15$ V, $T_A = +25°C$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}					
OP292				1.0	2.0	mV
		$-40°C \le T_A \le +85°C$		1.2	2.5	mV
		$-40°C \le T_A \le +125°C$		1.5	3	mV
OP492				1.4	2.5	mV
		$-40°C \le T_A \le +85°C$		1.7	2.8	mV
		$-40°C \le T_A \le +125°C$		2	3	mV
Input Bias Current	I_B			375	700	nA
		$-40°C \le T_A \le +125°C$		0.5	1	μA
Input Offset Current	I_{OS}			7	50	nA
		$-40°C \le T_A \le +85°C$		20	100	nA
		$-40°C \le T_A \le +125°C$		0.4	1.2	μA
Input Voltage Range		Note 1	−11		11	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm11$ V	78	100		dB
		$-40°C \le T_A \le +125°C$	75	95		dB
Large Signal Voltage Gain	A_{VO}	$R_L = 10$ kΩ, $V_O = \pm10$ V	25	120		V/mV
		$-40°C \le T_A \le +85°C$	10	75		V/mV
		$-40°C \le T_A \le +125°C$	5	60		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40°C \le T_A \le +125°C$		4	10	μV/°C
Bias Current Drift	$\Delta I_B/\Delta T$	$-40°C \le T_A \le +125°C$		3		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	$R_L = 2$ kΩ to GND	±11	±12.2		V
		$-40°C \le T_A \le +125°C$	±10	±11		V
		$R_L = 100$ kΩ to GND	±13.8	±14.3		V
		$-40°C \le T_A \le +125°C$	±13.5	±14.0		mV
Short Circuit Current Limit	I_{SC}	Short Circuit to GND	8	10.5		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = \pm2.25$ V to ±15 V	75	86		dB
		$-40°C \le T_A \le +125°C$	70	83		dB
Supply Current Per Amp	I_{SY}	$V_O = 0$ V				
OP292, OP492				1	1.4	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 10$ kΩ	2.5	4		V/μs
		$-40°C \le T_A \le +125°C$	2	3		V/μs
Gain Bandwidth Product	GBP			4		MHz
Phase Margin	ϕ_m			75		Degrees
Channel Separation	CS	$f_O = 1$ kHz		100		dB
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		25		μV p-p
Voltage Noise Density	e_n	f = 1 kHz		15		$nV/\sqrt{Hz}$
Current Noise Density	i_n			0.7		$pA/\sqrt{Hz}$

NOTES

[1] Input voltage range is guaranteed by CMRR tests.

Specifications subject to change without notice.

WAFER TEST LIMITS (@ V_S = +5.0 V, V_{CM} = 2.5 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Limit	Units
Offset Voltage	V_{OS}		±600	μV max
Input Bias Current	I_B		700	nA max
Input Offset Current	I_{OS}		50	nA max
Input Voltage Range[1]	V_{CM}		0/4	V min/V max
Common-Mode Rejection	CMRR	V_{CM} = 0 V to 4.0 V	75	dB min
Power Supply Rejection Ratio	PSRR	V = ±4.5 V to ±15 V	75	dB min
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O = 0.1 V to 4 V	25	V/mV min
Output Voltage	V_O	R_L = 2 kΩ	3.8	V min
Supply Current per Amp OP292, OP492	I_{SY}	V_O = 0 V, R_L = Open	1.2	mA max

NOTES

Electrical tests and wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

[1] Guaranteed by CMR test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . +33 V
Input Voltage[2] . . . . −15 V to +14 V
Differential Input Voltage[2] V
Output Short-Circuit Duration . . . . UNLIMITED
Storage Temperature Range
P, S Package . . . . −65°C to +150°C
Operating Temperature Range
OP292/OP492 P, S . . . . −40°C to +125°C
Junction Temperature Range
P, S Package . . . . −65°C to +125°C
Lead Temperature Range (Soldering, 60 sec) . . . . +300°C

Package Type	θ_{JA}[3]	θ_{JC}	Units
8-Pin Plastic DIP (P)	103	43	°C/W
14-Pin Plastic DIP (P)	83	39	°C/W
8-Pin SO (S)	158	43	°C/W
14-Pin SO (S)	120	36	°C/W

NOTES

[1] Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

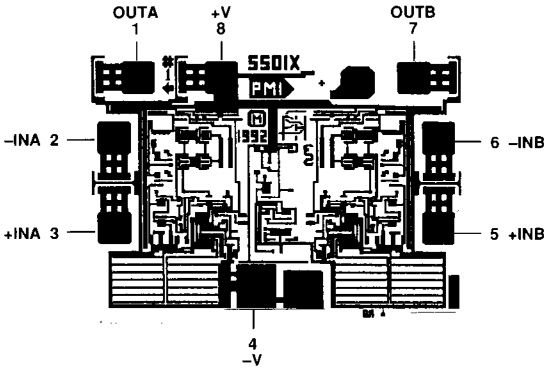
[2] For supply voltages less than +36 V, the absolute maximum input voltage is equal to the supply voltage.

[3] θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for P-DIP package; θ_{JA} is specified for device soldered in circuit board for SOIC package.

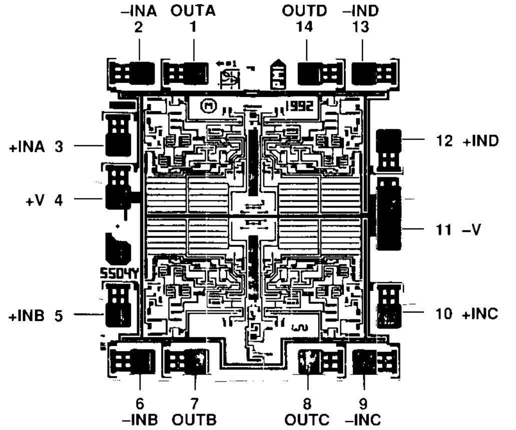
ORDERING GUIDE

Model	Temperature Range	Package Option
OP292GP	−40°C to +125°C	N-8
OP292GS	−40°C to +125°C	SO-8
OP492GP	−40°C to +125°C	N-14
OP492GS	−40°C to +125°C	SO-14
OP292/492GBC	+25°C	DICE

DICE CHARACTERISTICS



OP292 Die Size 0.040 × 0.057 Inch, 2,280 Sq. Mils Substrate Connected to V+, Number of Transistors: Bipolar 47, MOSFET 5.



OP492 Die Size 0.057 × 0.068 Inch, 3,876 Sq. Mils Substrate Connected to V+, Number of Transistors: Bipolar 91, MOSFET 9.

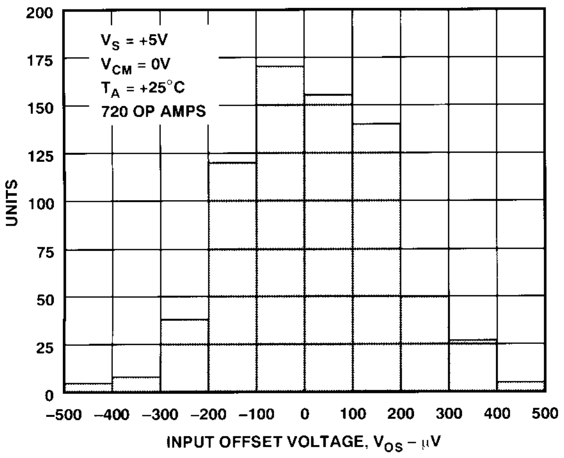


Figure 1. OP292 Input Offset Voltage Distribution @ +5 V

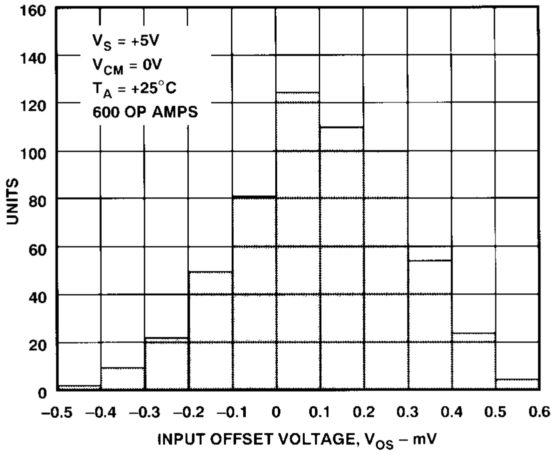


Figure 4. OP492 Input Offset Voltage Distribution @ +5 V

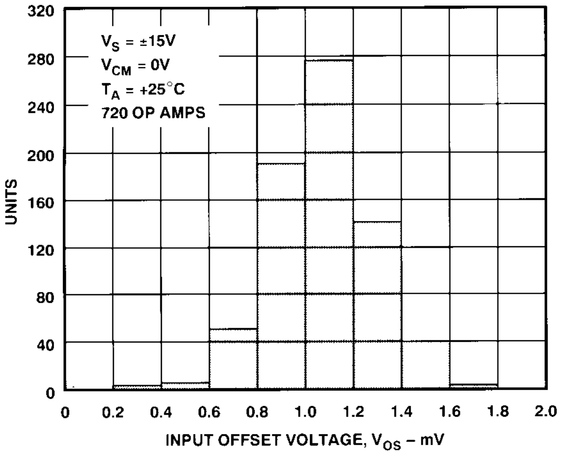


Figure 2. OP292 Input Offset Voltage Distribution @ ±15 V

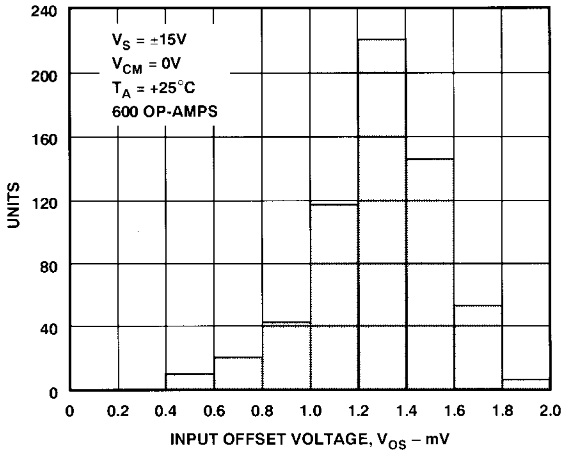


Figure 5. OP492 Input Offset Voltage Distribution @ ±15 V

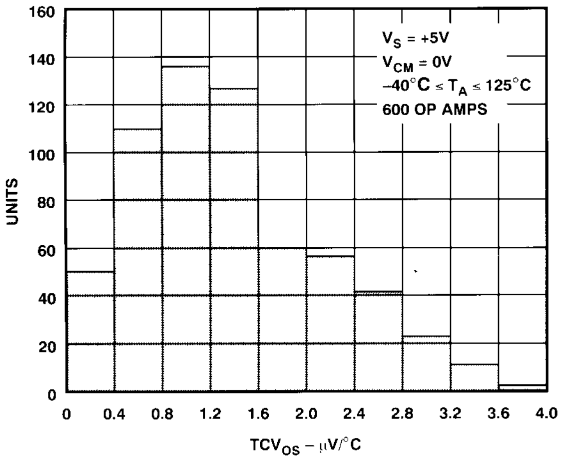


Figure 3. OP292 Temperature Drift (TCV_{OS}) Distribution @ +5 V

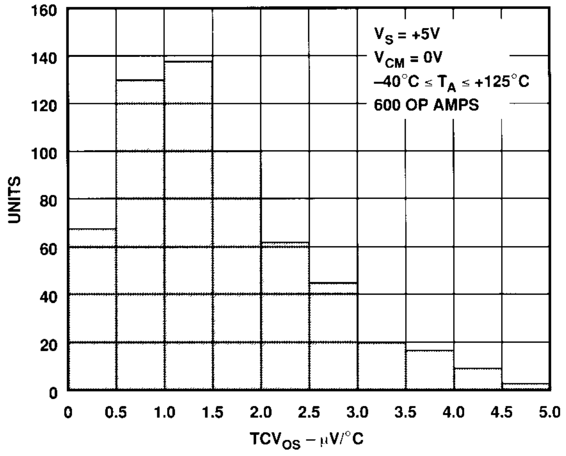


Figure 6. OP492 Temperature Drift (TCV_{OS}) Distribution @ +5 V

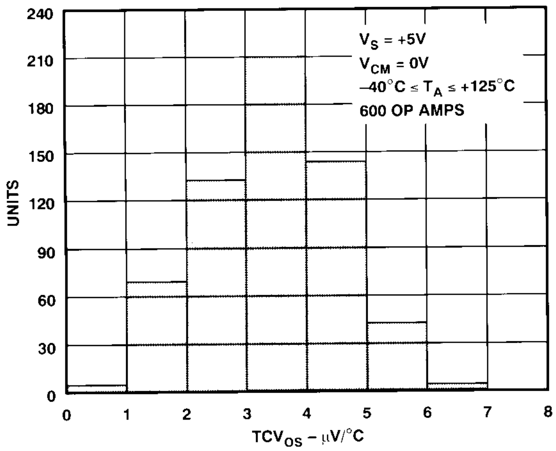


Figure 7. OP292 Temperature Drift (TCV$_{OS}$) Distribution @ ±15 V

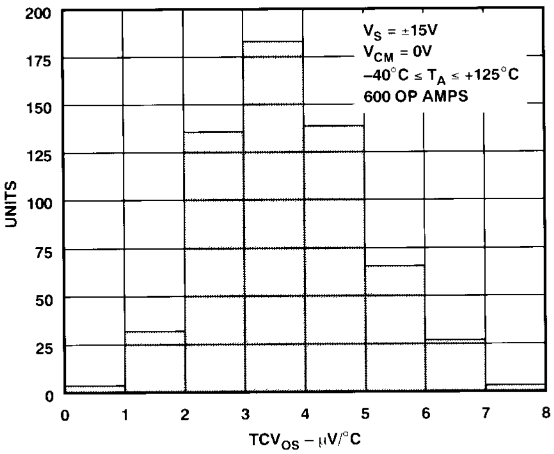


Figure 10. OP492 Temperature Drift (TCV$_{OS}$) Distribution @ ±15 V

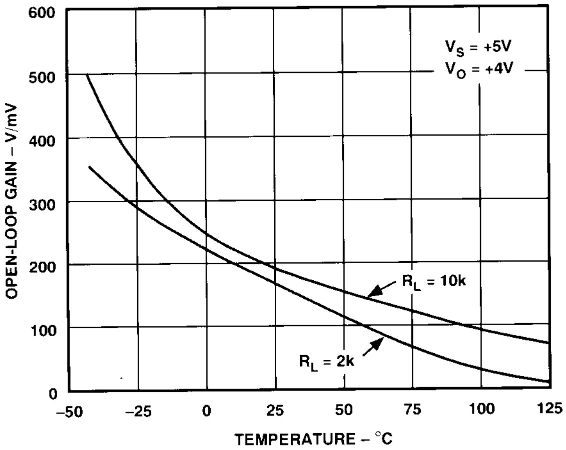


Figure 8. OP292 Open-Loop Gain vs. Temperature @ +5 V

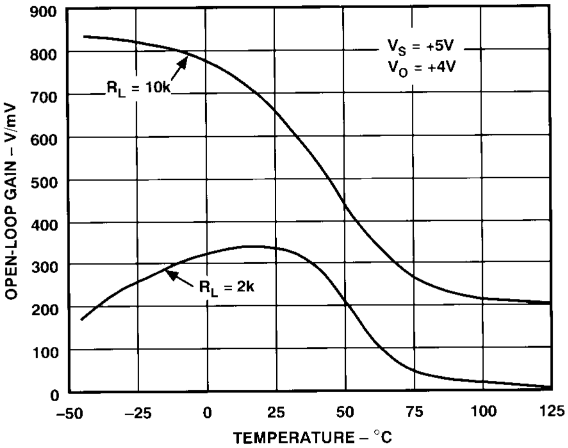


Figure 11. OP492 Open-Loop Gain vs. Temperature @ +5 V

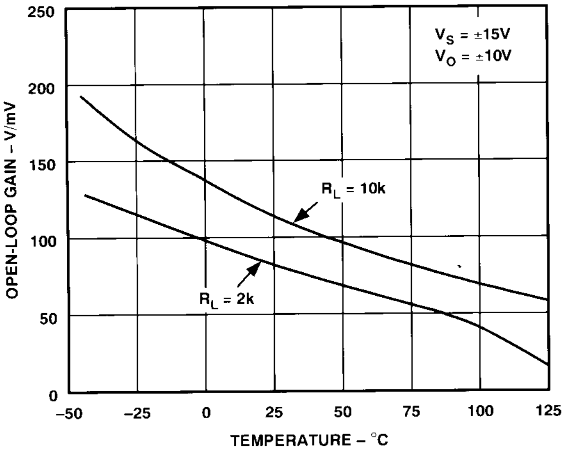


Figure 9. OP292 Open-Loop Gain vs. Temperature @ ±15 V

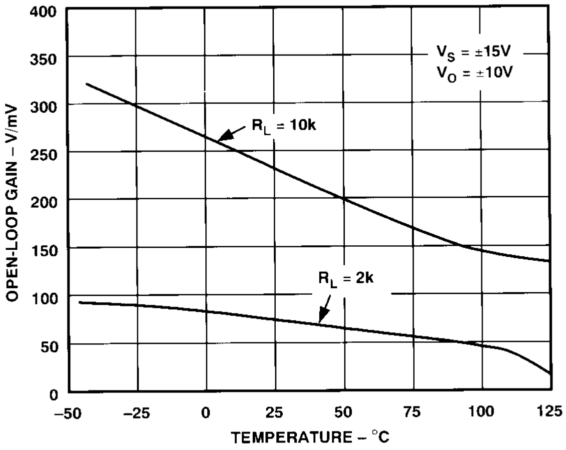


Figure 12. OP492 Open-Loop Gain vs. Temperature @ ±15 V

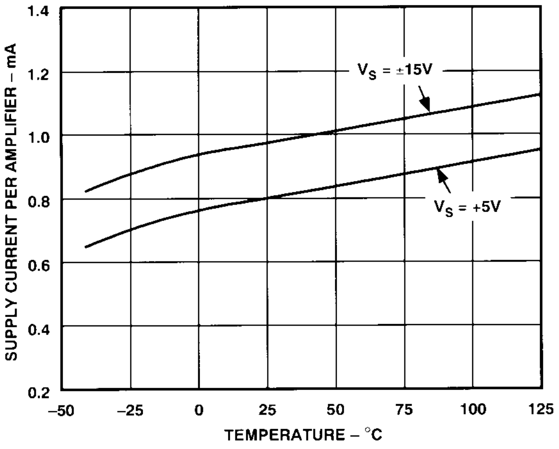


Figure 13. OP292 Supply Current per Amplifier vs. Temperature

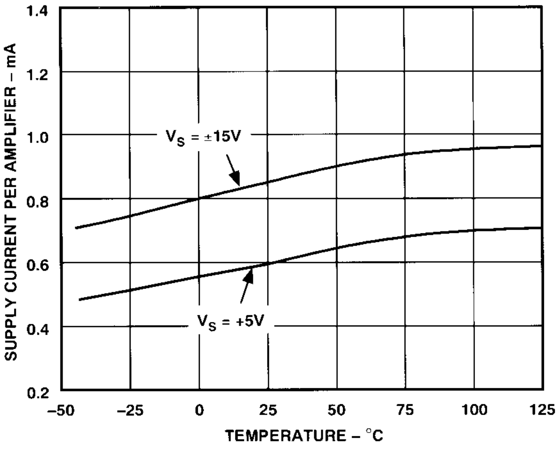


Figure 16. OP492 Supply Current per Amplifier vs. Temperature

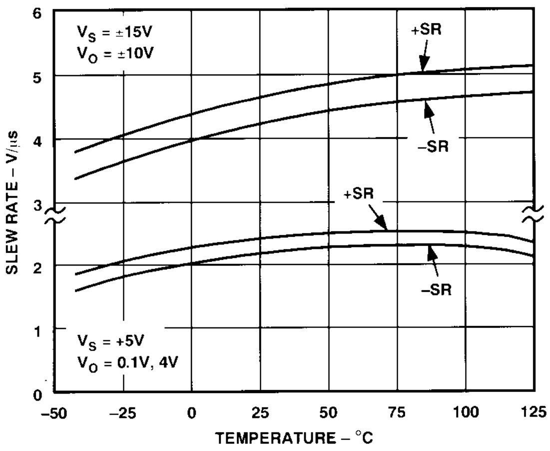


Figure 14. OP292 Slew-Rate vs. Temperature

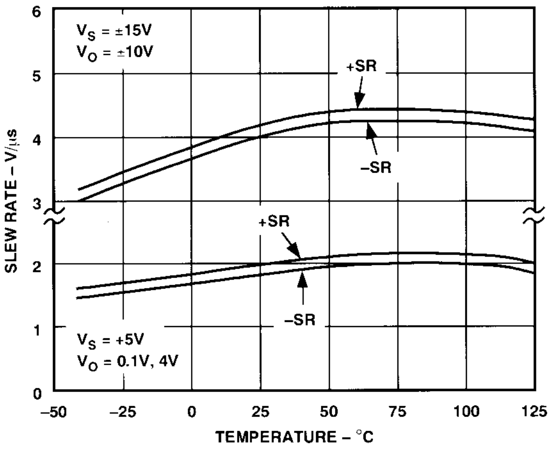


Figure 17. OP492 Slew-Rate vs. Temperature

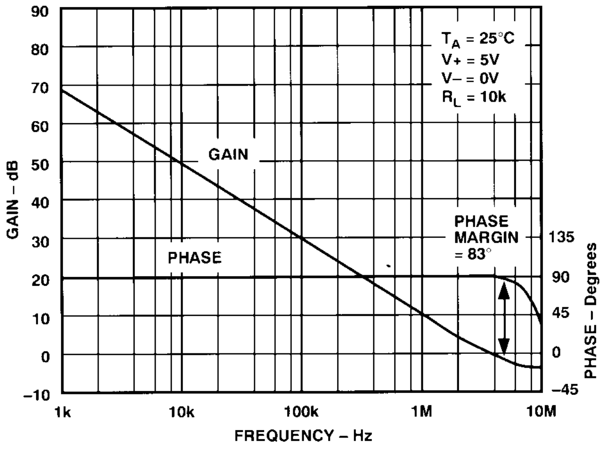


Figure 15. OP292/OP492 Open-Loop Gain and Phase vs. Frequency @ +5 V

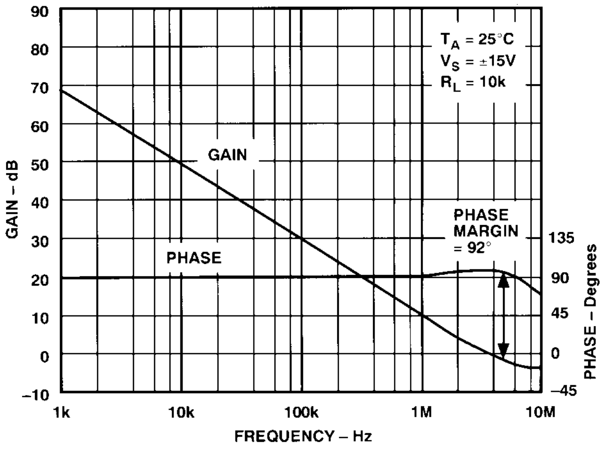


Figure 18. OP292/OP492 Open-Loop Gain/Phase vs. Frequency @ ±15 V

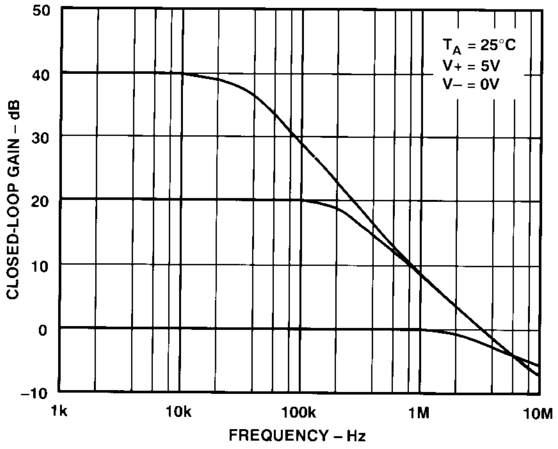


Figure 19. OP292/OP492 Closed-Loop Gain/Phase vs. Frequency @ +5 V

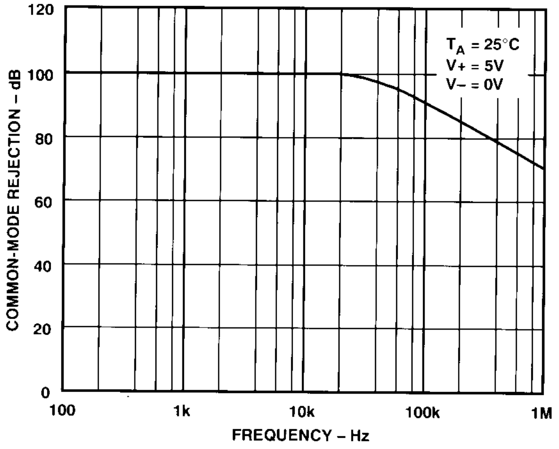


Figure 20. OP292/OP492 CMR vs. Frequency @ +5 V

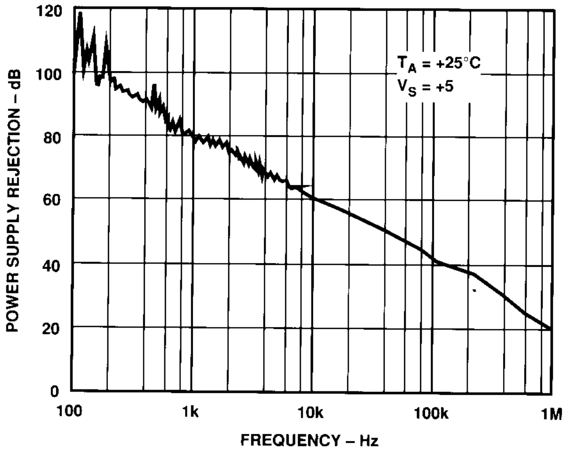


Figure 21. OP292/OP492 PSR vs. Frequency @ +5 V

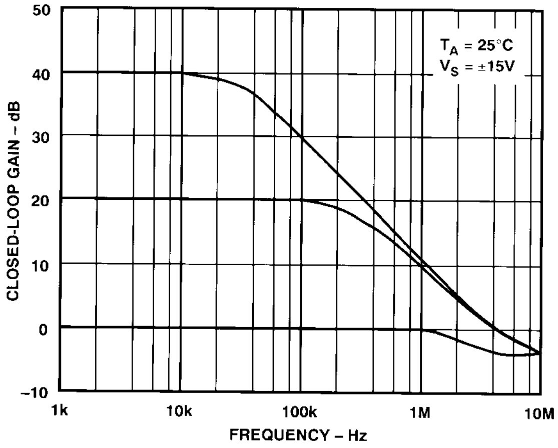


Figure 22. OP292/OP492 Closed-Loop Gain/Phase vs. Frequency @ ±15 V

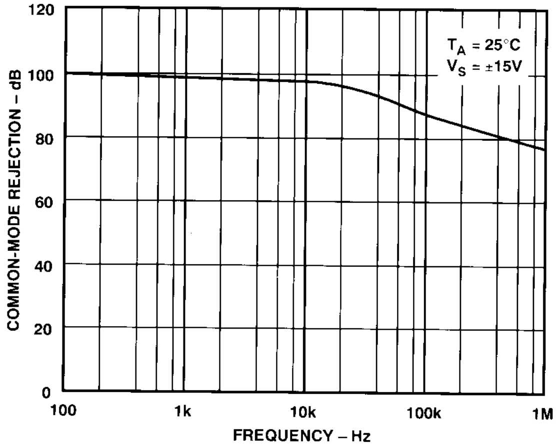


Figure 23. OP292/OP492 CMR vs. Frequency @ ±15 V

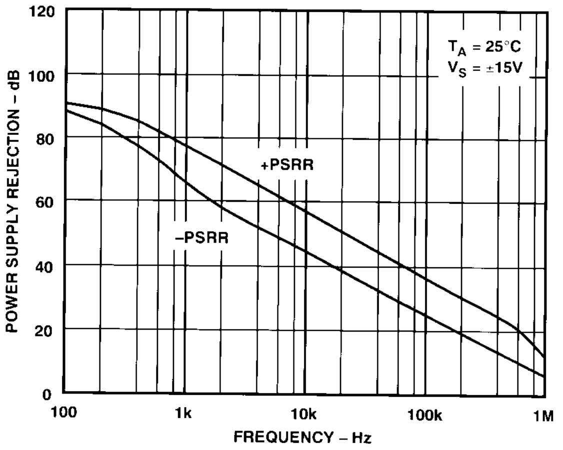


Figure 24. OP292/OP492 PSR vs. Frequency @ ±15 V

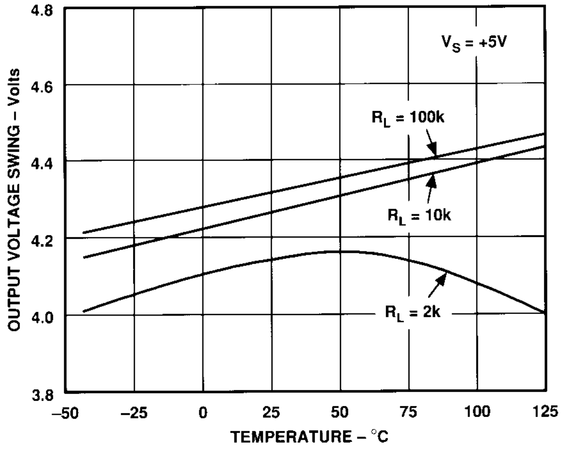


Figure 25. OP292/OP492 V_{OUT} Swing vs. Temperature @ +5 V

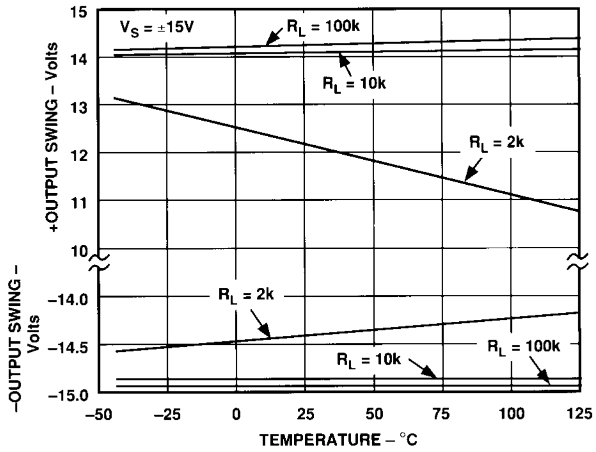


Figure 28. OP292/OP492 V_{OUT} Swing vs. Temperature @ ±15 V

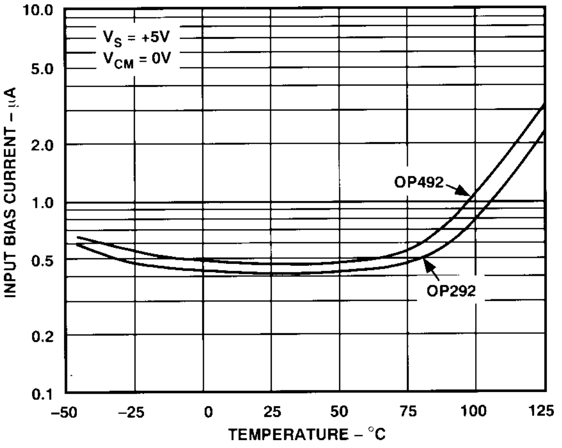


Figure 26. OP292/OP492 Input Bias Current vs. Temperature @ +5 V

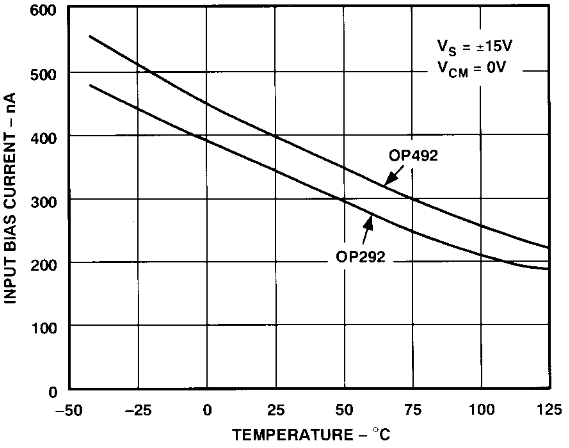


Figure 29. OP292/OP492 Input Bias Current vs. Temperature @ ±15 V

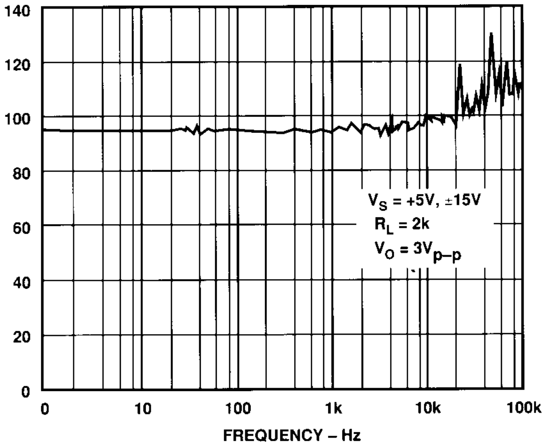


Figure 27. OP292/OP492 Channel Separation

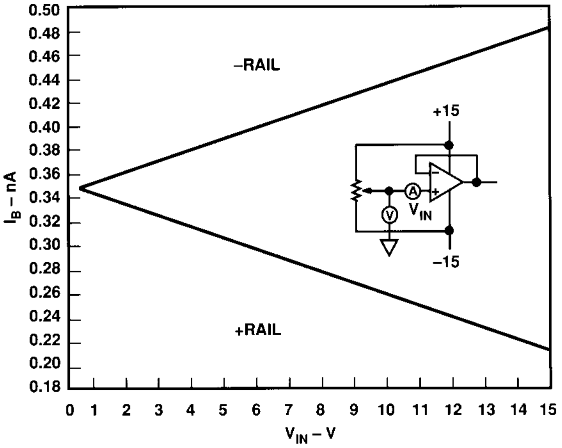


Figure 30. OP292/OP492 I_B Current vs. Common Mode Voltage

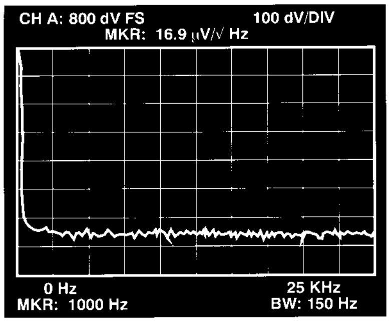


Figure 31. Voltage Noise Density

APPLICATION INFORMATION

PHASE REVERSAL

The OP492 has built-in protection against phase reversal when the input voltage goes to either supply rail. In fact it is safe for the input to exceed either supply rail by up to 0.6 V with no risk of phase reversal. However, the input should not go beyond the positive supply rail by more than 0.9 V, otherwise the output will reverse phase. If this condition can occur, the problem can be fixed by adding a 5 kΩ current limiting resistor in series with the input pin. With this addition, the input can go to more than 5 V beyond the positive rail without phase reversal.

An input voltage that is as much as 5 V below the negative rail will not result in phase reversal.

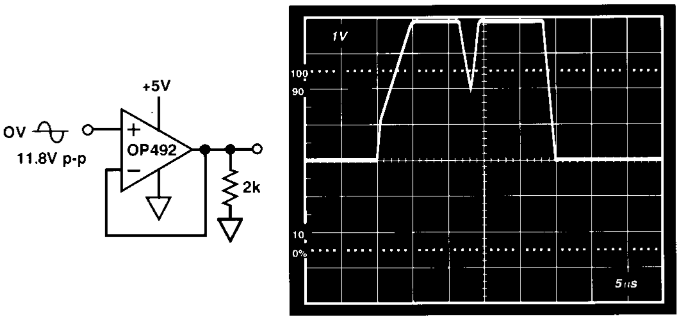


Figure 32. Output Can Reverse Phase If Input Exceeds the Positive Supply (V+) by More Than 0.9 V

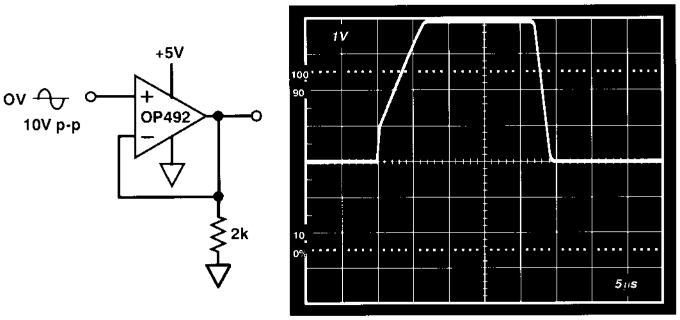


Figure 33. No Negative Rail Phase Reversal, Even with Input Signal at 5 V Below Ground

Power Supply Considerations

The OP292/OP492 are designed to operate equally well at single +5 V or ±15 V supplies. The lowest supply voltage recommended is 4.5 V.

It is a good design practice to bypass the supply pins with a 0.1 μF ceramic capacitor. It helps improve filtering of high frequency noise.

For dual supply operation, the negative supply (V−) must be applied at the same time, or before V+. If V+ is applied before V−, or in the case of a loss of V− supply, while either input is connected to ground or other low impedance source, excessive input current may result. Potentially damaging levels of input current can destroy the amplifier. If this condition can exist, simply add a 1k or larger resistor in series with the input to eliminate the problem.

TYPICAL APPLICATIONS

Direct Access Arrangement for Telephone Line Interface

Figure 34 shows a +5 V-only transmit/receive telephone line interface for a modem circuit. It allows full duplex transmission of modem signals on a transformer-coupled 600 Ω line in a differential manner. The transmit section gain can be set for the specific modem device output. Similarly the receive amplifier gain can be appropriately selected based on the modem device input requirements. The circuit operates on a single +5 V supply. The standard value resistors allow the use of a SIP packaged resistor array; this, coupled with a quad op amp in a single package, offers a compact, low part-count solution.

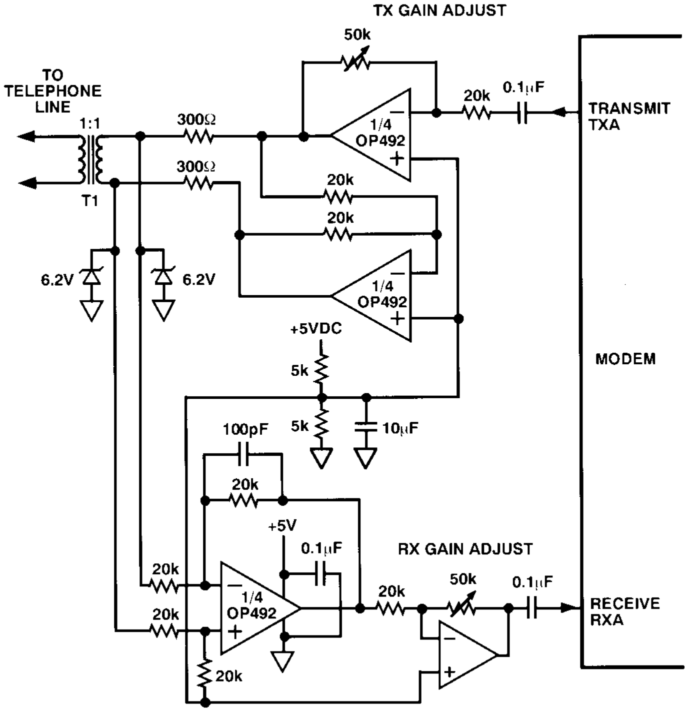


Figure 34. A Universal Direct Access Arrangement for Telephone Line Interface

A Single Supply Instrumentation Amplifier

A low cost single supply instrumentation amplifier can be built as shown in Figure 35. The circuit utilizes two op amps to form a high input impedance differential amplifier. Gain can be set by selecting resistor R_G which can be calculated using the transfer function equation. Normally, $V_{REFERENCE}$ is set to 0 V. Then the output voltage is a function of the gain times the differential input voltage. However, the output can be offset by setting $V_{REFERENCE}$ from 0 V to 4 V, as long as the input common-mode voltage of the amplifier is not exceeded.

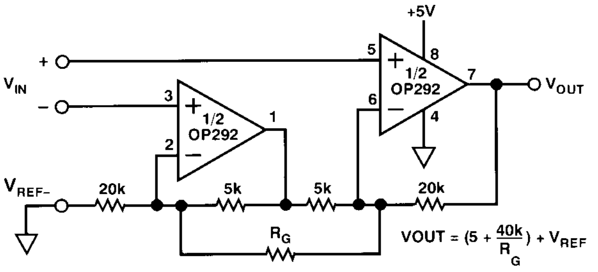


Figure 35. A Single Supply Instrumentation Amplifier

In this configuration, while the output can swing to near zero volts, one needs to be careful because the input's common-mode voltage range cannot operate to zero volts. This is because of the limitation of the circuit configuration where the first amplifier must be able to swing below ground in order to attain a 0 V common-mode voltage, which it cannot do. Depending on the gain of the instrumentation amplifier, the input common-mode extends to within about 0.3 V of zero. One can easily calculate the worst-case common-mode limit for a given gain.

DAC Output Amplifier

The OP292/OP492 are ideal for buffering the output of single supply D/A converters. Figure 36 shows a typical amplifier used to buffer the output of a CMOS DAC that is connected for single supply operation. To do that, the normally current output 12-bit CMOS DAC (R-2R ladder type) is connected backward to produce a voltage output. This operating configuration necessitates a low voltage reference. In this case, a 1.235 V low power reference is used. The relatively high output impedance (10k) is buffered by the OP292 and at the same time gained up to a much more usable level. The potentiometer provides an accurate gain trim for a 4.095 V full-scale, allowing 1 mV increment per LSB of control resolution.

The DAC8043 device comes in an 8-pin DIP package providing a cost-effective, compact solution to a 12-bit analog channel.

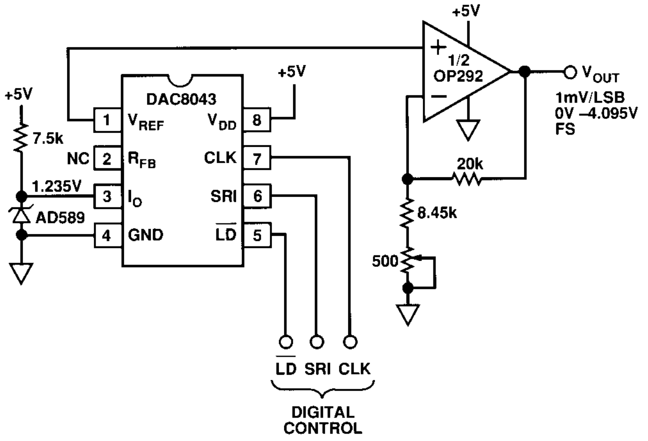
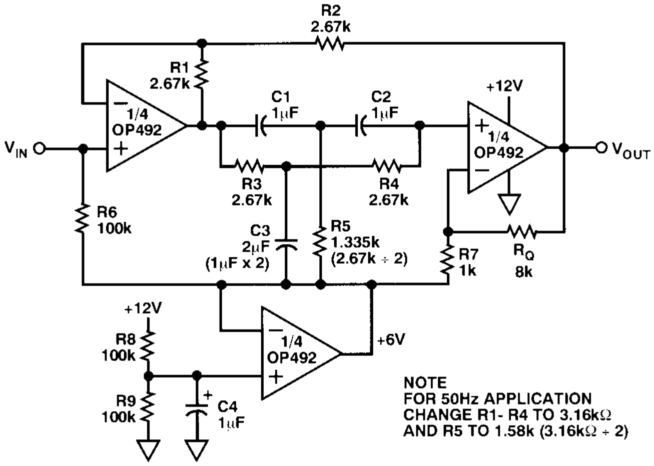


Figure 36. A 12-Bit Single-Supply DAC With Serial Bus Control

A 50 Hz/60 Hz Single-Supply Notch Filter

Figure 37 shows a notch filter that achieves nearly 30 dB of 60 Hz rejection while powered by only a single 12 V supply. The circuit also works well on +5 V systems. The filter utilizes a twin-T configuration whose frequency selectivity depends heavily on the relative matching of the capacitors and resistors in the twin-T section. Mylar is a good choice for the twin-T's capacitors, and the relative matching of the capacitors and resistors determines the filter's passband symmetry. Using 1% resistors and 5% capacitors produces satisfactory results.

The amount of rejection and the Q of the filter is solely determined by one resistor, and is shown in the table. The bottom amplifier is used to split the supply to bias the amplifier to mid-level. The circuit can be modified to reject 50 Hz by simply changing the resistors in the twin-T section (R1 through R4) from 2.67k to 3.16k, and change R5 to 1/2 of 3.16k. For best results, the common value resistors can be from a resistor array for optimum matching characteristics.



FILTER Q	R_Q (kΩ)	REJECTION (dB)	VOLTAGE GAIN
0.75	1.0	40	1.33
1.00	2.0	35	1.50
1.25	3.0	30	1.60
2.50	8.0	25	1.80
5.00	18	20	1.90
10.00	38	15	1.95

Figure 37. A Single-Supply 50 Hz/60 Hz Notch Filter

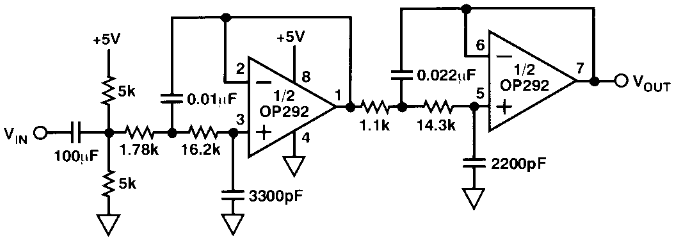


Figure 38. A 4-Pole Bessel Low Pass Filter Using Sallen-Key Topology

A 4-Pole Bessel Low-Pass Filter

The linear phase filter in Figure 38 is designed to roll off at a voiceband cutoff frequency of 3.6 kHz. The 4 poles are formed by two cascading stages of two-pole Sallen-Key filters.

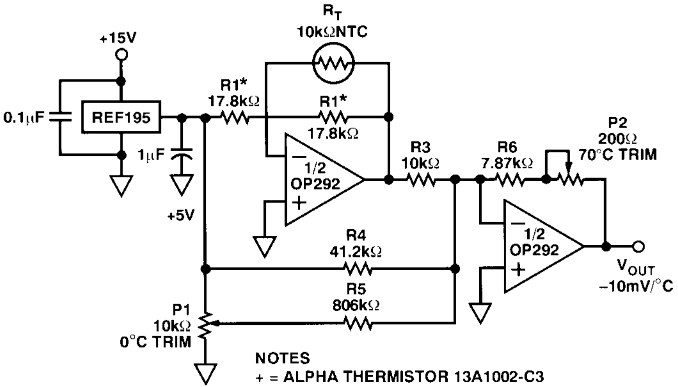
A Low Cost, Linearized Thermistor Amplifier

An inexpensive thermometer amplifier circuit can be implemented using low cost thermistors. One such implementation is shown in Figure 39. The circuit measures temperature over the range of 0°C to +70°C to an accuracy of ±0.3°C as the linearization circuit works well within a narrow temperature range. However, it can measure higher temperature but at a slightly reduced accuracy. To achieve the aforementioned accuracy, the thermistor's nonlinearity must be corrected. This is done by connecting the thermistor in parallel with the 10k in the feedback loop of the first stage amplifier. A constant operating current of 281 μA is supplied by the resistor R1 with the +5 V reference from the REF-195 such that the thermistor's self-heating error is kept below 0.1°C.

In many cases, the thermistor is placed some distance from the signal conditioning circuit. Under this condition, a 0.1 μF capacitor placed across R2 will help to suppress noise pickup.

This linearization network creates an offset voltage which is corrected by summing a compensating current with potentiometer P1. The temperature dependent signal is amplified by the second stage, producing a transfer coefficient of −10 mV/°C at the output.

To calibrate, a precision decade box can be used in place of the thermistor. For 0°C trim, the decade box is set to 32.650k, and P1 is adjusted until the circuit's output reads 0 V. To trim the circuit at the full-scale temperature of 70°C, the decade box is then set to 1.752k and P2 is adjusted until the circuit reads −0.70 V.



NOTES
+ = ALPHA THERMISTOR 13A1002-C3
* = 0.1% IMPERIAL ASTRONICS M015
ALL RESISTORS ARE 1%, 25 ppm/°C
EXCEPT R5 = 1%, 100 ppm/°C

Figure 39. A Low Cost Linearized Thermistor Amplifier

A Single-Supply Ultrasonic Clamping/Limiting Receiver Amplifier

Figure 40 shows an ultrasonic receiver amplifier using the nonlinear impedance of low cost diodes to effectively control the gain for wide dynamic range. This circuit amplifies a 40 kHz ultrasonic signal through a pair of low cost clamping amplifiers before feeding a bandpass filter to extract a clean 40 kHz signal for processing.

The signal is ac-coupled into the false-ground bias node by virtue of the capacitive piezoelectric sensing element. Rather than using an amplifier to generate a supply splitting bias, the false ground voltage is generated by a low cost resistive voltage divider.

Each amplifier stage provides ac gain while passing on the dc self-bias. As long as the output signal at each stage is less than a diode's forward voltage, each amplifier has unrestricted gain to amplify low level signals. However, as the signal strength increases, the feedback diodes begin to conduct, shunting the feedback current, and thus reducing the gain. Although distorting the waveform, the diodes effectively maintain a relatively constant amplitude even with large signals that otherwise would saturate the amplifier. In addition, this design is considerably more stable than the feedback type AGC.

The overall circuit has a gain range from −2 to −400, where the inversion comes from the bandpass filter stage. Operating with a Q of 5, the filter restores a clean, undistorted signal to the output. The circuit also work well with 5 V supply systems.

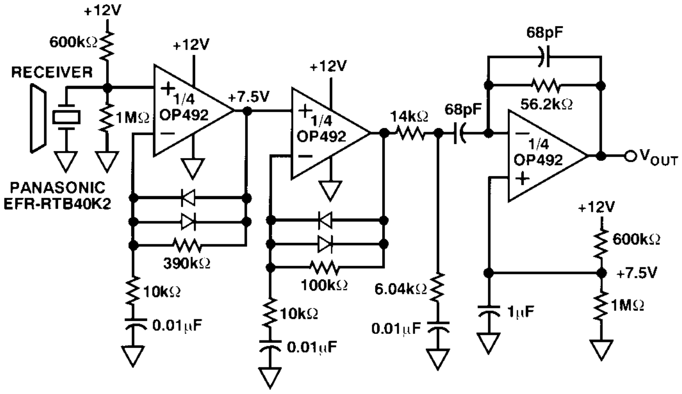


Figure 40. A 40 kHz Ultrasonic Clamping/Limiting Receiver Amplifier

Precision Single-Supply Voltage Comparator

The OP292/OP492 have excellent overload recovery characteristics, making them suitable for precision comparator applications. Figure 41 shows the saturation recovery characteristics of the OP492. The amplifier exhibits very little propagation delay. The amplifier compares a signal precisely to less than 0.5 mV offset error.

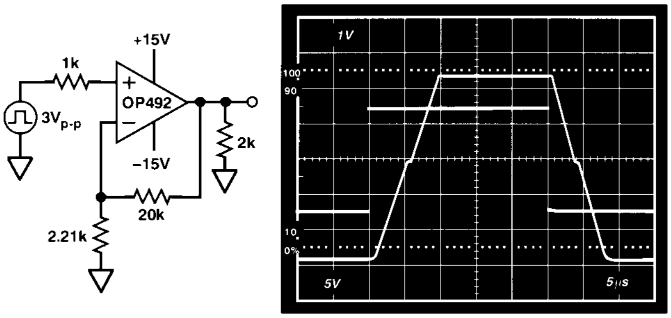


Figure 41. The OP492 Has Fast Overload Recovery for Comparator Applications

Programmable Precision Window Comparator

The OP292/OP492 can be used for precise level detection such as in test equipment where a signal is measured within a range. Figure 42 shows such an implementation. The threshold voltage level is set by a pair of 12-bit D/A converters. The DACs have serial interface thus minimizing interconnection requirements. The DAC8512 has a control resolution of 1 mV/bit. Thus for 5 V supply operation, maximum DAC output is 4.095 V. However, the OP292 will accept a maximum input of 4.0 V.

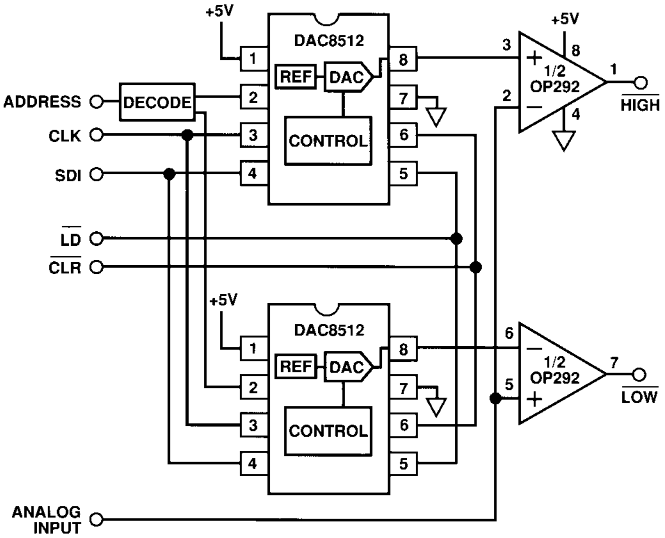


Figure 42. Programmable Window Comparator with 12-Bit Threshold Level Control

```
* OP292 SPICE Macro-model Rev. A, 6/93
*                         ARG / PMI
*
* Copyright 1993 by Analog Devices
*
* Refer to "README.DOC" file for License Statement. Use of
* this model indicates your acceptance of the terms and pro-
* visions in the License Statement.
*
* Node assignments
*                  noninverting input
*                  |  inverting input
*                  |  |    positive supply
*                  |  |    |   negative supply
*                  |  |    |   |    output
*                  |  |    |   |    |
.SUBCKT OP292      2  1   99  50   34
*
* INPUT STAGE AND POLE AT 40 MHz
*
I1      99   4    50E-6
IOS     2    1    10E-9
EOS     2    3    POLY(1) (21,30) 1.5E-3 75
CIN     1    2    3E-12
Q1      5    1    7     QP
Q2      6    3    8     QP
R3      5    50   2E3
R4      6    50   2E3
R5      4    7    966
R6      4    8    966
C1      5    6    .995E-12
*
* GAIN STAGE
*
EREF    98   0    (30,0)  1
G1      98   9    (5,6) 500E-6
R7      9    98   210.819E3
D1      9    10   DX
D2      11   9    DX
V1      99   10   .6
V2      11   50   .6
*
* ZERO/POLE AT 6 MHz/12 MHz
*
E1      12   98   (9,30)  2
R8      12   13   1
R9      13   98   1
C3      12   13   26.526E-9
*
* ZERO AT 15 MHz
*
E2      14   98   (13,30) 1E6
R10     14   15   1E6
R11     15   98   1
C4      14   15   10.610E-15
*
* COMMON MODE STAGE WITH ZERO AT 40 kHz
*
ECM     20   98   POLY(2)  (1,30)  (2,30)  0  0.5  0.5
R20     20   21   1E6
R21     21   98   1
C5      20   21   3.979E-12
```

```
*
* POLE AT 100 MHz
*
G2     98   16   (15,30) 1
R12    16   98   1
C6     16   98   1.592E-9
*
* OUTPUT STAGE
*
RS1    99   30   1E6
RS2    30   50   1E6
ISY    99   50   .44E-3
G3     31   50   POLY(1) (16,30) -1.635E-6 4E-6
R16    31   50   1E6
DCL    50   31   DZ
I2     99   32   250E-6
RCL    33   50   56
M1     32   31   50      50      MN L=9E-6 W=1000E-6 AD=15E-9 AS=15E-9
M2     34   31   50      50      MN L=9E-6 W=1000E-6 AD=15E-9 AS=15E-9
CC     31   32   14E-12
Q3     99   32   34      QNA
Q4     33   32   34      QPA
Q5     31   33   50      QNA
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+ ISE=2.57E-13 NE=5 BR=0.4 NR=0.988 VAR=15 IKR=1.465E-4
+ ISC=6.9E-16 NC=0.99 RB=2.0E3 IRB=7.73E-6 RBM=132.8 RE=4 RC=209
+ CJE=2.1E-13 VJE=0.573 MJE=0.364 FC=0.5 CJC=1.64E-13 VJC=0.534 MJC=0.5
+ CJS=1.37E-12 VJS=0.59 MJS=0.5 TF=0.43E-9 PTF=30)
.MODEL QPA PNP(IS=5.21E-17 BF=131 NF=0.99 VAF=62 IKF=8.35E-4
+ ISE=1.09E-14 NE=2.61 BR=0.5 NR=0.984 VAR=15 IKR=3.96E-5
+ ISC=7.58E-16 NC=0.985 RB=1.52E3 IRB=1.67E-5 RBM=368.5 RE=6.31 RC=354.4
+ CJE=1.1E-13 VJE=0.745 MJE=0.33 FC=0.5 CJC=2.37E-13 VJC=0.762 MJC=0.4
+ CJS=7.11E-13 VJS=0.45 MJS=0.412 TF=1.0E-9 PTF=30)
.MODEL MN NMOS(LEVEL=3 VTO=1.3 RS=0.3 RD=0.3
+ TOX=8.5E-8 LD=1.48E-6 WD=1E-6 NSUB=1.53E16 UO=650 DELTA=10 VMAX=2E5
+ XJ=1.75E-6 KAPPA=0.8 ETA=0.066 THETA=0.01 TPG=1 CJ=2.9E-4 PB=0.837
+ MJ=0.407 CJSW=0.5E-9 MJSW=0.33)
.MODEL QP PNP(BF=61.5)
.MODEL DX D
.MODEL DZ D(BV=3.6)
.ENDS OP292
```

```
* OP492 SPICE Macro-model              Rev. A, 6/93
*                                      ARG / PMI
*
* Copyright 1993 by Analog Devices
*
* Refer to "README.DOC" file for License Statement. Use of
* this model indicates your acceptance of the terms and pro-
* visions in the License Statement.
*
* Node assignments
*                      noninverting input
*                      |  inverting input
*                      |  |  positive supply
*                      |  |  |   negative supply
*                      |  |  |   |  output
*                      |  |  |   |  |
.SUBCKT OP492          2  1  99  50 34
*
* INPUT STAGE AND POLE AT 40 MHz
*
I1      99   4    50E-6
IOS     2    1    10E-9
EOS     2    3    POLY(1) (21,30) 1.5E-3 75
CIN     1    2    3E-12
Q1      5    1    7     QP
Q2      6    3    8     QP
R3      5    50   2E3
R4      6    50   2E3
R5      4    7    966
R6      4    8    966
C1      5    6    .995E-12
*
* GAIN STAGE
*
EREF    98   0    (30,0)   1
G1      98   9    (5,6)    500E-6
R7      9    98   210.819E3
D1      9    10   DX
D2      11   9    DX
V1      99   10   .6
V2      11   50   .6
*
* ZERO/POLE AT 6 MHz/12 MHz
*
E1      12   98   (9,30)   2
R8      12   13   1
R9      13   98   1
C3      12   13   26.526E-9
*
* ZERO AT 15 MHz
*
E2      14   98   (13,30)    1E6
R10     14   15   1E6
R11     15   98   1
C4      14   15   10.610E-15
*
* COMMON MODE STAGE WITH ZERO AT 40 kHz
*
ECM     20   98   POLY(2)   (1,30)   (2,30)   0   0.5   0.5
R20     20   21   1E6
R21     21   98   1
C5      20   21   3.979E-12
```

```
*
* POLE AT 100 MHz
*
G2    98   16   (15,30)   1
R12   16   98   1
C6    16   98   1.592E-9
*
* OUTPUT STAGE
*
RS1   99   30   1E6
RS2   30   50   1E6
ISY   99   50   .44E-3
G3    31   50   POLY(1)   (16,30)   -1.635E-6   4E-6
R16   31   50   1E6
DCL   50   31   DZ
I2    99   32   250E-6
RCL   33   50   56
M1    32   31   50   50   MN   L=9E-6   W=1000E-6   AD=15E-9   AS=15E-9
M2    34   31   50   50   MN   L=9E-6   W=1000E-6   AD=15E-9   AS=15E-9
CC    31   32   14E-12
Q3    99   32   34 QNA
Q4    33   32   34 QPA
Q5    31   33   50 QNA
.MODEL QNA NPN(IS=1.19E-16 BF=253 NF=0.99 VAF=193 IKF=2.76E-3
+ ISE=2.57E-13 NE=5 BR=0.4 NR=0.988 VAR=15 IKR=1.465E-4
+ ISC=6.9E-16 NC=0.99 RB=2.0E3 IRB=7.73E-6 RBM=132.8 RE=4 RC=209
+ CJE=2.1E-13 VJE=0.573 MJE=0.364 FC=0.5 CJC=1.64E-13 VJC=0.534 MJC=0.5
+ CJS=1.37E-12 VJS=0.59 MJS=0.5 TF=0.43E-9 PTF=30)
.MODEL QPA PNP(IS=5.21E-17 BF=131 NF=0.99 VAF=62 IKF=8.35E-4
+ ISE=1.09E-14 NE=2.61 BR=0.5 NR=0.984 VAR=15 IKR=3.96E-5
+ ISC=7.58E-16 NC=0.985 RB=1.52E3 IRB=1.67E-5 RBM=368.5 RE=6.31 RC=354.4
+ CJE=1.1E-13 VJE=0.745 MJE=0.33 FC=0.5 CJC=2.37E-13 VJC=0.762 MJC=0.4
+ CJS=7.11E-13 VJS=0.45 MJS=0.412 TF=1.0E-9 PTF=30)
.MODEL MN NMOS(LEVEL=3 VTO=1.3 RS=0.3 RD=0.3
+ TOX=8.5E-8 LD=1.48E-6 WD=1E-6 NSUB=1.53E16 UO=650 DELTA=10 VMAX=2E5
+ XJ=1.75E-6 KAPPA=0.8 ETA=0.066 THETA=0.01 TPG=1 CJ=2.9E-4 PB=0.837
+ MJ=0.407 CJSW=0.5E-9 MJSW=0.33)
.MODEL QP PNP(BF=61.5)
.MODEL DX D
.MODEL DZ D(BV=3.6)
.ENDS OP492
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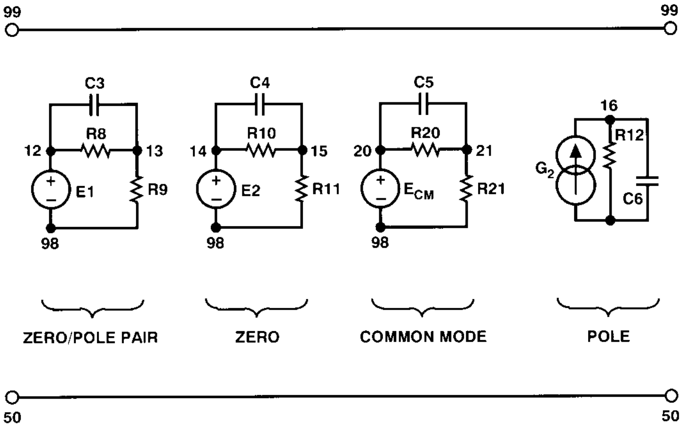
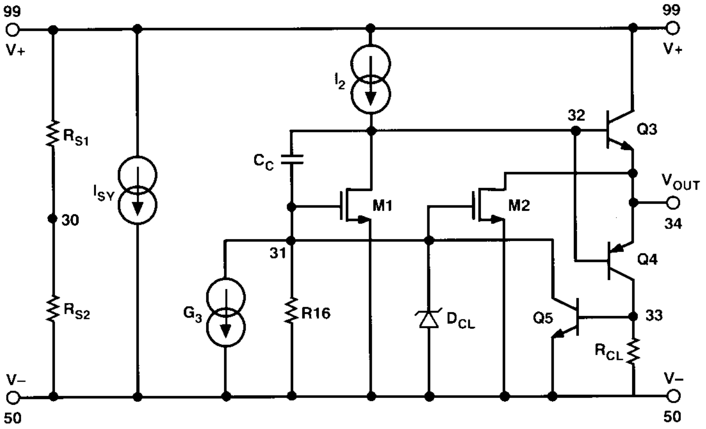
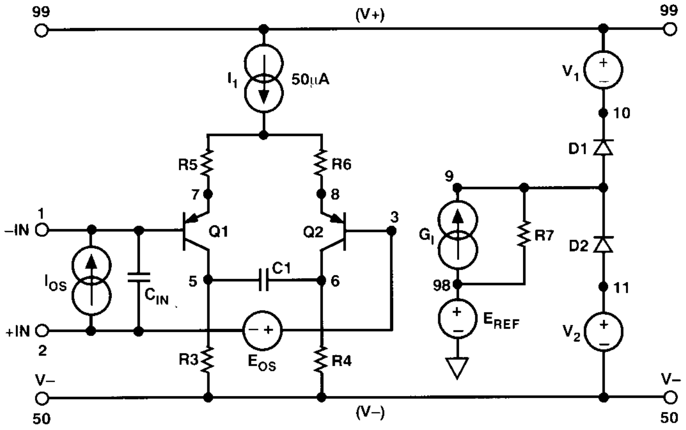
OP292/OP492 SPICE







OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

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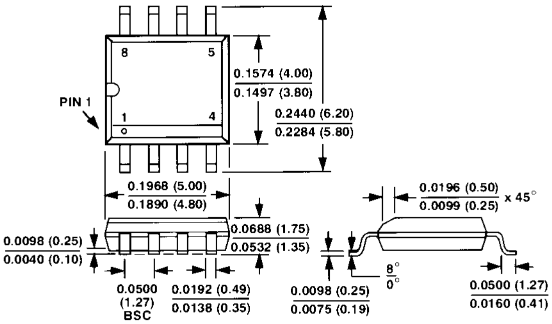
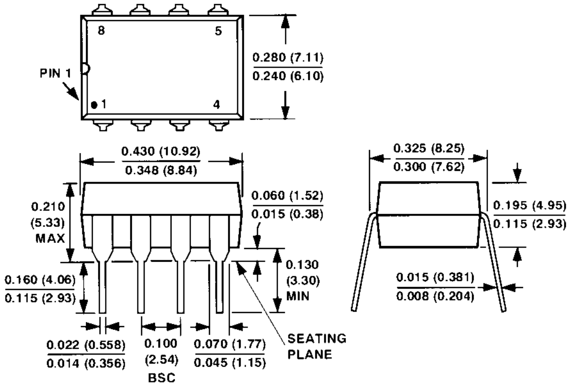
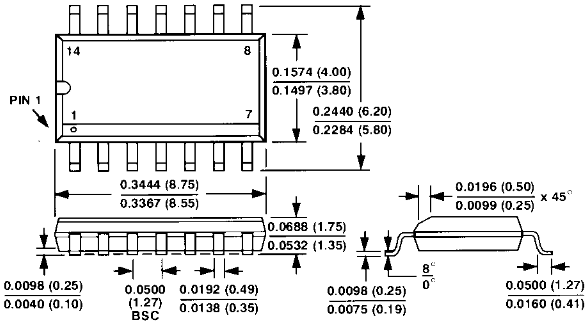
(S Suffix)



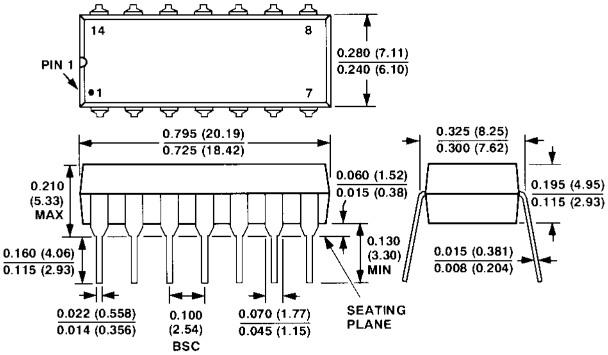
N-8
8-Lead Epoxy DIP
(P Suffix)



SO-14
14-Lead Narrow-Body SOIC
(S Suffix)



N-14
14-Lead Epoxy DIP
(P Suffix)



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