PRELIMINARY

8XC51GB
CHMOS SINGLE-CHIP 8-BIT MICROCONTROLLER

Commercial/Express

87C51GB—8 Kbytes OTP/8 Kbytes Internal Program Memory
83C51GB—8 Kbytes Factory Programmable ROM
80C51GB—CPU with RAM and I/O
8XC51GB—3.5 MHz to 12 MHz ±20% V_{CC}
8XC51GB-1—3.5 MHz to 16 MHz ±20% V_{CC}

- 8 Kbytes On-Chip ROM/OTP ROM
- 256 Bytes of On-Chip Data RAM
- Two Programmable Counter Arrays with:
  - — 2 x 5 High Speed Input/Output Channels Compare/Capture
  - — Pulse Width Modulators
  - — Watchdog Timer Capabilities
- Three 16-Bit Timer/Counters with
  - — Four Programmable Modes:
  - — Capture, Baud Rate Generation (Timer 2)
- Dedicated Watchdog Timer
- 8-Bit, 8-Channel A/D with:
  - — Eight 8-Bit Result Registers
  - — Four Programmable Modes
- Programmable Serial Channel with:
  - — Framing Error Detection
  - — Automatic Address Recognition
- Serial Expansion Port
- Programmable Clock Out
- Extended Temperature Range: (−40°C to +85°C)
- 48 Programmable I/O Lines with 40 Schmitt Trigger Inputs
- 15 Interrupt Sources with:
  - — 7 External, 8 Internal Sources
  - — 4 Programmable Priority Levels
- Pre-Determined Port States on Reset
- High Performance CHMOS Process
- TTL and CHMOS Compatible Logic Levels
- Power Saving Modes
- 64K External Data Memory Space
- 64K External Program Memory Space
- Three Level Program Lock System
- ONCE (ON-Circuit Emulation) Mode
- Quick Pulse Programming Algorithm
- MCS® 51 Microcontroller Fully Compatible Instruction Set
- Boolean Processor
- Oscillator Fail Detect
- Available in 68-Pin PLCC

MEMORY ORGANIZATION

PROGRAM MEMORY: Up to 8 Kbytes of the program memory can reside in the on-chip ROM. Also, the device can address up to 64K of program memory external to the chip.

DATA MEMORY: This microcontroller has a 256 x 8 on-chip RAM. In addition it can address up to 64 Kbytes of external data memory.

The Intel 8XC51GB is a single-chip control oriented microcontroller which is fabricated on Intel's CHMOS III-E technology. The 8XC51GB is an enhanced version of the 8XC51FA and uses the same powerful instruction set and architecture as existing MCS 51 microcontroller products. Added features make it an even more powerful microcontroller for applications that require On-Chip A/D, Pulse Width Modulation, High Speed I/O, up/down counting capabilities and memory protection features. It also has a more versatile serial channel that facilitates multi-processor communications.

November 1994 **Order Number: 272337-002**

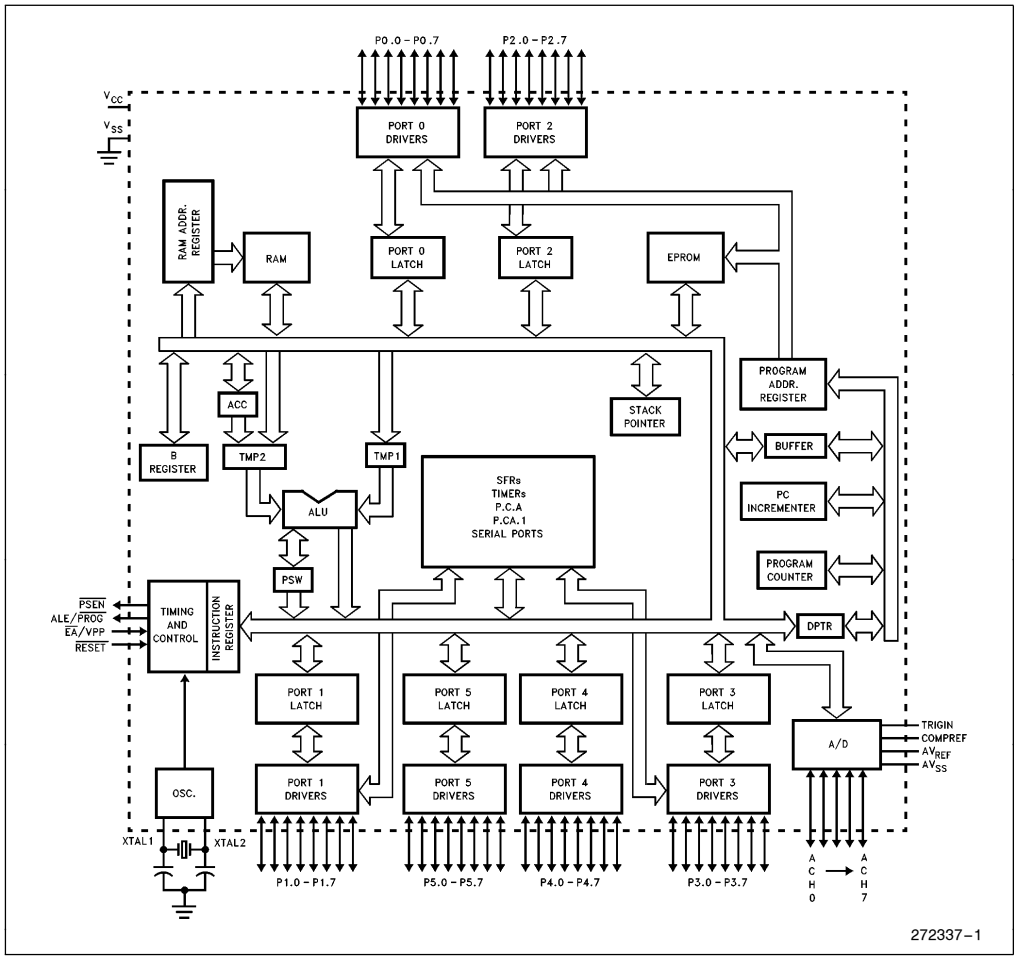


Figure 1. 8XC51GB Block Diagram

PROCESS INFORMATION

This device is manufactured on P629.0, a CHMOS III-E process. Additional process and reliability information is available in Intel's Components Quality and Reliability Handbook, Order No. 210997.

PACKAGES

Part	Prefix	Package Type
8XC51GB	N	68-Pin PLCC

PARALLEL I/O PORTS

The 8XC51GB contains six 8-bit parallel I/O ports. All six ports are bidirectional and consist of a latch, an output driver, and an input buffer. Many of the port pins have multiplexed I/O and control functions.

Port Pins as Outputs

Port 0 has open drain outputs when it is not serving as the external data bus. The internal pullup is active only when the pin is outputting a logic 1 during external memory access. An external pullup resistor is required on Port 0 when it is serving as an output port.

Ports 1, 2, 3, 4, and 5 have quasi-bidirectional outputs. A strong pullup provides a fast rise time when the pin is set to a logic 1. This pullup turns on for two oscillator periods to drive the pin high and then turns off. The pin is held high by a weak pullup.

Writing the P0, P1, P2, P3, P4 or P5 Special Function Register sets the corresponding port pins. All six port registers are bit addressable.

Port Pins as Inputs

The pins of all six ports are configured as inputs by writing a logic 1 to them. Since Port 0 is an open drain port, it provides a very high input impedance. Since pins of Port 1, 2, 3, 4 and 5 have weak pullups (which are always on), they source a small current when driven low externally. All ports except Port 0 have Schmitt trigger inputs.

Port States During Reset

Ports 0 and 3 reset asynchronously to a one and Ports 1, 2, 4, and 5 reset to a zero asynchronously.

PIN DESCRIPTIONS

The 8XC51GB will be packaged in the 68-lead PLCC package. Its pin assignment is shown in Figure 2.

V_{CC}: Supply Voltage.

V_{SS}: Circuit Ground.

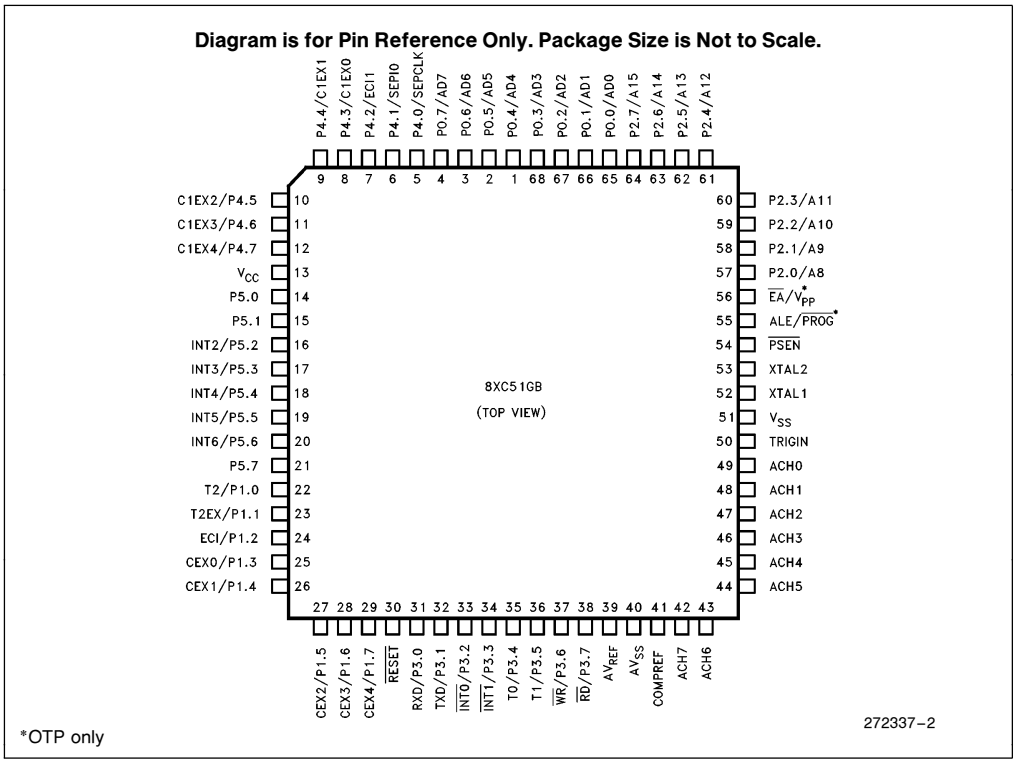


Figure 2. Pin Connections

ALTERNATE PORT FUNCTIONS

Ports 0, 1, 2, 3, 4 and 5 have alternate functions as well as their I/O function as described below.

Port Pin	Alternate Function
P0.0/ADO–P0.7/AD7	Multiplexed Address/Data for External Memory
P1.0/T2	Timer 2 External Clock Input/Clock-Out
P1.1/T2EX	Timer 2 Reload/Capture/Direction Control
P1.2/ECI	PCA External Clock Input
P1.3/CEXO–P1.7/CEX4	PCA Capture Input, Compare/PWM Output
P2.0/A8–P2.7/A15	High Byte of Address for External Memory
P3.0/RXD	Serial Port Input
P3.1/TXD	Serial Port Output
P3.2/$\overline{\text{INT0}}$	External Interrupt 0
P3.3/$\overline{\text{INT1}}$	External Interrupt 1
P3.4/T0	Timer 0 External Clock Input
P3.5/T1	Timer 1 External Clock Input
P3.6/$\overline{\text{WR}}$	Write Strobe for External Memory
P3.7/$\overline{\text{RD}}$	Read Strobe for External Memory
P4.0/SEPCLK	Clock Source for Serial Expansion Port
P4.1/SEPDAT	Data I/O for the Serial Expansion Port
P4.2/ECI1	PCA1 External Clock Input
P4.3/C1EX0–P4.7/C1EX4	PCA1 Capture Input, Compare/PWM Output
P5.2/INT2–P5.6/INT6	External Interrupt INT2–INT6

$\overline{\text{RST}}$: Reset input. A low on this pin for two machine cycles while the oscillator is running resets the device. The port pins will be driven to their reset condition when a voltage below V_{IL} max voltage is applied, whether the oscillator is running or not. An internal pullup resistor permits a power-on reset with only a capacitor connected to V_{SS}.

ALE/$\overline{\text{PROG}}$: Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin (ALE/$\overline{\text{PROG}}$) is also the program pulse input during programming of the 87C51GB.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With this bit set, the pin is weakly pulled high. However, the ALE disable feature will be suspended during a MOVX or MOVC instruction, idle mode, power down mode and ICE mode. The ALE disable feature will be terminated by reset. When the ALE disable feature is suspended or terminated, the ALE pin will no longer be pulled up weakly. Setting the ALE-disable bit has no affect if the microcontroller is in external execution mode.

Throughout the remainder of this data sheet, ALE will refer to the signal coming out of the ALE/$\overline{\text{PROG}}$ pin, and the pin will be referred to as the ALE/$\overline{\text{PROG}}$ pin.

$\overline{\text{PSEN}}$: Program Store Enable is the read strobe to external Program Memory.

When the 8XC51GB is executing code from external Program Memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external Data Memory.

$\overline{\text{EA}}$/V_{PP}: External Access enable. $\overline{\text{EA}}$ must be strapped to V_{SS} in order to enable the device to fetch code from external Program Memory locations 0000H to 1FFFH. Note, however, that if either of the Program Lock bits are programmed, $\overline{\text{EA}}$ will be internally latched on reset.

$\overline{\text{EA}}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12.75V programming supply voltage (V_{PP}) during programming (OTP only).

XTAL1: Input to the inverting oscillator amplifier.

XTAL2: Output from the inverting oscillator amplifier.

A/D CONVERTER

The 8XC51GB A/D converter has a resolution of 8 bits and an accuracy of ±1 LSB (±2 LSB for channels 0 and 1). The conversion time for a single channel is 20 μs at a clock frequency of 16 MHz with the sample and hold function included. Independent supply voltages are provided for the A/D. Also, the A/D operates both in Normal Mode or in Idle Mode.

The A/D has 8 analog input pins; ACH0 (A/D CHannel 0) . . . ACH7, 1 reference input pin; COMPREF (COMParison REFerence), 1 control input pin; TRIGIN (TRIGger IN), and 2 power pins; AVREF (Voltage REFerence) and analog ground (ANalog GrouND). In addition, the A/D has 8 conversion result registers; ADRES0 (A/D result for channel 0) . . . ADRES7, 1 comparison result register; ACMP (Analog Comparison), and 1 control register; ACON (A/D Control).

The control bit ACE (A/D Conversion Enable) in ACON controls whether the A/D is in operation or not. ACE = 0 idles the A/D. ACE = 1 enables A/D conversion. The control bit AIM (A/D Input mode) in ACON controls the mode of channel selection. AIM = 0 is the Scan Mode, and AIM = 1 is the Select Mode. The result registers ADRES4 . . . ADRES7 always contain the result of a conversion from the corresponding channels ACH4 . . . CH7. However, the result registers ADRES0 . . . ADRES3 depend on the mode selected. In the scan mode, ADRES0 . . . ADRES3 contain the values from ACH0 . . . ACH3. In the Select Mode, one of the four channels ACH0 . . . ACH3 is converted four times, and the four values are stored sequentially in locations ADRES0 . . . ADRES3. Its channel is selected by bits ACS1 and ACS0 (A/D Channel Select 1 and 0) in ACON.

PROGRAMMABLE COUNTER ARRAYS

The Programmable Counter Arrays (PCA–PCA1) are each made up of a Counter Module and five Register/Comparator Modules as shown below. The 16-bit output of the counter module is available to all five Register/Comparator Modules, providing one common timing reference. Each Register/Comparator Module is associated with a pin of Port 1 or Port 4 and is capable of performing input capture, output compare and pulse width modulation functions. The PCAs are exactly the same in function except for the addition of clock input sources on PCA1.

The PCA Counter and five Register/Comparator Modules each have a status bit in the CCON/C1CON Special Function Registers. These six status bits are set according to the selected modes of operation described below. The CCON/C1CON Register provides a convenient means to determine which of the six PCA/PCA1 interrupts has occurred. The EC Bit in the IE (Interrupt Enable) Special Function Register is a global interrupt enable for the PCA.

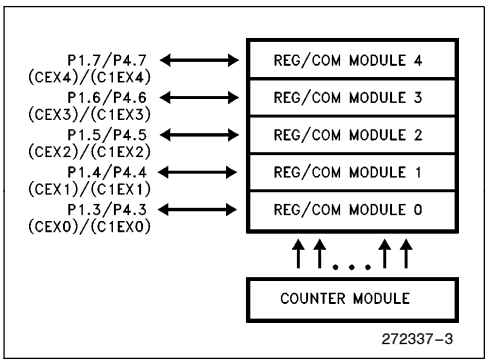
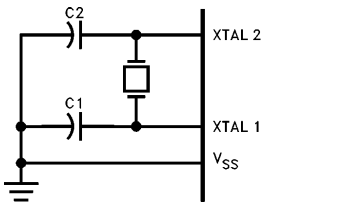


Figure 3. Programmable Counter Arrays

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 4. Either a quartz crystal or ceramic resonator may be used. More detailed information concerning the use of the on-chip oscillator is available in Application Note AP-155, ''Oscillators for Microcontrollers,'' Order No. 230659.

To drive the device from an external clock source, XTAL should be driven, while XTAL2 floats, as shown in Figure 5. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the data sheet must be observed.



C1, C2 = 30 pF ±10 pF for Crystals
For Ceramic Resonators contact resonator manufacturer.

Figure 4. Oscillator Connections

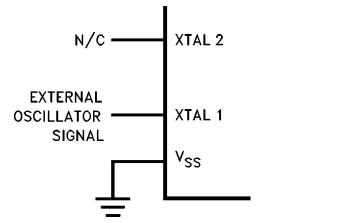


Figure 5. External Clock Drive Configuration

IDLE MODE

The user's software can invoke the Idle Mode. When the microcontroller is in this mode, power consumption is reduced. The Special Function Registers and the onboard RAM retain their values during idle, peripherals continue to operate, but the processor stops executing instructions. Idle Mode will be exited if the chip is reset or if an enabled interrupt occurs. The PCA timer/counter can optionally be left running or paused during Idle Mode. The Watchdog Timer continues to count in Idle Mode and must be serviced to prevent a device RESET while in Idle.

POWER DOWN MODE

To save even more power, a Power Down mode can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power Down mode is terminated.

On the 8XC51GB either a hardware reset or an external interrupt can cause an exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt does not redefine the SFR's or change the on-chip RAM. An external interrupt will modify the interrupt associated SFR's in the same way an interrupt will in all other modes. The interrupt must be enabled and configured as level sensitive. To properly terminate Power Down the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level. The reset or external interrupt must be held active long enough for the oscillator to restart and stabilize. The Oscillator Fail Detect must be disabled prior to entering Power Down.

DESIGN CONSIDERATIONS

- When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.
- As $\overline{\text{RESET}}$ rises, the 8XC51GB will remain in reset for up to 5 machine cycles (60 oscillator periods) after $\overline{\text{RESET}}$ reaches V_{IH1}.

Table 1. Status of the External Pins during Idle and Power Down

Mode	Program Memory	ALE	$\overline{\text{PSEN}}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

NOTE:
For more detailed information on the reduced power modes refer to current Embedded Microcontrollers and Processors Handbook Volume I (Order No. 270645), and Application Note AP-252 (Embedded Applications Handbook, Order No. 270648), ''Designing with the 80C51BH.''

ONCE MODE

The ONCE (''On-Circuit Emulation'') Mode facilitates testing and debugging of systems using the 8XC51GB without removing it from the circuit. The ONCE Mode is invoked by:

1) Pulling ALE low while the device is in reset and $\overline{PSEN}$ is high;
2) Holding ALE low as $\overline{RESET}$ is deactivated.

While the device is in ONCE Mode, the Port 0 pins float, and the other port pins and ALE and $\overline{PSEN}$ are weakly pulled high. The oscillator circuit remains active. While the 8XC51GB is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

Watchdog Timer (WDT)

The 8XC51GB contains a dedicated Watchdog Timer (WDT) to allow recovery from a software or hardware upset. The WDT consists of a 14-bit counter which is cleared on Reset, and subsequently incremented every machine cycle. While the oscillator is running, the WDT will be incrementing and cannot be disabled. The counter may be reset by writing 1EH and E1H in sequence to the WDTRST Special Function Register. If the counter is not reset before it reaches 3FFFH (16383D), the chip will be forced into a reset sequence by the WDT. This works out to 12.28 ms @ 16 MHz. WDTRST is a write only register. The WDT does not force the external reset pin low.

While in Idle mode the WDT continues to count. If the user does not wish to exit Idle with a reset, then the processor must be periodically ''woken up'' to service the WDT. In Power Down mode, the WDT stops counting and holds its current value.

Serial Expansion Port (SEP)

The Serial Expansion Port is a half-duplex synchronous serial interface with the following features:

Four Clock Frequencies— XTAL/12, 24, 48, 96.

Four Interface Modes— High/Low/Falling/Rising Edges.

Interrupt Driven.

Oscillator Fail Detect (OFD)

The Oscillator Fail Detect circuitry triggers a reset if the oscillator frequency is lower than the OFD trigger frequency. It can be disabled by software by writing E1H followed by 1EH to the OFDCON register. Before going into Power Down Mode, the OFD must be disabled or it will force the GB out of Power Down. The OFD has the following features.

OFD Trigger Frequency: Below 20 KHz, the 8XC51GB will be held in reset. Above 400 KHz, the 8XC51GB will not be held is reset.

Functions in Normal and Idle Modes.

Reactivated by Reset (or External Interrupt Zero/One Pins) after Software Disable.

8XC51GB EXPRESS

The Intel EXPRESS products are designed to meet the needs of those applications whose operating requirements exceed commercial standards.

With the commercial standard temperature range, operational characteristics are guaranteed over the temperature range of 0°C to +70°C. With the extended temperature range option, operational characteristics are guaranteed over the range of −40°C to +85°C. The 87C51GB EXPRESS is packaged in the 68-lead PLCC package. In order to designate a part as an EXPRESS part, a ''T'' is added as a prefix to the part number. TN87C51GB denotes an EXPRESS part in a PLCC package.

All AC and DC parameters in this data sheet apply to the EXPRESS devices.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature under Bias ....0°C to +70°C

Storage Temperature .....−65°C to +150°C

Voltage on EA/V_{PP} Pin to V_{SS} .....0V to +13.0V*

I_{OL} per I/O Pin .....15 mA

Voltage on Any Other Pin to V_{SS} .....−0.5V to +6.5V

Power Dissipation.....1.5W (Based on Package heat transfer limitations, not device power consumption)

*OTP only.

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature Under Bias			
	Commercial	0	+70	°C
	Express	−40	+85	°C
V_{CC}	Supply Voltage	4.0	6.0	V
f_{OSC}	Oscillator Frequency			
	8XC51GB	3.5	12	MHz
	8XC51GB-1	3.5	16	MHz

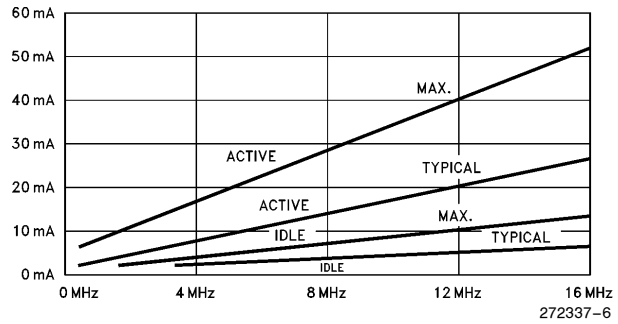
DC CHARACTERISTICS (Over Operating Conditions)

Symbol	Parameter	Min	Typ(1)	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage (except Port 2 and $\overline{EA}$)	−0.5		0.2 V_{CC} − 0.1	V	
V_{IL1}	Input Low Voltage (Port 2)	−0.5		0.2 V_{CC} − 0.3	V	
V_{IL2}	Input Low Voltage ($\overline{EA}$)	0		0.2 V_{CC} − 0.3	V	
V_{IH}	Input High Voltage (except XTAL1 and $\overline{RST}$)	0.2 V_{CC} + 0.9		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage (XTAL1, $\overline{RST}$)	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage (Ports 1, 2, 3, 4 and 5)			0.3	V	I_{OL} = 100 μA (2,3)
				0.45	V	I_{OL} = 1.6 mA (2,3)
				1.0	V	I_{OL} = 3.5 mA (2,3)
V_{OL1}	Output Low Voltage (Port 0, $\overline{PSEN}$, ALE)			0.3	V	I_{OL} = 200 μA (2,3)
				0.45	V	I_{OL} = 3.2 mA (2,3)
				1.0	V	I_{OL} = 7.0 mA (2,3)

DC CHARACTERISTICS (Over Operating Conditions) (Continued)

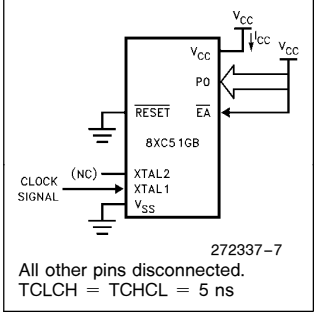
Symbol	Parameter	Min	Typ(1)	Max	Unit	Test Conditions
V_{OH}	Output High Voltage (Ports 1, 2, 3, 4 and 5, ALE, $\overline{PSEN}$)	V_{CC} − 0.3			V	I_{OH} = −10 μA (4)
		V_{CC} − 0.7			V	I_{OH} = −30 μA (4)
		V_{CC} − 1.5			V	I_{OH} = −60 μA (4)
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	V_{CC} − 0.3			V	I_{OH} = −200 μA
		V_{CC} − 0.7			V	I_{OH} = −3.2 mA
		V_{CC} − 1.5			V	I_{OH} = −7.0 mA
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3, 4, 5)			−50	μA	V_{IN} = 0.45V
I_{TL}	Logical 1-to-0 Transition Current (Ports 1, 2, 3, 4, 5)			−650	μA	V_{IN} = 2.0V
I_{LI}	Input Leakage Current (Port 0)			±10	μA	0.45 < V_{IN} < V_{CC}
RRST	RST Pullup Resistor	50		300	kΩ	
C_{IO}	Pin Capacitance		10		pF	Freq = 1 MHz T_A = 25°C
I_{PD}	Power Down Current			50	μA	(5)
I_{DL}	Idle Mode Current			18	mA	(5)
I_{CC}	Operating Current @16 MHz			50	mA	(5)
I_{REF}	A/D Converter Reference Current			5	mA	

NOTES:
1. Typical values are obtained using V_{CC} = 5.0V, T_A = 25°C, and are not guaranteed.
2. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per Port Pin: 10 mA
   Maximum I_{OL} per 8-Bit Port—
   Port 0: 26 mA
   Ports 1–5: 15 mA
   Maximum Total I_{OL} for All Outputs Pins: 101 mA
   If I_{OL} exceeds the test conditions, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
3. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses above 0.4V on the low level outputs of ALE and Ports 1, 2 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from 1 to 0. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8V. It may be desirable to qualify ALE or other signals with a Schmitt Trigger, or CMOS-level input logic.
4. Capacitive loading on Ports 0 and 2 cause the V_{OH} on ALE and $\overline{PSEN}$ to drop below the 0.9 V_{CC} specification when the address lines are stabilizing.
5. See Figures 6–10 for test conditions. Minimum V_{CC} for Power Down is 2V.



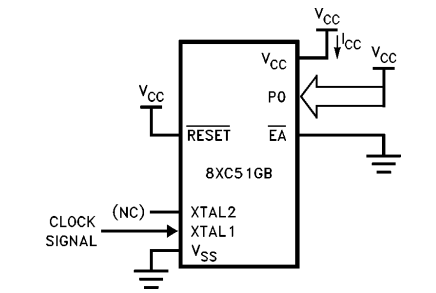
I_{CC} Max at other frequencies is given by:
Active Mode
I_{CC} Max = (Osc Freq × 3) + 4
Idle Mode
I_{CC} Max = (Osc Freq × 0.5) + 4
Where Osc Freq is in MHz, I_{CC} is in mA. $T_{CLCH} = T_{CHCL} = 5$ ns

Figure 6. I_{CC} vs Frequency



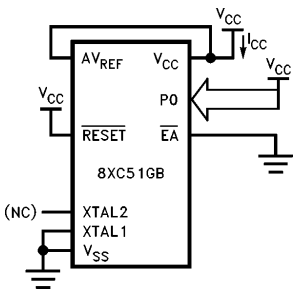
All other pins disconnected.
TCLCH = TCHCL = 5 ns

Figure 7. I_{CC} Test Condition, Active Mode



All other pins disconnected.
TCLCH = TCHCL = 5 ns

Figure 8. I_{CC} Test Condition Idle Mode



All other pins disconnected.

Figure 9. I_{CC} Test Condition, Power Down Mode V_{CC} = 2.0V to 5.5V

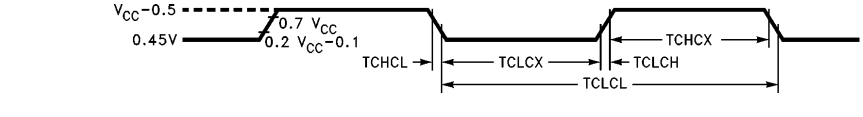


Figure 10. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes. TCLCH = TCHCL = 5 ns.

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a "T" (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for:

A: Address
C: Clock
D: Input Data
H: Logic Level HIGH
I: Instruction (Program Memory Contents)
L: Logic Level LOW, or ALE
P: $\overline{\text{PSEN}}$
Q: Output Data
R: $\overline{\text{RD}}$ Signal
T: Time
V: Valid
W: $\overline{\text{WR}}$ Signal
X: No Longer a Valid Logic Level
Z: Float

For Example:

TAVLL = Time from Address Valid to ALE Low
TLLPL = Time from ALE Low to $\overline{\text{PSEN}}$ Low

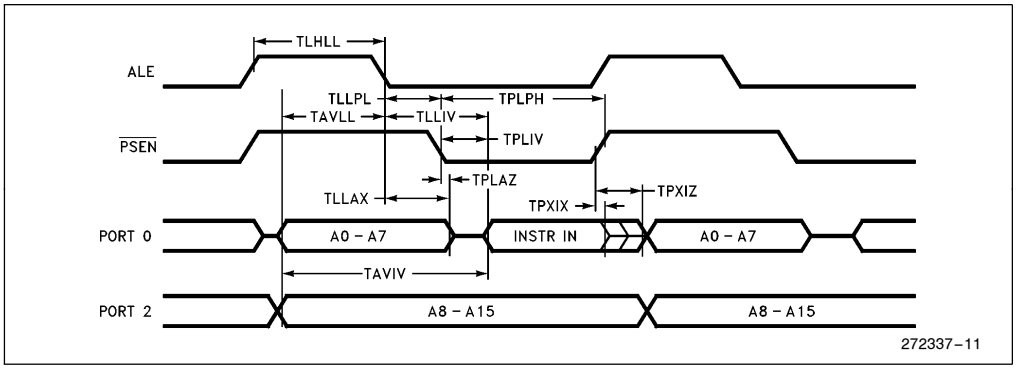
AC SPECIFICATIONS

Over Operating Conditions, Load Capacitance on Port 0, ALE, and $\overline{\text{PSEN}}$ = 100 pF, Load Capacitance on all other outputs = 80 pF

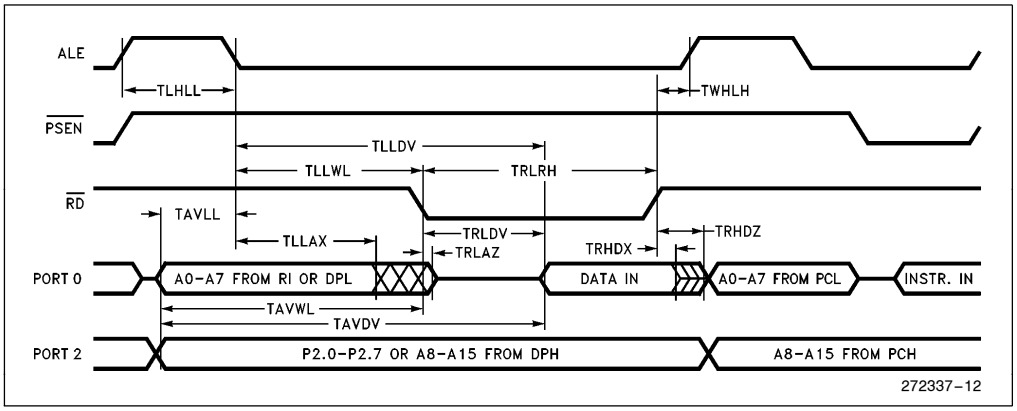
EXTERNAL PROGRAM AND DATA MEMORY CHARACTERISTICS

Symbol	Parameter	12 MHz Osc.		Variable Osc.		Units
		Min	Max	Min	Max	
1/TCLCL	Osc. Freq.			3.5	16	MHz
TLHLL	ALE Pulse Width	127		2TCLCL − 40		ns
TAVLL	ADDR Valid to ALE Low	43		TCLCL − 40		ns
TLLAX	ADDR Hold after ALE Low	53		TCLCL − 30		ns
TLLIV	ALE Low to Valid Inst. IN		234		4TCLCL − 100	ns
TLLPL	ALE LOW to $\overline{\text{PSEN}}$ LOW	53		TCLCL − 30		ns
TPLPH	$\overline{\text{PSEN}}$ Pulse Width	205		3TCLCL − 45		ns
TPLIV	$\overline{\text{PSEN}}$ Low to Valid Instr In		145		3TCLCL − 105	ns
TPXIX	Input Instr. Hold after $\overline{\text{PSEN}}$	0		0		ns
TPXIZ	Input Instr. Float after $\overline{\text{PSEN}}$		59		TCLCL − 25	ns
TAVIV	ADDR to Valid Instr. In		312		5TCLCL − 105	ns
TPLAZ	$\overline{\text{PSEN}}$ Low to ADDR Float		10		10	ns
TRLRH	$\overline{\text{RD}}$ Pulse Width	400		6TCLCL − 100		ns
TWLWH	$\overline{\text{WR}}$ Pulse Width	400		6TCLCL − 100		ns
TRLDV	$\overline{\text{RD}}$ Low to Valid Data In		252		5TCLCL − 165	ns
TRHDX	Data Hold after $\overline{\text{RD}}$	0		0		ns
TRHDZ	Data Float after $\overline{\text{RD}}$		107		2TCLCL − 60	ns
TLLDV	ALE Low to Valid Data In		517		8TCLCL − 150	ns
TAVDV	ADDR to Valid Data In		585		9TCLCL − 165	ns
TLLWL	ALE Low to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ Low	200	300	3TCLCL − 50	3TCLCL + 50	ns
TAVWL	ADDR Valid to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ Low	203		4TCLCL − 130		ns
TQVWX	Data Valid to $\overline{\text{WR}}$ Transition	33		TCLCL − 50		ns
TWHQX	Data Hold after $\overline{\text{WR}}$	33		TCLCL − 50		ns
TQVWH	Data Valid to $\overline{\text{WR}}$ High	433		7 TCLCL − 150		ns
TRLAZ	$\overline{\text{RD}}$ Low to Addr Float		0		0	ns
TWHLH	$\overline{\text{RD}}$ or $\overline{\text{WR}}$ High to ALE High	43	123	TCLCL − 40	TCLCL + 40	ns

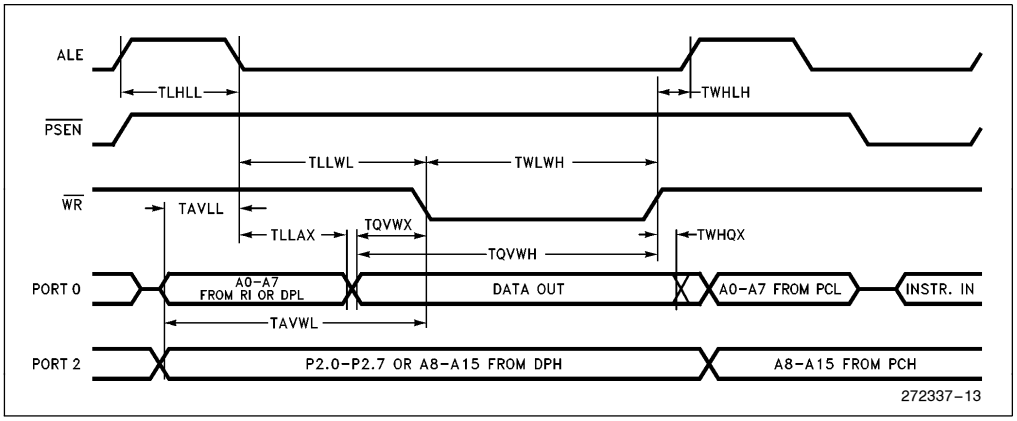
EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE



EXTERNAL DATA MEMORY WRITE CYCLE

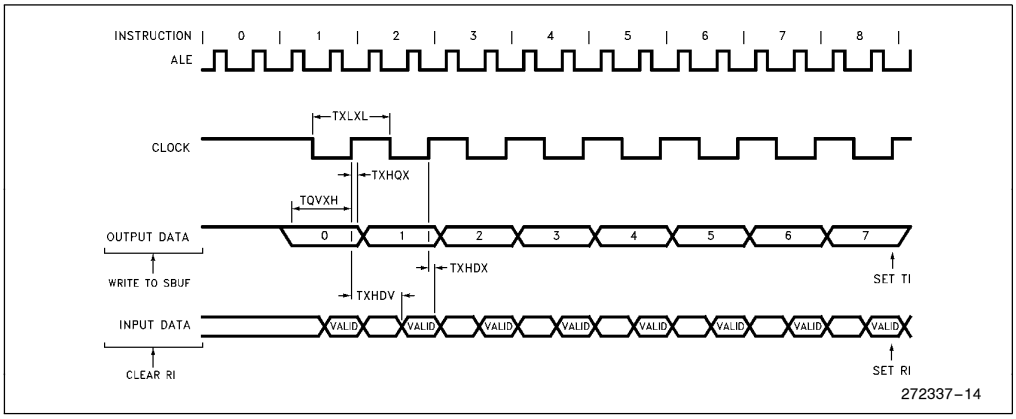


SERIAL PORT TIMING—SHIFT REGISTER MODE

Test Conditions: Over Operating Conditions, Load Capacitance = 80 pF

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	1		12TCLCL		μs
TQVXH	Output Data Setup to Clock Rising Edge	700		10TCLCL − 133		ns
TXHQX	Output Data Hold after Clock Rising Edge	50		2TCLCL − 117		ns
TXHDX	Input Data Hold after Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		700		10TCLCL − 133	ns

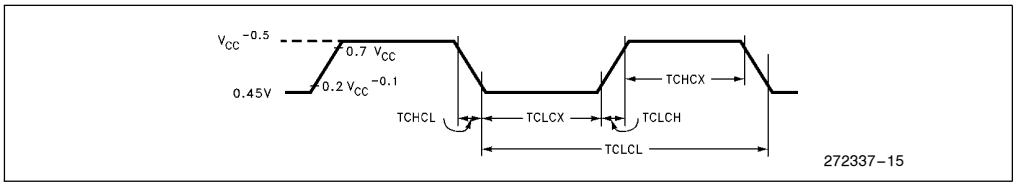
SHIFT REGISTER MODE TIMING WAVEFORMS



EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency	3.5	16	MHz
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

EXTERNAL CLOCK DRIVE WAVEFORM

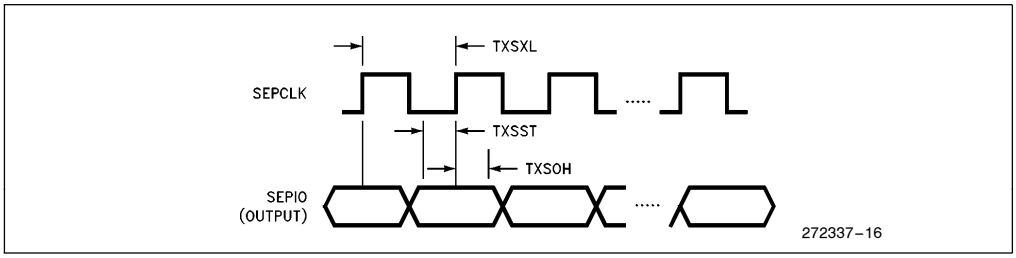


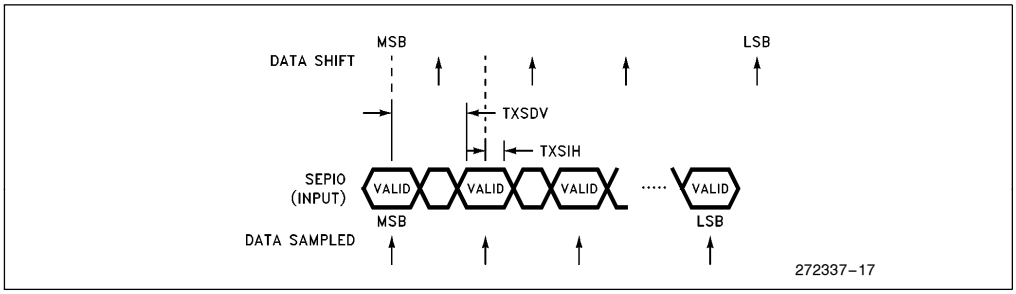
SEP AC TIMING SPECIFICATIONS

Test Conditions: Over Operating Conditions, Load Capacitance = 80 pF

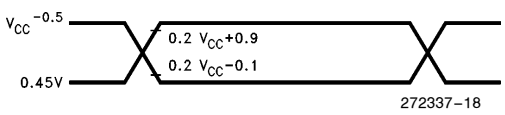
Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
TXSXL	SEPCLK Cycle Time	1		12 TCLCL		μs
TXSST	Output Data Setup to SEPCLK	435		6 TCLCL − 65		ns
TXSOH	Output Data Hold after SEPCLK	445		6 TCLCL − 55		ns
TXSIH	Input Data Hold after SEPCLK Sampling Edge	210		2 TCLCL + 43		ns
TXSDV	Input Data Valid to SEPCLK Sampling Edge		947		12 TCLCL − 53	ns

SEP Waveform (SEPS1 = 0; SEPS0 = 0; CLKPOL = 0; CLKPH = 0)



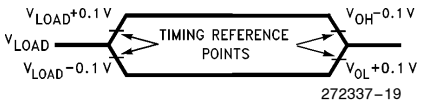


AC TESTING INPUT, OUTPUT WAVEFORMS



AC inputs during testing are driven at $V_{CC}-0.5V$ for a Logic "1" and 0.5V for a Logic "0". Timing measurements are made at V_{IH} for a Logic "1" and V_{OL} max for a Logic "0".

FLOAT WAVEFORMS



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.

A TO D CHARACTERISTICS

The absolute conversion accuracy is dependent on the accuracy of AV_{REF}. The specifications given below assume adherence to the Operating Conditions section of this data sheet. Testing is done at $AV_{REF} = 5.12V$, and $V_{CC} = 5.0V$.

OPERATING CONDITIONS

V_{CC} . . . . . 4.0V to 6.0V
AV_{REF} . . . . . 4.5V to 5.5V
V_{SS}, AV_{SS} 0V
ACH0–7 . . . . . AV_{SS} to V_{REF}
T_A . . . . . 0°C to +70°C Ambient
FOSC (STD Version) . . . . . 3.5 MHz to 12 MHz
FOSC (-1 Version) . . . . . 3.5 MHz to 16 MHz

A/D CONVERTER SPECIFICATIONS $T_A = 0°C$ to $+70°C$

Parameter	Min	Typ*	Max	Units**	Notes
Resolution	256 8		256 8	Levels Bits	
Absolute Error (Ch 2–7)	0		±1	LSB	
Absolute Error (Ch 0 and 1)	0		±2	LSB	
Full Scale Error		±1		LSB	
Zero Offset Error		±1		LSB	
Non-Linearity	0		±1	LSB	
Differential Non-Linearity	0		±1	LSB	
Channel-to-Channel Matching	0		±1	LSB	
Repeatability		±0.25		LSB	

A/D CONVERTER SPECIFICATIONS $T_A = 0°C$ to $+70°C$ (Continued)

Parameter	Min	Typ*	Max	Units**	Notes
Temperature Coefficients:					
Offset		0.003		LSB/°C	
Full Scale		0.003		LSB/°C	
Differential Non-Linearity		0.003		LSB/°C	
Input Capacitance		3		pF	
Off Isolation	−60			dB	(8, 9)
Feedthrough		−60		dB	(8)
V_{CC} Power Supply Rejection		−60		dB	(8)
Input Resistance to Sample-and-Hold Capacitor	750		1.2K	Ω	
DC Input Leakage	0		3.0	μA	

NOTES:
*These values are expected for most parts at 25°C
**AN "LSB" as used here, has a value of approximately 20 mV.
8. DC to 100 KHz
9. Multiplexer Break-Before-Make Guaranteed.
10. There is no indication when a single A/D conversion is complete. Please refer to the 8XC51GB Hardware Description on how to read a single A/D conversion.
11. $T_{CY} = 12$ TCLCL

A/D Conversion Time		Notes
Per Channel	26 T_{CY}	(10, 11)
8 Conversions	208 T_{CY}	(11)

PROGRAMMING THE OTP

The part must be running with a 4 MHz to 6 MHz oscillator. The address of a location to be programmed is applied to address lines while the code byte to be programmed in that location is applied to data lines. Control and program signals must be held at the levels indicated in Table 2. Normally $\overline{EA}/V_{PP}$ is held at logic high until just before ALE/$\overline{PROG}$ is to be pulsed. The $\overline{EA}/V_{PP}$ is raised to V_{PP}, ALE/$\overline{PROG}$ is pulsed low and then $\overline{EA}/V_{PP}$ is returned to a high (also refer to timing diagrams).

NOTE:
Exceeding the V_{PP} maximum for any amount of time could damage the device permanently. The V_{PP} source must be well regulated and free of glitches.

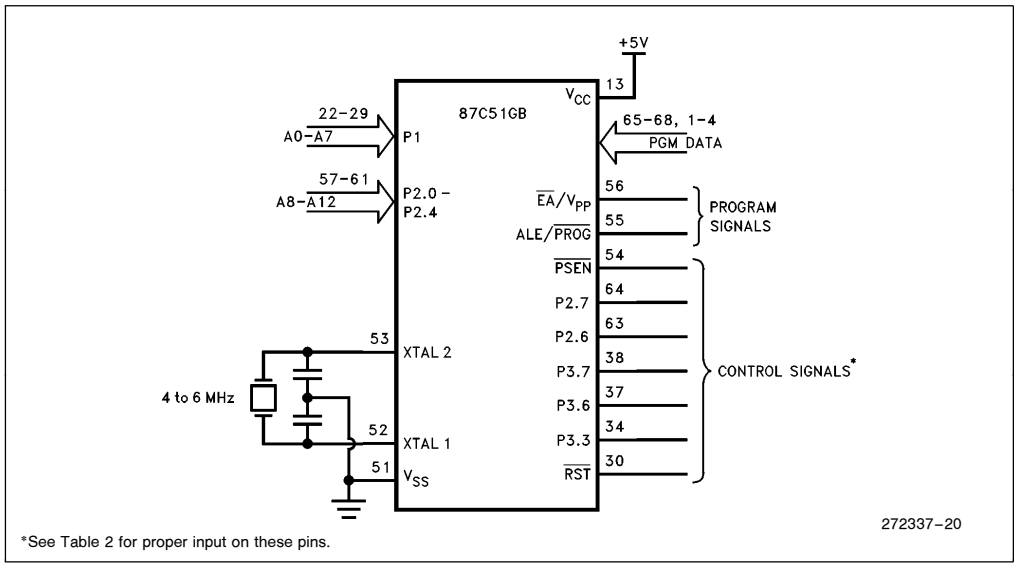
DEFINITION OF TERMS

ADDRESS LINES: P1.0–P1.7, P2.0–P2.4, respectively for A0–A12.

DATA LINES: P0.0–P0.7 for D0–D7.

CONTROL SIGNALS: $\overline{RST}$, $\overline{PSEN}$, P2.6, P2.7, P3.3, P3.6, P3.7

PROGRAM SIGNALS: ALE/$\overline{PROG}$, $\overline{EA}/V_{PP}$



*See Table 2 for proper input on these pins.

Figure 11. Programming the OTP

Table 2. OTP Programming Modes

Mode		$\overline{RST}$	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code Data		L	L	⎍	12.75V	L	H	H	H	H
Verify Code Data		L	L	H	H	L	L	L	H	H
Program Encryption Array Address 0–3FH		L	L	⎍	12.75V	L	H	H	L	H
Program Lock Bits	Bit 1	L	L	⎍	12.75V	H	H	H	H	H
	Bit 2	L	L	⎍	12.75V	H	H	H	L	L
	Bit 3	L	L	⎍	12.75V	H	L	H	H	L
Read Signature Byte		L	H	H	H	L	L	L	L	L

PROGRAMMING ALGORITHM

Refer to Table 2 and Figures 11 and 12 for address, data, and control signals set up. To program the 87C51GB the following sequence must be exercised.

1. Input the valid address on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ from V_{CC} to 12.75V $\pm$0.25V.
5. Pulse ALE/$\overline{PROG}$ 5 times for the OTP array, and 25 times for the encryption table and the lock bits.

Repeat 1 through 5 changing the address and data for the entire array or until the end of the object file is reached.

PROGRAM VERIFY

Program verify may be done after each byte that is programmed, or after a block of bytes that is programmed. In either case a complete verify of the array will ensure that it has been programmed correctly.

The lock bits cannot be directly verified. Verification of the lock bits is done by observing that their features are enabled. Refer to the Program Lock section in this data sheet.

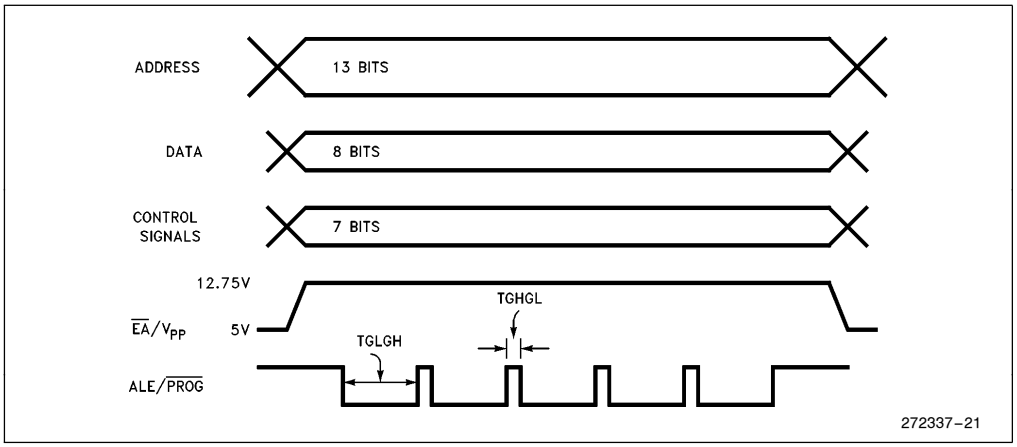


Figure 12. Programming Signal's Waveforms

ROM and EPROM Lock System

The 87C51GB and the 83C51GB program lock systems, when programmed, protect the on-board program against software piracy.

The 83C51GB has a one-level program lock system and a 64-byte encryption table. See line 2 of Table 3. If program protection is desired, the user submits the encryption table with their code, and both the lock bit and encryption array are programmed by the factory. The encryption array is not available without the lock bit. For the lock bit to be programmed, the user must submit an encryption table.

The 87C51GB has a 3-level program lock system and a 64-byte encryption array. Since this is an EPROM device, all locations are user programmable. See Table 3.

Encryption Array

Within the programmable array are 64 bytes of Encryption Array that are initially unprogrammed (all 1's). Every time that a byte is addressed during a verify, 5 address lines are used to select a byte of the Encryption Array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an Encryption Verify byte. The algorithm, with the array in the unprogrammed state (all 1's), will return the code in its original, unmodified form. For programming the Encryption Array, refer to Table 2.

When using the encryption array feature, one important factor needs to be considered. If a code byte has the value 0FFH, verification of the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the contents of the encryption array. For this reason it is strongly recommended that all unused code bytes be programmed with some value other than 0FFH, and not all of them the same value. This practice will ensure the maximum possible program protection.

Program Lock Bits

The 87C51GB has 3 programmable lock bits that when programmed according to Table 3 will provide different levels of protection for the on-chip code **and data**. The 83C51GB has 1 program lock bit. See line 2 of Table 3.

Reading the Signature Bytes

The 8XC51GB has 3 signature bytes in locations 30H, 31H, and 60H. To read these bytes follow the procedure for verify, but activate the control lines provided in Table 2 for Read Signature Byte.

Location	Contents	
	87C51GB	83C51GB
30H	89H	89H
31H	58H	58H
60H	EBH	EBH/6BH

Table 3. Program Lock Bits and the Features

	*Program Lock Bits			Protection Type
	LB1	LB2	LB3	
1	U	U	U	No Program Lock features enabled. (Code verify will still be encrypted by the Encryption Array if programmed).
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on Reset, and further programming of the EPROM is disabled.
3	P	P	U	Same as 2, also verify is disabled.
4	P	P	P	Same as 3, also external execution is disabled.

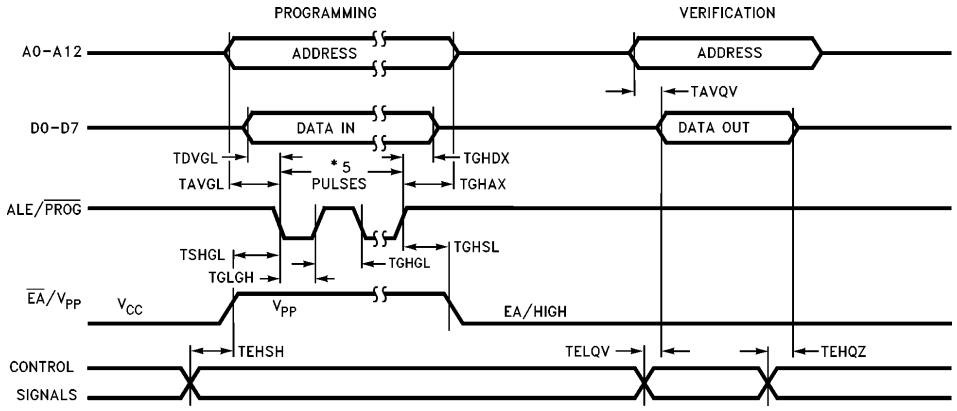
*Any other combination of lock bits is not defined.

OTP PROGRAMMING AND VERIFICATION CHARACTERISTICS

(T_A = 21°C to 27°C; V_{CC} = 5V ± 20%; V_{SS} = 0V)

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13.0	V
I_{PP}	Programming Supply Current		75	mA
1/TCLCL	Oscillator Frequency	4	6	MHz
TAVGL	Address Setup to $\overline{PROG}$ Low	48TCLCL		
TGHAX	Address Hold after $\overline{PROG}$	48TCLCL		
TDVGL	Data Setup to $\overline{PROG}$ Low	48TCLCL		
TGHDX	Data Hold after $\overline{PROG}$	48TCLCL		
TEHSH	(Enable) High to V_{PP}	48TCLCL		
TSHGL	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
TGHSL	V_{PP} Hold after $\overline{PROG}$	10		µs
TGLGH	$\overline{PROG}$ Width	90	110	µs
TAVQV	Address to Data Valid		48TCLCL	
TELQV	ENABLE Low to Data Valid		48TCLCL	
TEHQZ	Data Float after ENABLE	0	48TCLCL	
TGHGL	$\overline{PROG}$ High to $\overline{PROG}$ Low	10		µs

PROGRAMMING AND VERIFICATION WAVEFORMS



*25 Pulses for Encryption Table and Lock Bits.

A/D Glossary of Terms

Absolute Error—The maximum difference between corresponding actual and ideal code transitions. Absolute Error accounts for all deviations of an actual converter from an ideal converter.

Actual Characteristic—The characteristic of an actual converter. The characteristic of a given converter may vary over temperature, supply voltage, and frequency conditions. An actual characteristic rarely has ideal first and last transition locations or ideal code widths. It may even vary over multiple conversions under the same conditions.

Break-Before-Make—The property of a multiplexer which guarantees that a previously selected channel will be deselected before a new channel is selected (e.g., the converter will not short inputs together).

Channel-to-Channel Matching—The difference between corresponding code transitions of actual characteristics taken from different channels under the same temperature, voltage and frequency conditions.

Characteristic—A graph of input voltage versus the resultant output code for an A/D converter. It describes the transfer function of the A/D converter.

Code—The digital value output by the converter.

Code Center—The voltage corresponding to the midpoint between two adjacent code transitions.

Code Transition—The point at which the converter changes from an output code of Q, to a code of Q + 1. The input voltage corresponding to a code transition is defined to be that voltage which is equally likely to produce either of two adjacent codes.

Code Width—The voltage corresponding to the difference between two adjacent code transitions.

Crosstalk—See ''Off-Isolation''.

DC Input Leakage—Leakage current to ground from an analog input pin.

Differential Non-Linearity—The difference between the ideal and actual code widths of the terminal based characteristic.

Feedthrough—Attenuation of a voltage applied on the selected channel of the A/D Converter after the sample window closes.

Full Scale Error—The difference between the expected and actual input voltage corresponding to the full scale code transition.

Ideal Characteristic—A characteristic with its first code transition at V_{IN} = 0.5 LSB, its last code transition at V_{IN} = (V_{REF} − 1.5 LSB) and all code widths equal to one LSB.

Input Resistance—The effective series resistance from the analog input pin to the sample capacitor.

LSB—Least Significant Bit—The voltage corresponding to the full scale voltage divided by 2^n, where n is the number of bits of resolution of the converter. For an 8-bit converter with a reference voltage of 5.12V, one LSB is 20 mV. Note that this is different than digital LSBs since an uncertainty of two LSBs, when referring to an A/D converter, equals 40 mV. (This has been confused with an uncertainty of two digital bits, which would mean four counts, or 80 mV).

Monotonic—The property of successive approximation converters which guarantees that increasing input voltages produce adjacent codes of increasing value, and that decreasing input voltages produce adjacent codes of decreasing value.

No Missed Codes—For each and every output code, there exists a unique input voltage range which produces that code only.

Non-Linearity—The maximum deviation of code transitions of the terminal based characteristic from the corresponding code transitions of the ideal characteristic.

Off-Isolation—Attenuation of a voltage applied on a deselected channel of the A/D converter. (Also referred to as Crosstalk.)

Repeatability—The difference between corresponding code transitions from different actual characteristics taken from the same converter on the same channel at the same temperature, voltage and frequency conditions.

Resolution—The number of input voltage levels that the converter can unambiguously distinguish between. Also defines the number of useful bits of information which the converter can return.

Sample Delay—The delay from receiving the start conversion signal to when the sample window opens.

Sample Delay Uncertainty—The variation in the sample delay.

Sample Time—The time that the sample window is open.

Sample Time Uncertainty—The variation in the sample time.

Sample Window—Begins when the sample capacitor is attached to a selected channel and ends when the sample capacitor is disconnected from the selected channel.

Successive Approximation—An A/D conversion method which uses a binary search to arrive at the best digital representation of an analog input.

Temperature Coefficients—Change in the stated variable per degree centrigrade temperature change. Temperature coefficients are added to the typical values of a specification to see the effect of temperature drift.

Terminal Based Characteristic—An actual characteristic which has been rotated and translated to remove zero offset and full scale error.

V_{CC} Rejection—Attenuation of noise on the V_{CC} line to the A/D converter.

Zero Offset—The difference between the expected and actual input voltage corresponding to the first code transition.

DATA SHEET REVISION SUMMARY

The following differences exist between this datasheet and the previous version (270869-003):

1. Merged 87C51GB Express (270889-001).
2. New order number 272337-001.

The following differences exist between the 270869-003 data sheet and the previous version (270869-002):

1. Changed data sheet status from ''Advance Information'' to ''Preliminary'' and updated associated notices.
2. Added 83C51GB throughout.
3. Added Package and Process Information.
4. Clarified ± 2 LSB accuracy for channels 0 and 1 in A/D Converter Section.
5. Added ''ROM and EPROM Lock System'' section and added 83C51GB to ''Program Lock Bits'' section.
6. Modified Signature Bytes Table.

The following differences exist between the 270869-002 data sheet and the previous version (270869-001):

1. Changed data sheet status from ''Product Preview'' to ''Advance Information'' and updated associated notices.
2. Asynchronous port reset was added to $\overline{\text{RESET}}$ pin description.
3. ALE disable paragraph was added to ALE pin description.
4. C_1, C_2 guidelines clarified in Figure 4.
5. Operating Conditions heading was added.
6. Maximum I_{OL} per I/O pin was added to Absolute Maximum Ratings.
7. VT_+, VT_-, V_{HYS}, V_{OL2}, and V_{TL} removed.
8. V_{OL} value for ALE included with V_{OL1}.
9. V_{IL1} and V_{IL2} added.
10. RRST minimum changed from 40K to 50K. RRST maximum changed from 225K to 300K.
11. I_{PD} maximum changed from 200 μA to 50 μA.
12. I_{DL} maximum changed from 15 mA to 18 mA.
13. Typical values for I_{PD}, I_{DL}, I_{CC}, and I_{REF} removed.
14. Note 3 (page 9) was reworded.
15. SEP AC Timings added.
16. A/D Absolute Error for Channels 0 and 1 changed to ± 2 LSB.
17. T_{CY} clarified.
18. Encryption array paragraph was added.
19. Corrected pin numbers on Figure 11 to reflect PLCC package.