DATA SHEET

TDA1592
PLL stereo decoder and noise blanker

Preliminary specification
Supersedes data of June 1993
File under Integrated Circuits, IC01

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Philips
Semiconductors

PHILIPS

PLL stereo decoder and noise blanker TDA1592

FEATURES

- Adjustment-free voltage controlled PLL oscillator for ceramic resonator (f = 456 kHz)
- Pilot signal dependent mono/stereo switching
- Analog control of mono/stereo change over [stereo blend, Stereo Noise Controller (SNC)]
- Adjacent channel noise suppression (114 kHz)
- Pilot canceller
- Analog control of de-emphasis; High Cut Control (HCC)
- Reduced and controlled de-emphasis for AM operation (pin 7 to GND)
- Applicable as source selector for AM/FM/cassette switching
- Soft mute for silent tuning
- Separate interference noise detector
- Integrated input low-pass filter for delayed noise blanking
- Noise blanking at MPX-demodulator outputs.

GENERAL DESCRIPTION

The TDA1592 is a monolithic bipolar integrated circuit providing the stereo decoder function and noise blanking for FM car radio applications.

The device operates in a power supply range of 7.5 to 12 V.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 5)	7.5	10	12	V
I_P	supply current	–	15	20	mA
$V_{o(rms)}$	audio output signal (RMS value)	800	900	1000	mV
THD	total harmonic distortion	–	0.1	0.3	%
S/N	signal-to-noise ratio	–	82	–	dB
α_{cs}	channel separation	30	40	–	dB
V_{trigg}	interference voltage trigger level	–	10	–	mV

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1592	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
TDA1592T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

BLOCK DIAGRAM

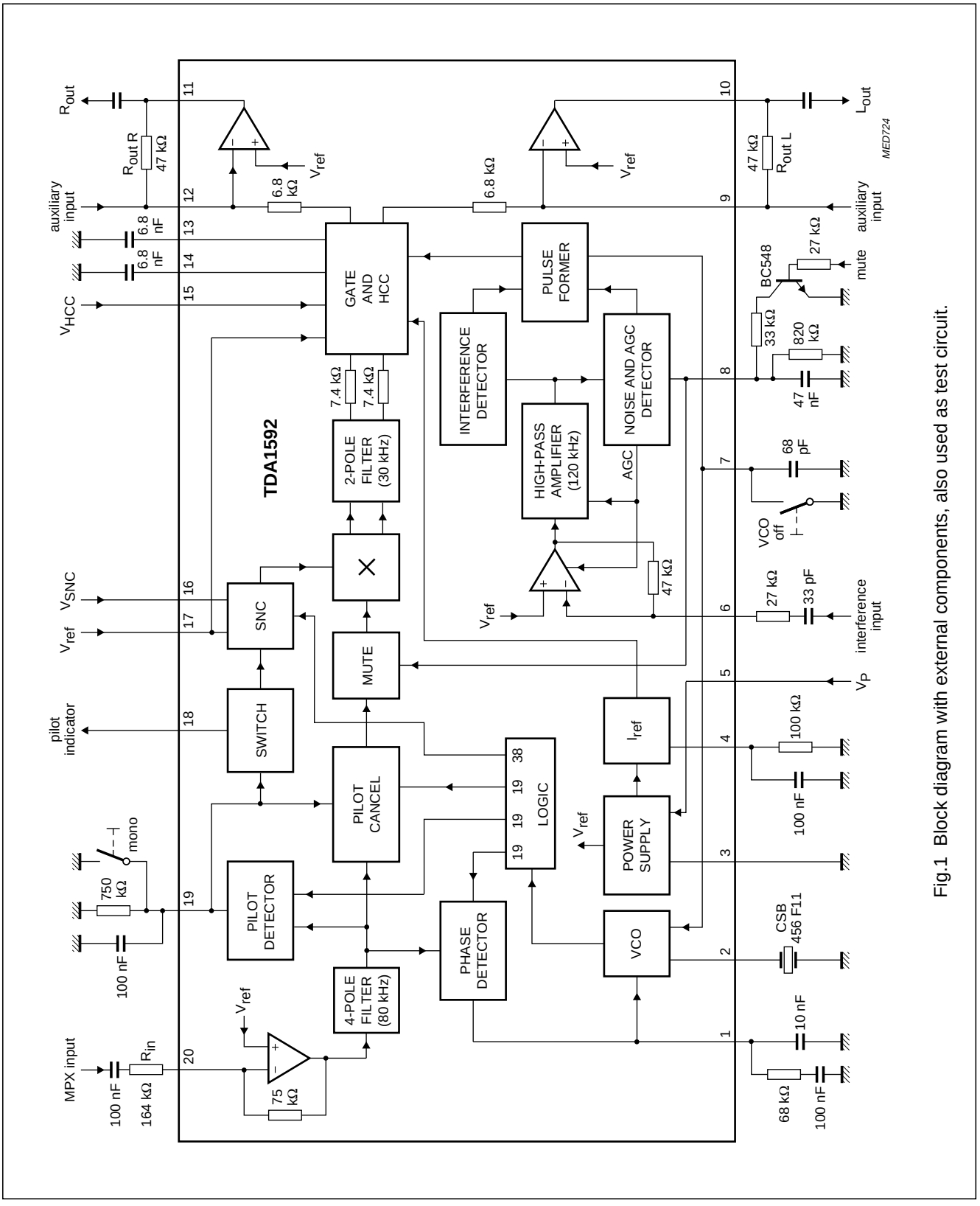


Fig.1 Block diagram with external components, also used as test circuit.

PINNING

SYMBOL	PIN	DESCRIPTION
PLL	1	phase locked loop filter
OSC	2	oscillator input/output pin for ceramic resonator
GND	3	ground (0 V)
I_{ref}	4	reference current
V_P	5	supply voltage (+10 V)
INFI	6	interference signal input
PUFO	7	pulse former time constant; VCO **off**
NDET	8	noise detector time constant; mute **on**
FB-L	9	AF feedback input for left audio signal
V_{oL}	10	AF output signal left
V_{oR}	11	AF output signal right
FB-R	12	AF feedback input for right audio signal
C_{DEEL}	13	de-emphasis capacitor for left channel
C_{DEER}	14	de-emphasis capacitor for right channel
HCC	15	HCC input for de-emphasis control
SNC	16	stereo blend input
V_{ref}	17	externally applied reference voltage of 1 to 5 V
IDENT	18	identification output (HIGH = pilot existing; stereo)
PILOT	19	pilot detector level (forced mono input)
$V_{i\ MPX}$	20	MPX input signal from IF demodulator

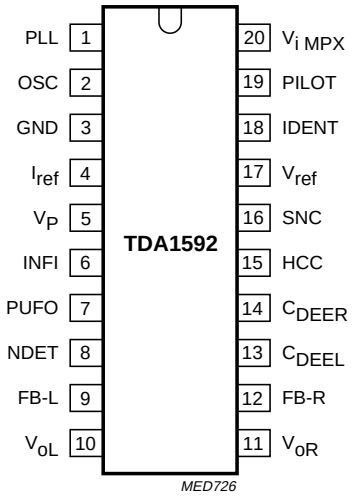


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The MPX input of the TDA1592 (pin 20) is the null-node of an operational amplifier with internal feedback resistor. Adapting the stereo decoder input to the level of the FM demodulator output is realized by the value of input resistor R_{in} (see Fig.3). The total gain of the stereo decoder is applicable by varying the feedback resistors R_{out} (pins 9, 10, 11 and 12) of the output operational amplifiers (see Fig.4).

The input amplifier is followed by an integrated 4th order Bessel low-pass filter with a cut-off frequency of 80 kHz. It provides necessary signal delay for noise blanking and damping of high frequency interferences at the stereo decoder input.

The soft mute facility (pin 8) provides silent tuning for RDS processing. The mute time constant may be adjusted from pin 8. In mute position and the VCO switched **off** (pin 7), the output amplifiers can be used for cassette playback, AM stereo purpose or other signal sources.

The voltage to current converted MPX signal is fed to phase detector, pilot detector and pilot canceller circuits. The oscillator is alignment-free with an external ceramic resonator at 456 kHz as reference (pin 2). The required 19 kHz and 38 kHz signals are generated by division of the oscillator output signal in a logical circuit. For regeneration of the 38 kHz subcarrier, a PLL is used. The 19 kHz quadrature phase signal is fed to the 19 kHz phase detector, where it is compared with the incoming pilot tone. The DC output signal of the phase detector (pin 1) controls the oscillator (PLL).

The pilot presence detector is driven by internally generated in-phase 19 kHz. Its pilot-dependent DC output voltage (pin 19) is fed to a threshold switch, which activates the pilot indicator logic output (pin 18) and turns the stereo decoder to stereo operation. The same DC voltage is used to control the amplitude of an anti-phase internally generated 19 kHz signal. In the pilot canceller, the pilot tone is compensated by this anti-phase 19 kHz signal.

The pilot cancelled signal is fed to the multiplex decoder. There, the side signal is demodulated and combined with the main signal in a matrix to left and right audio channel.

Compensation for roll-off in the incoming MPX signal caused by IF filters and FM demodulator is realized by corresponding side signal amplification.

A smooth mono to stereo take-over, which is controlled by the level detector voltage of the IF part, is achieved by the SNC (pins 16 and 17; see Fig.6).

From the output of the MPX demodulator the signals are fed to 2-pole low-pass filters with a cut-off frequency of 30 kHz to provide additional signal delay for noise blanking and attenuation of the subcarrier and its harmonics.

These filters are followed by the noise suppression gates, which are combined with de-emphasis and HCC. The de-emphasis is defined by internal resistors (aligned by an external current) and external capacitors (pins 13 and 14). For HCC, the de-emphasis time constant can be changed to higher values (pins 15 and 17; see Figs 7 to 9). This function is controlled by an analog input signal, derived from the level detector voltage of the IF part. When the VCO is turned **off** (pin 7 to GND), de-emphasis is reduced to 20 μs for full frequency response when AM-AF is fed through the stereo decoder. De-emphasis remains controllable.

From the gate circuits audio is fed through internal series resistors to the inverting inputs of the output operational amplifiers (pins 9 and 12), which can also be used as signal inputs for cassette playback or other sources when the mute is activated. The gain of these amplifiers is defined by external feedback resistors R_{out} (pins 9, 10, 11 and 12).

The input of the ignition noise blanker is the null node of an operational amplifier (pin 6). It can be driven by the level detector output of the FM-IF limiter and/or the MPX signal. Its sensitivity is dependent on the value of the series input resistor at pin 6.

The operational amplifier output signal is fed through an integrated 120 kHz high-pass filter, becomes amplified and is then fed in parallel to the noise detector and the interference detector. The noise detector is a negative peak detector. Its output (pin 8) controls the trigger sensitivity (prevention to false triggering at noisy input signals) and the attenuation of the input operational amplifier. The output of the interference detector, when receiving a steep pulse, triggers a mono flip-flop, which is a part of the pulse former circuit. The time constant of the mono flip-flop is defined by an external capacitor (pin 7) and its output activates the blanking gates in the audio.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 5)	0	13.2	V
P_{tot}	total power dissipation	0	0.25	W
T_{stg}	storage temperature	–55	+150	°C
T_{amb}	operating ambient temperature	–40	+85	°C
V_{es}	electrostatic handling for all pins; note 1	–400	+400	V

Note

1. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

CHARACTERISTICS

V_P = 10 V; T_{amb} = 25 °C; input signal $V_{i\ MPX(p-p)}$ = 1.7 V; m = 100% ($\Delta f = \pm 75$ kHz, f_{mod} = 1 kHz); de-emphasis of 50 μs and series resistor at input R_1 = 164 kΩ; measurements taken in Fig.1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 5)		7.5	10	12	V
I_P	supply current		–	15	20	mA
Stereo decoder						
$V_{i\ MPX(p-p)}$	MPX input signal		–	1.7	–	V
$\Delta V_{i\ MPX(p-p)}$	overdrive margin of MPX input signal	THD = 1%	6	–	–	dB
$V_{o(rms)}$	AF mono output signal at pins 10 and 11 (RMS value)	without pilot	800	900	1000	mV
ΔV_o	overdrive margin of output signal	THD = 1%	6	–	–	dB
V_{10-11}/V_o	difference of output voltage levels		–	–	1	dB
$V_{o\ 10,11}$	DC output voltage (pins 10 and 11)		3.2	3.7	4.2	V
$R_{o\ 10,11}$	output resistance		–	150	–	Ω
I_o	output current		330	400	–	μA
$R_{2,3}$	maximum feedback resistor		–	–	68	kΩ
$V_{4,3}$	reference voltage		3.7	3.8	3.9	V
α_{cs}	channel separation	pin 16 open-circuit; see Fig.6	30	40	–	dB
THD	total harmonic distortion		–	0.1	0.3	%
S/N	signal-to-noise ratio	f = 20 to 16000 Hz	77	82	–	dB
α_{19}	pilot signal suppression	f = 19 kHz	40	50	–	dB
α_{38}	subcarrier suppression	f = 38 kHz	35	50	–	dB
α_{57}		f = 57 kHz	46	–	–	dB
α_{76}		f = 76 kHz	–	60	–	dB
IM2	intermodulation for f_{spur} = 1 kHz	f_{mod} = 10 kHz; note 1	–	60	–	dB
IM3		f_{mod} = 13 kHz	–	58	–	dB
$\alpha_{57\ VF}$	traffic radio (VWF)	f = 57 kHz; note 2	–	70	–	dB
α_{67}	SCA (Subsidiary Communications Authorization)	f = 67 kHz; note 3	70	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
α_{114}	ACI (Adjacent Channel Interference)	f = 114 kHz; note 4	–	80	–	dB
α_{190}		f = 190 kHz; note 4	–	70	–	dB
PSRR	power supply ripple rejection	f = 100 Hz; $V_{ripple\ (rms)}$ = 100 mV	–	35	–	dB
VCO (pin 2)						
f_{osc}	oscillator frequency (ceramic resonator)		–	456	–	kHz
	frequency range of free running oscillator		451	–	459	kHz
$\Delta f/f$	capture and holding range		–	±0.65	–	%
V_7	VCO-**off** voltage (pin 7)		0	–	0.6	V
Mono/stereo control (pins 16, 17 and 19)						
$V_{i\ pilot}$	pilot threshold voltage for automatic switching by pilot input voltage (RMS value)	stereo **on**	–	24	30	mV
		stereo **off**	8	20	–	mV
HYS	hysteresis of pilot threshold voltage		–	2	–	dB
V_{19}	switching voltage for external mono control (pin 19)		–	–	0.7	V
V_{ref}	reference input voltage range (pin 17)		1	–	5	V
$V_{16\text{-}17}$	control voltage for channel separation due to pin 17 (V_{ref})	α_{cs} = 6 dB; see Fig.5	–80	–100	–120	mV
		α_{cs} = 20 dB; see Fig.5	–40	–55	–70	mV
Pilot indicator logic level output (pin 18)						
V_{18}	LOW voltage	I_{18} = 500 μA	–	250	400	mV
I_{18}	HIGH current	V_{18} = 10 V	–	–	1	μA
Muting (pin 8)						
$MUTE_{att}$	mute attenuation (pin 8)	V_8 < 1.6 V	80	–	–	dB
		V_8 > 4 V	–	–	0.2	dB
$V_{o(offset)}$	DC offset voltage (pins 10 and 11)	after muting	–	–	±50	mV
HCC (pin 15)						
CR_{deem}	control range of de-emphasis	see Figs 7 and 8				
	for European standard	C_{deem} = 6.8 nF	50	–	150	μs
	for USA standard	C_{deem} = 10 nF	75	–	225	μs
$V_{15\text{-}17}$	control voltage (pin 15 due to pin 17) in both standards	lower value CR_{deem}	–	0	–	mV
		upper value CR_{deem}	–	–300	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
HCC (pin 15, pin 7 to GND)						
CR_{deem}	control range of de-emphasis	see Fig.9				
	for European standard	C_{deem} = 6.8 nF	15	–	90	µs
	for USA standard	C_{deem} = 10 nF	22	–	135	µs
V_{15-17}	control voltage (pin 15 due to pin 17) in both standards	lower value CR_{deem}	–	0	–	mV
		upper value CR_{deem}	–	–300	–	mV
ΔV_{10}, ΔV_{11}	DC offset voltage at AF outputs (AM **on**/**off**)		–	–	±200	mV
Noise interference detector						
V_{pulse}	trigger sensitivity	τ_{pulse} = 10 µs	–	10	–	mV
ΔV_8	trigger threshold voltage offset as a function of V_{trigg}	f_{int} = 120 kHz				
		$V_{interf.in}$ = 10 mV	150	200	250	mV
		$V_{interf.in}$ = 100 mV	550	650	750	mV
t_{sup}	AF suppression time; pulse width		–	40	–	µs
$I_{13,14}$	input offset current (pins 13 and 14)	during AF suppression time	–	20	–	nA

Notes

1. Intermodulation suppression [Beat Frequency Components (BFC)]:

$$IM2 = \frac{V_{o(signal)}\,(\text{at 1 kHz})}{V_{o(spurious)}\,(\text{at 1 kHz})};\ f_s = (2 \times 10\ \text{kHz}) - 19\ \text{kHz}$$

$$IM3 = \frac{V_{o(signal)}\,(\text{at 1 kHz})}{V_{o(spurious)}\,(\text{at 1 kHz})};\ f_s = (3 \times 13\ \text{kHz}) - 38\ \text{kHz}$$

   measured with 91% mono signal; f_{mod} = 10 kHz or 13 kHz; 9% pilot signal.

2. ARI suppression:

$$\alpha_{57}ARI = \frac{V_{o(signal)}\,(\text{at 1 kHz})}{V_{o(spurious)}\,(\text{at 1 kHz} \pm 23\ \text{Hz})}$$

   measured with 91% stereo signal; f_{mod} = 1 kHz; 9% pilot signal; 5% ARI subcarrier (f_s = 57 kHz; f_{mod} = 23 Hz; AM m = 0.6).

3. Subsidiary Communication Authorization (SCA):

$$\alpha_{67} = \frac{V_{o(signal)}\,(\text{at 1 kHz})}{V_{o(spurious)}\,(\text{at 9 kHz})};\ f_s = (2 \times 38\ \text{kHz}) - 67\ \text{kHz}$$

   measured with 81% mono signal; f_{mod} = 1 kHz; 9% pilot signal; 10% SCA subcarrier (f_s = 67 kHz, unmodulated).

4. Adjacent Channel Interference (ACI):

$$\alpha_{114} = \frac{V_{o(signal)}\,(\text{at 1 kHz})}{V_{o(spurious)}\,(\text{at 4 kHz})};\ f_s = 110\ \text{kHz} - (3 \times 38\ \text{kHz})$$

$$\alpha_{190} = \frac{V_{o(signal)}\,(\text{at 1 kHz})}{V_{o(spurious)}\,(\text{at 4 kHz})};\ f_s = 186\ \text{kHz} - (5 \times 38\ \text{kHz})$$

   measured with 90% mono signal; f_{mod} = 1 kHz; 9% pilot signal; 1% spurious signal (f_s = 110 kHz or 186 kHz, unmodulated).

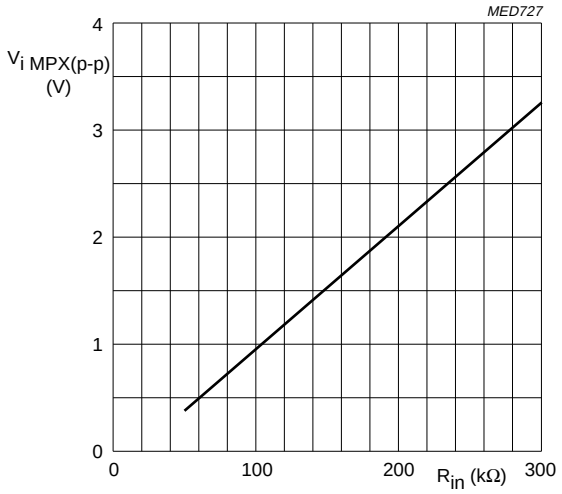


Fig.3 Input signal as a function of series input resistor R_{in}.

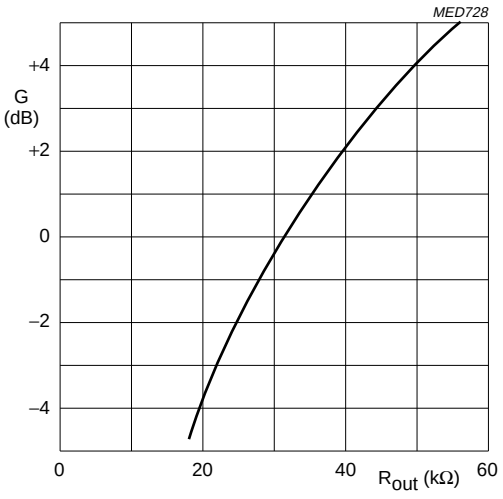
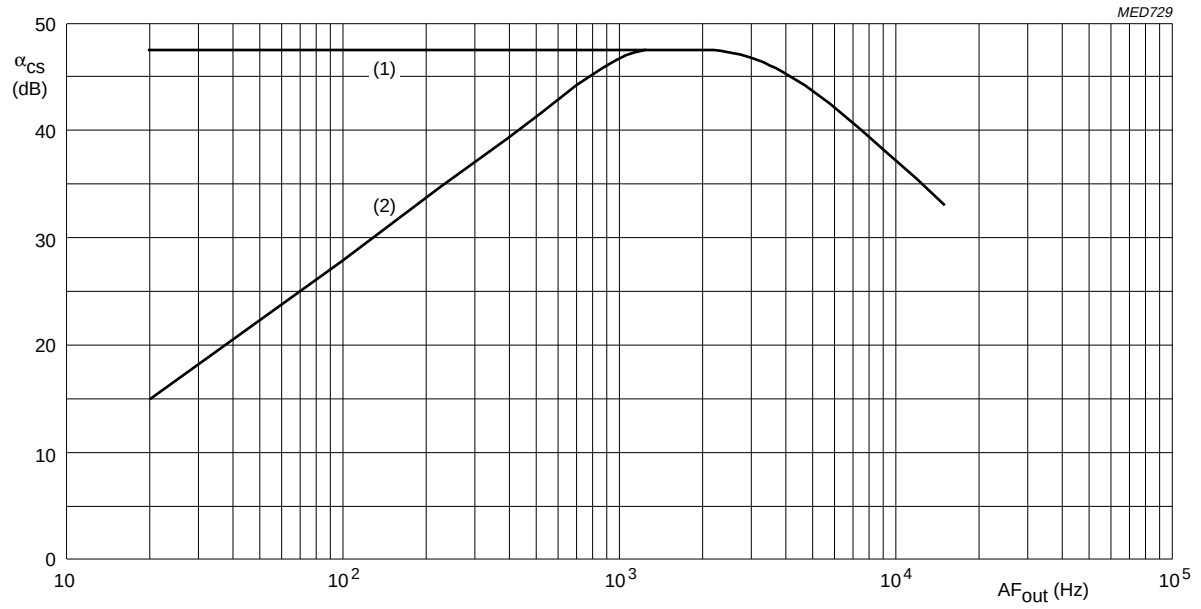


Fig.4 Overall signal gain as a function of feedback resistors R_{out} (R_{in} = 164 kΩ).



(1) Coupling capacitor C_K at pin 20 = 10 μF.
(2) Coupling capacitor C_K at pin 20 = 0.1 μF.

Fig.5 Channel separation as a function of audio frequency.

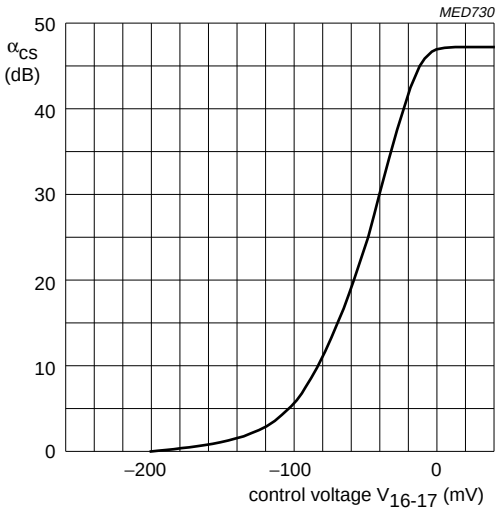


Fig.6 Stereo blend characteristic (SNC).

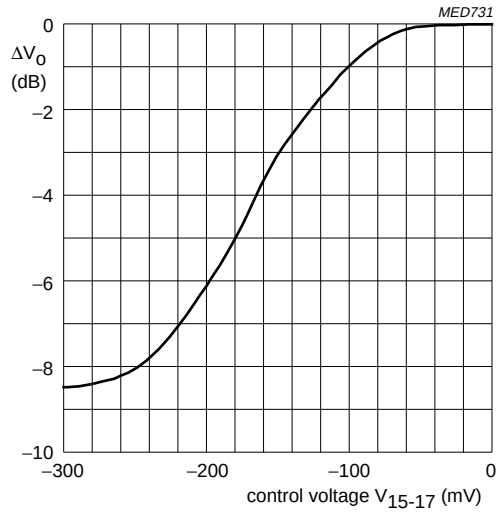
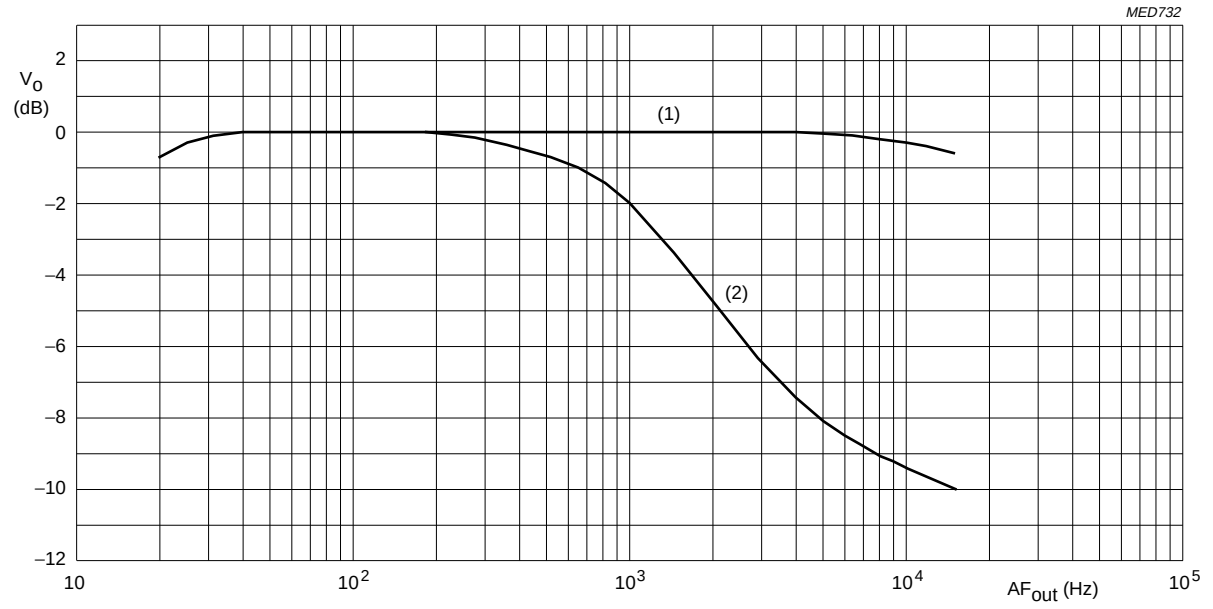
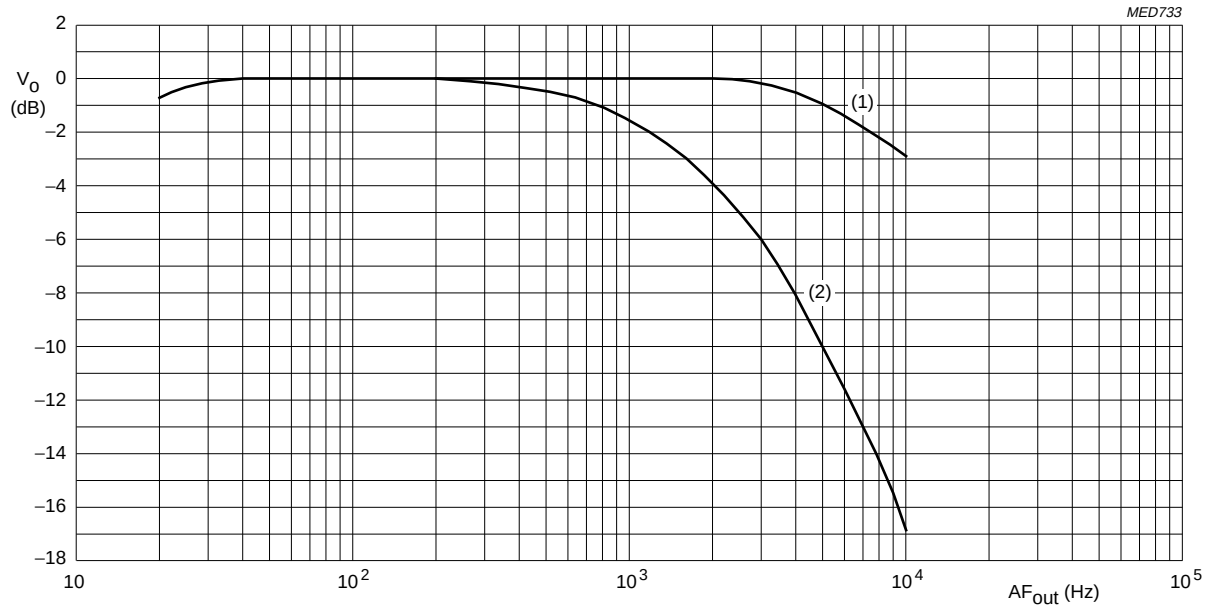


Fig.7 HCC with f_{mod} = 10 kHz.



(1) $V_{15\text{-}17}$ = 0.
(2) $V_{15\text{-}17}$ = –300 mV.

Fig.8 HCC with pre-emphasis as a function of audio frequency.



(1) $V_{15\text{-}17}$ = 0.
(2) $V_{15\text{-}17}$ = –300 mV.

Fig.9 HCC as a function of audio frequency (pin 7 connected to GND; without pre-emphasis).

INTERNAL PIN CONFIGURATION

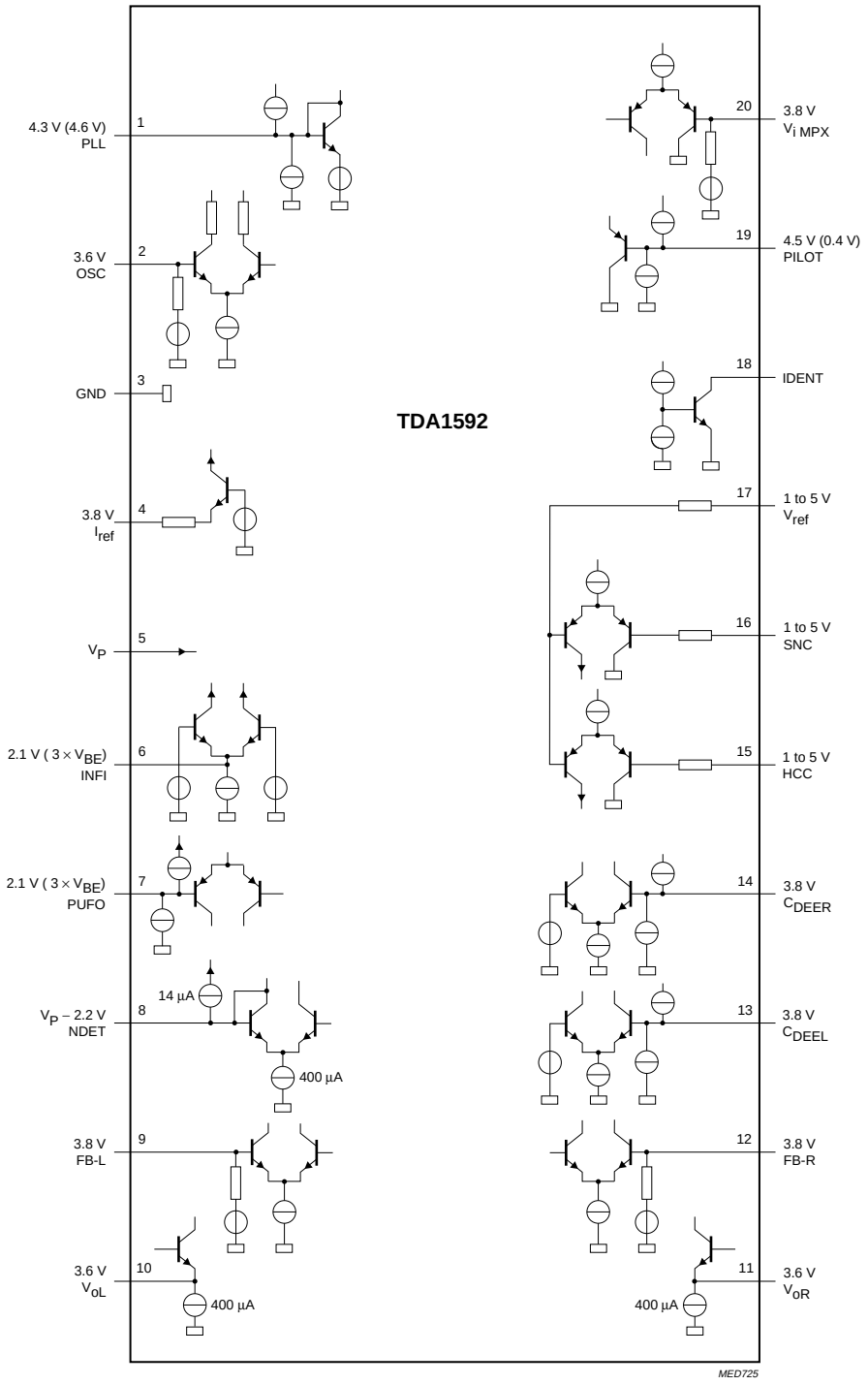


Fig.10 Internal circuitry.

TEST INFORMATION

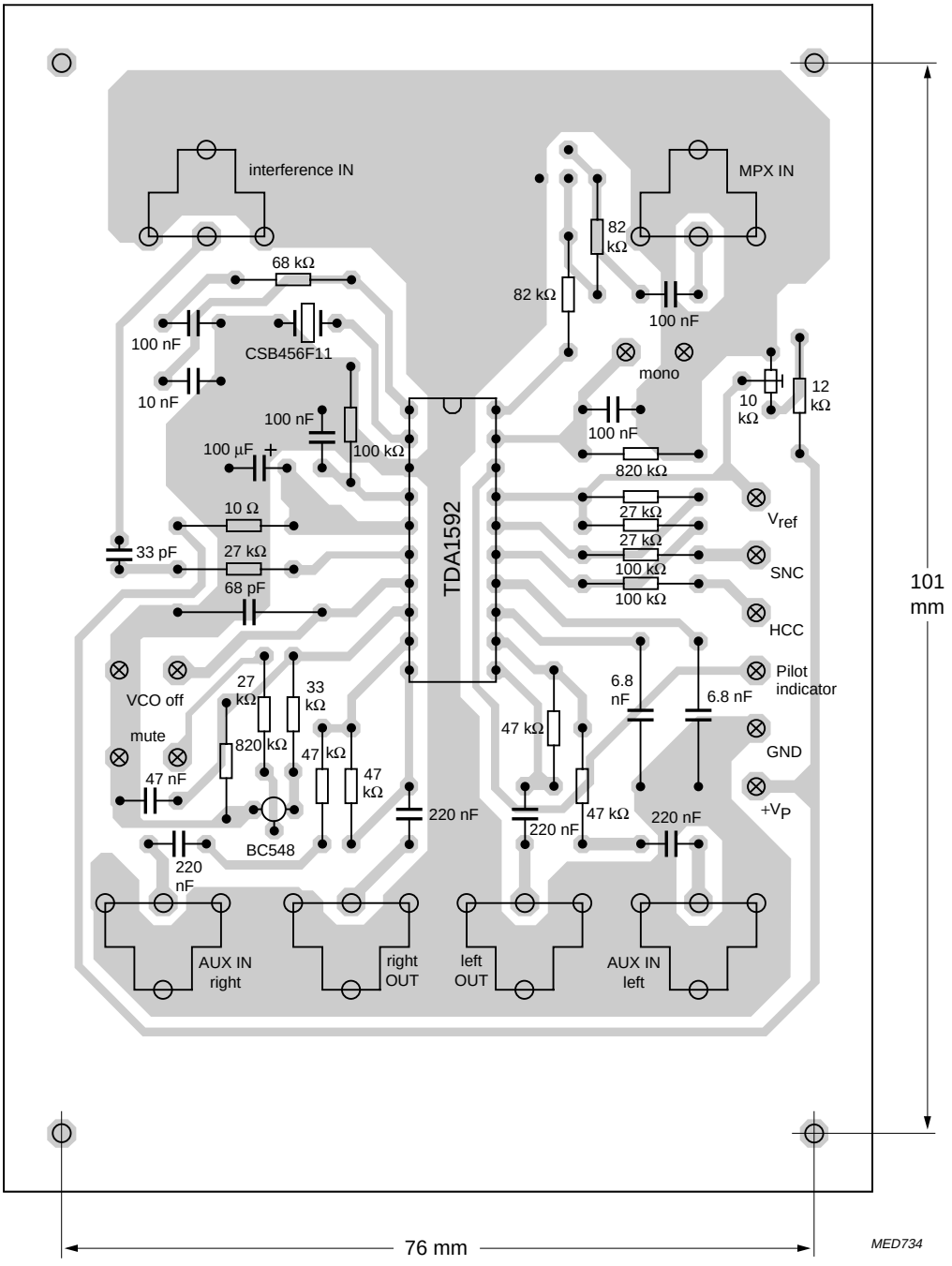
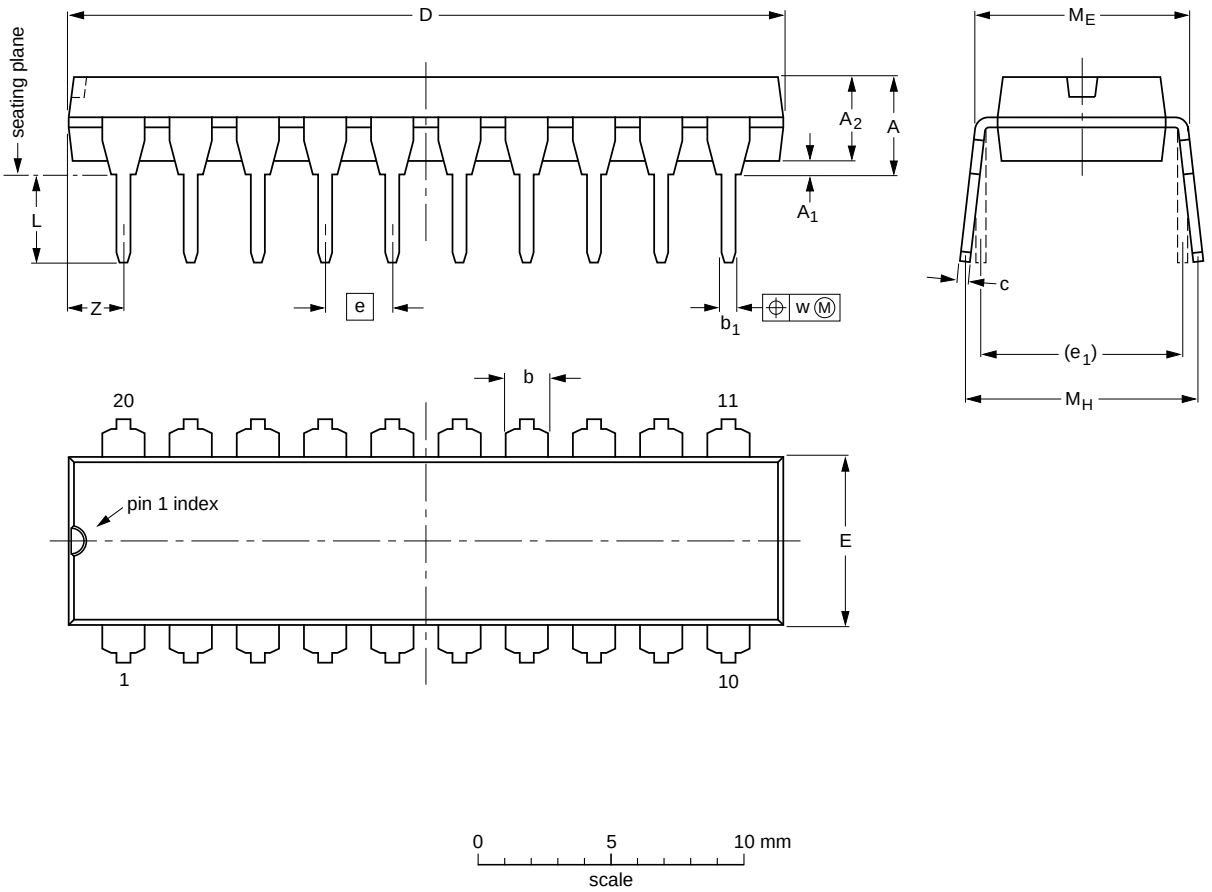


Fig.11 TDA1592 test board (component side).

PACKAGE OUTLINES

DIP20: plastic dual in-line package; 20 leads (300 mil) SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

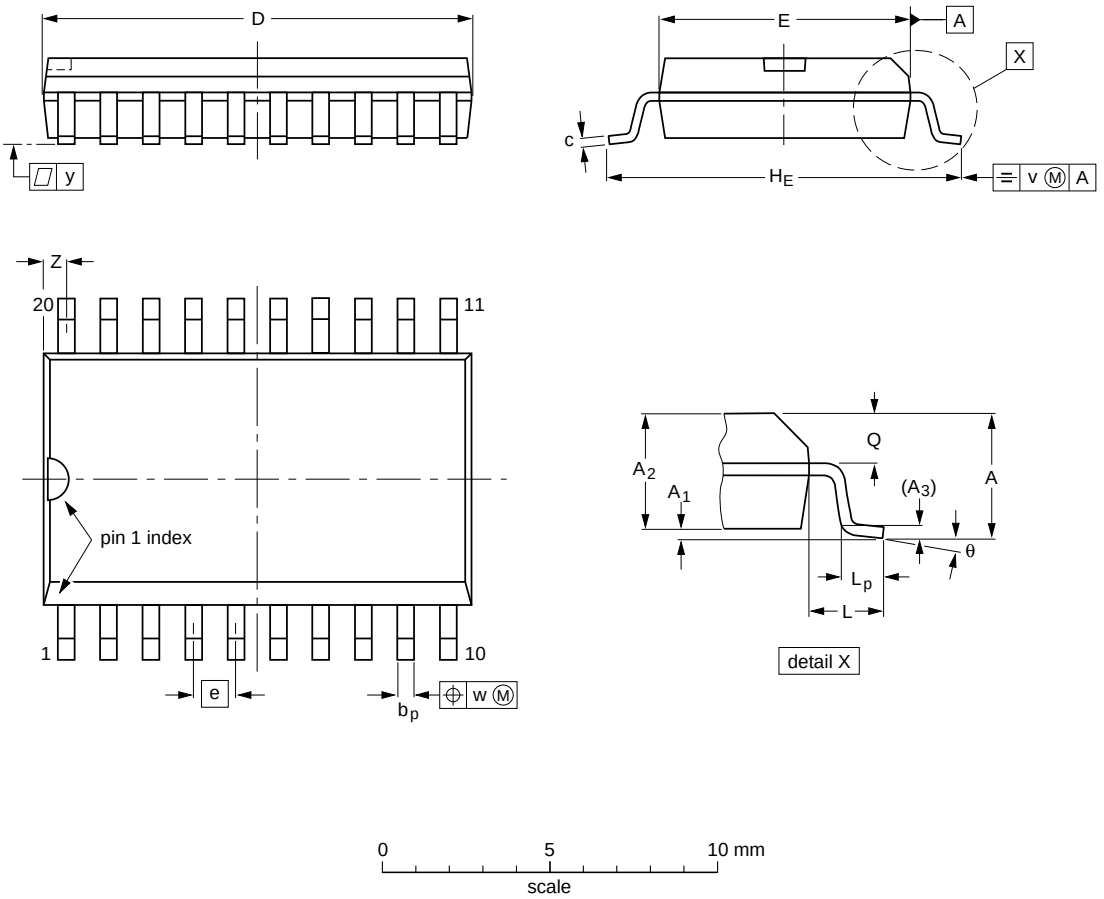
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~92-11-17~~ 95-01-24

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

DIP

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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