## Features

- **Single 3.3V ± 10% Supply**
- **Fast Read Access Time – 200 ns**
- **Automatic Page Write Operation**
  - **Internal Address and Data Latches for 128 Bytes**
  - **Internal Control Timer**
- **Fast Write Cycle Time**
  - **Page Write Cycle Time – 10 ms Maximum**
  - **1 to 128-Byte Page Write Operation**
- **Low Power Dissipation**
  - **15 mA Active Current**
  - **20 µA CMOS Standby Current**
- **Hardware and Software Data Protection**
- **$\overline{\text{DATA}}$ Polling for End of Write Detection**
- **High Reliability CMOS Technology**
  - **Endurance: $10^5$ Cycles**
  - **Data Retention: 10 Years**
- **JEDEC Approved Byte-Wide Pinout**
- **Industrial Temperature Range**
- **Green (Pb/Halide-free) Packaging Option Only**

1-Megabit
(128K x 8)
Low Voltage
Paged Parallel
EEPROMs

AT28LV010

## 1. Description

The AT28LV010 is a high-performance 3-volt only Electrically Erasable and Program-mable Read-Only Memory. Its 1 megabit of memory is organized as 131,072 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 200 ns with power dissipation of just 54 mW. When the device is deselected, the CMOS standby current is less than 20 µA.

The AT28LV010 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 128-byte page register to allow writing of up to 128 bytes simultaneously. During a write cycle, the address and 1 to 128 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{\text{DATA}}$ polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's 28LV010 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. Software data protection is implemented to guard against inadvertent writes. The device also includes an extra 128 bytes of EEPROM for device identification or tracking.

# 2. Pin Configurations

| Pin Name | Function |
|----------|----------|
| A0 - A16 | Addresses |
| $\overline{CE}$ | Chip Enable |
| $\overline{OE}$ | Output Enable |
| $\overline{WE}$ | Write Enable |
| I/O0 - I/O7 | Data Inputs/Outputs |
| NC | No Connect |
| DC | Don't Connect |

## 2.2  32-lead TSOP Top View

| | | | |
|---|---|---|---|
| A11 | 1 | 32 | $\overline{OE}$ |
| A9 | 2 | 31 | A10 |
| A8 | 3 | 30 | $\overline{CE}$ |
| A13 | 4 | 29 | I/O7 |
| A14 | 5 | 28 | I/O6 |
| NC | 6 | 27 | I/O5 |
| $\overline{WE}$ | 7 | 26 | I/O4 |
| VCC | 8 | 25 | I/O3 |
| NC | 9 | 24 | GND |
| A16 | 10 | 23 | I/O2 |
| A15 | 11 | 22 | I/O1 |
| A12 | 12 | 21 | I/O0 |
| A7 | 13 | 20 | A0 |
| A6 | 14 | 19 | A1 |
| A5 | 15 | 18 | A2 |
| A4 | 16 | 17 | A3 |

## 2.1  32-lead PLCC Top View

Top pins (left to right): A12 (4), A15 (3), A16 (2), DC (1), VCC (32), $\overline{WE}$ (31), NC (30)

Left pins (top to bottom): A7 (5), A6 (6), A5 (7), A4 (8), A3 (9), A2 (10), A1 (11), A0 (12), I/O0 (13)

Right pins (top to bottom): A14 (29), A13 (28), A8 (27), A9 (26), A11 (25), $\overline{OE}$ (24), A10 (23), $\overline{CE}$ (22), I/O7 (21)

Bottom pins (left to right): I/O1 (14), I/O2 (15), GND (16), I/O3 (17), I/O4 (18), I/O5 (19), I/O6 (20)

## 3.   Block Diagram



## 4.   Device Operation

### 4.1   Read

The AT28LV010 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

### 4.2   Write

The write operation of the AT28LV010 allows 1 to 128 bytes of data to be written into the device during a single internal programming period. Each write operation must be preceded by the software data protection (SDP) command sequence. This sequence is a series of three unique write command operations that enable the internal write circuitry. The command sequence and the data to be written must conform to the software protected write cycle timing. Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last and data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Each successive byte must be written within 150 μs ($t_{BLC}$) of the previous byte. If the $t_{BLC}$ limit is exceeded the AT28LV010 will cease accepting data and commence the internal programming operation. If more than one data byte is to be written during a single programming operation, they must reside on the same page as defined by the state of the A7 - A16 inputs. For each $\overline{WE}$ high to low transition during the page write operation, A7 - A16 must be the same.

The A0 to A6 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

## 4.3 $\overline{\text{DATA}}$ Polling

The AT28LV010 features $\overline{\text{DATA}}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{\text{DATA}}$ Polling may begin at anytime during the write cycle.

## 4.4 Toggle Bit

In addition to $\overline{\text{DATA}}$ Polling the AT28LV010 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

## 4.5 Data Protection

If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Atmel® has incorporated both hardware and software features that will protect the memory against inadvertent writes.

### 4.5.1 Hardware Protection

Hardware features protect against inadvertent writes to the AT28LV010 in the following ways: (a) $V_{CC}$ power-on delay – once $V_{CC}$ has reached 2.0V (typical) the device will automatically time out 5 ms (typical) before allowing a write; (b) write inhibit – holding any one of $\overline{\text{OE}}$ low, $\overline{\text{CE}}$ high or $\overline{\text{WE}}$ high inhibits write cycles; and (c) noise filter – pulses of less than 15 ns (typical) on the $\overline{\text{WE}}$ or $\overline{\text{CE}}$ inputs will not initiate a write cycle.

### 4.5.2 Software Data Protection

The AT28LV010 incorporates the industry standard software data protection (SDP) function. Unlike standard 5-volt only EEPROM's, the AT28LV010 has SDP enabled at all times. Therefore, all write operations must be preceded by the SDP command sequence.

The data in the 3-byte command sequence is not written to the device; the addresses in the command sequence can be utilized just like any other location in the device. Any attempt to write to the device without the 3-byte sequence will start the internal timers. No data will be written to the device. However, for the duration of $t_{WC}$, read operations will effectively be polling operations.

## 5. DC and AC Operating Range

|  |  | AT28LV010-20 | AT28LV010-25 |
|---|---|---|---|
| Operating Temperature (Case) | Ind. | -40°C - 85°C | -40°C - 85°C |
| $V_{CC}$ Power Supply |  | 3.3V $\pm$ 5% | 3.3V $\pm$ 10% |

## 6. Operating Modes

| Mode | $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | I/O |
|---|---|---|---|---|
| Read | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $D_{OUT}$ |
| Write[2] | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $D_{IN}$ |
| Standby/Write Inhibit | $V_{IH}$ | X[1] | X | High Z |
| Write Inhibit | X | X | $V_{IH}$ | |
| Write Inhibit | X | $V_{IL}$ | X | |
| Output Disable | X | $V_{IH}$ | X | High Z |

Notes: 1. X can be $V_{IL}$ or $V_{IH}$.

2. Refer to AC Programming Waveforms.

## 7. Absolute Maximum Ratings*

Temperature Under Bias ................................ -55°C to +125°C

Storage Temperature ..................................... -65°C to +150°C

All Input Voltages (including NC Pins)
with Respect to Ground ................................... -0.6V to +6.25V

All Output Voltages
with Respect to Ground ............................. -0.6V to $V_{CC}$ + 0.6V

Voltage on $\overline{OE}$ and A9
with Respect to Ground ................................... -0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

## 8. DC Characteristics

| Symbol | Parameter | Condition | | Min | Max | Units |
|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Load Current | $V_{IN}$ = 0V to $V_{CC}$ | | | 1 | μA |
| $I_{LO}$ | Output Leakage Current | $V_{I/O}$ = 0V to $V_{CC}$ | | | 1 | μA |
| $I_{SB}$ | $V_{CC}$ Standby Current CMOS | $\overline{CE}$ = $V_{CC}$ - 0.3V to $V_{CC}$ + 1V | Ind. | | 50 | μA |
| $I_{CC}$ | $V_{CC}$ Active Current | f = 5 MHz; $I_{OUT}$ = 0 mA; $V_{CC}$ = 3.6V | | | 15 | mA |
| $V_{IL}$ | Input Low Voltage | | | | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | | 2.0 | | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 1.6 mA; $V_{CC}$ = 3.0V | | | 0.45 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -100 μA; $V_{CC}$ = 3.0V | | 2.4 | | V |

## 9. AC Read Characteristics

| Symbol | Parameter | AT28LV010-20 | | Units |
|---|---|---|---|---|
| | | Min | Max | |
| $t_{ACC}$ | Address to Output Delay | | 200 | ns |
| $t_{CE}$[1] | $\overline{CE}$ to Output Delay | | 200 | ns |
| $t_{OE}$[2] | $\overline{OE}$ to Output Delay | 0 | 80 | ns |
| $t_{DF}$[3][4] | $\overline{CE}$ or $\overline{OE}$ to Output Float | 0 | 55 | ns |
| $t_{OH}$ | Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, Whichever Occurred First | 0 | | ns |

## 10. AC Read Waveforms[1][2][3][4]
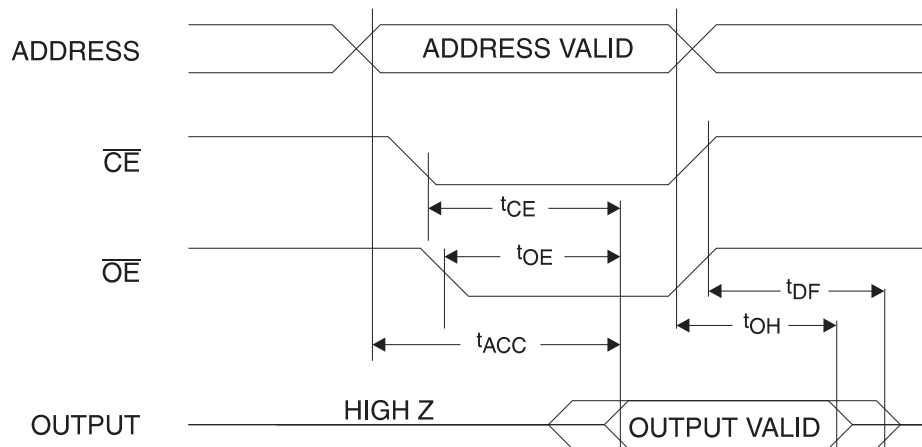


Notes: 1. $\overline{CE}$ may be delayed up to $t_{ACC}$ - $t_{CE}$ after the address transition without impact on $t_{ACC}$.

2. $\overline{OE}$ may be delayed up to $t_{CE}$ - $t_{OE}$ after the falling edge of $\overline{CE}$ without impact on $t_{CE}$ or by $t_{ACC}$ - $t_{OE}$ after an address change without impact on $t_{ACC}$.

3. $t_{DF}$ is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first ($C_L$ = 5 pF).

4. This parameter is characterized and is not 100% tested.

## 11. Input Test Waveforms and Measurement Level

AC
DRIVING
LEVELS

3.0V

1.5V

0.0V

$t_R$, $t_F$ < 5 ns

AC
MEASUREMENT
LEVEL

## 12. Output Test Load

5.0V

1.8K

OUTPUT
PIN

1.3K

100 pF
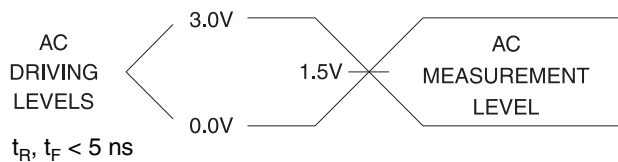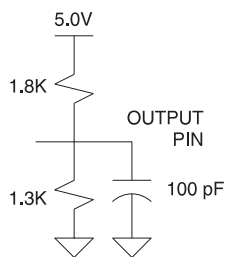
## 13. Pin Capacitance

f = 1 MHz, T = 25°C[1]

| Symbol | Typ | Max | Units | Conditions |
|--------|-----|-----|-------|------------|
| $C_{IN}$ | 4 | 6 | pF | $V_{IN} = 0V$ |
| $C_{OUT}$ | 8 | 12 | pF | $V_{OUT} = 0V$ |

Note: 1. This parameter is characterized and is not 100% tested.

# 14. AC Write Characteristics[1]

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $t_{AS}$, $t_{OES}$ | Address, $\overline{OE}$ Set-up Time | 0 | | ns |
| $t_{AH}$ | Address Hold Time | 100 | | ns |
| $t_{CS}$ | Chip Select Set-up Time | 0 | | ns |
| $t_{CH}$ | Chip Select Hold Time | 0 | | ns |
| $t_{WP}$ | Write Pulse Width ($\overline{WE}$ or $\overline{CE}$) | 200 | | ns |
| $t_{DS}$ | Data Set-up Time | 100 | | ns |
| $t_{DH}$, $t_{OEH}$ | Data, $\overline{OE}$ Hold Time | 10 | | ns |

Note:  1.  All write operations must be preceded by the SDP command sequence.

# 15. AC Write Waveforms

## 15.1  $\overline{WE}$ Controlled
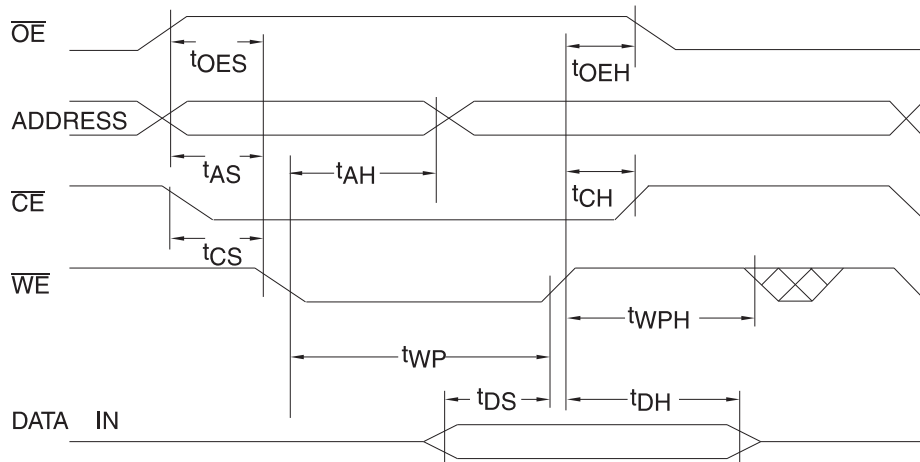


## 15.2  $\overline{CE}$ Controlled
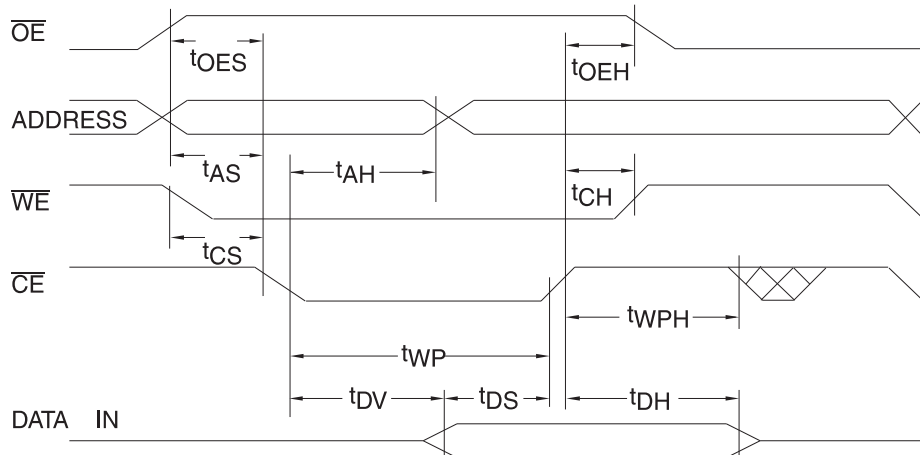
## 16. Software Protected Write Characteristics

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $t_{WC}$ | Write Cycle Time | | 10 | ms |
| $t_{AS}$ | Address Set-up Time | 0 | | ns |
| $t_{AH}$ | Address Hold Time | 100 | | ns |
| $t_{DS}$ | Data Set-up Time | 100 | | ns |
| $t_{DH}$ | Data Hold Time | 10 | | ns |
| $t_{WP}$ | Write Pulse Width | 200 | | ns |
| $t_{BLC}$ | Byte Load Cycle Time | | 150 | µs |
| $t_{WPH}$ | Write Pulse Width High | 100 | | ns |

## 17. Programming Algorithm



LOAD DATA AA TO ADDRESS 5555

LOAD DATA 55 TO ADDRESS 2AAA

LOAD DATA A0 TO ADDRESS 5555 — WRITES ENABLED[2]

LOAD DATA XX TO ANY ADDRESS[3]

LOAD LAST BYTE TO LAST ADDRESS[3] — ENTER DATA PROTECT STATE
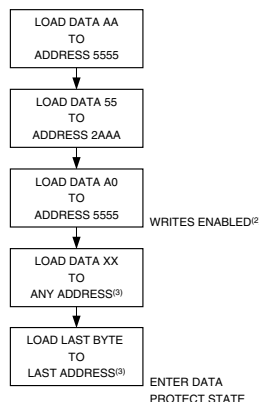
Notes: 1. Data Format: I/O7 - I/O0 (Hex); Address Format: A14 - A0 (Hex).

2. Data protect state will be re-activated at the end of program cycle.

3. 1 to 128 bytes of data are loaded.

## 18. Software Protected Program Cycle Waveforms[1][2][3]
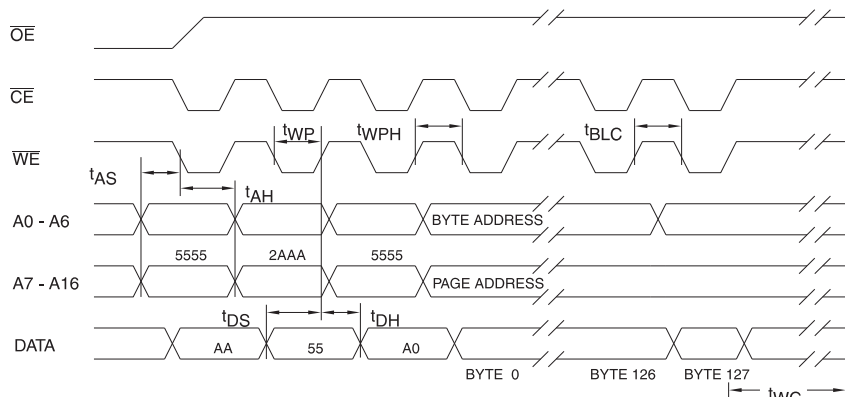


Notes: 1. A0 - A14 must conform to the addressing sequence for the first three bytes as shown above.

2. After the command sequence has been issued and a page write operation follows, the page address inputs (A7 - A16) must be the same for each high to low transition of $\overline{WE}$ (or $\overline{CE}$).

3. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

## 19. $\overline{\text{Data}}$ Polling Characteristics[1]

| Symbol | Parameter | Min | Typ | Max | Units |
|--------|-----------|-----|-----|-----|-------|
| $t_{DH}$ | Data Hold Time | 10 | | | ns |
| $t_{OEH}$ | $\overline{\text{OE}}$ Hold Time | 10 | | | ns |
| $t_{OE}$ | $\overline{\text{OE}}$ to Output Delay[2] | | | | ns |
| $t_{WR}$ | Write Recovery Time | 0 | | | ns |

Notes: 1. These parameters are characterized and not 100% tested.

2. See AC Read Characteristics

## 20. $\overline{\text{Data}}$ Polling Waveforms
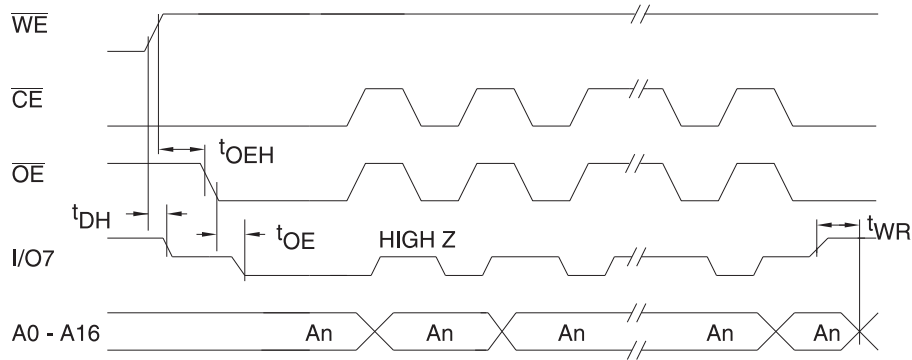


## 21. Toggle Bit Characteristics[1]

| Symbol | Parameter | Min | Typ | Max | Units |
|--------|-----------|-----|-----|-----|-------|
| $t_{DH}$ | Data Hold Time | 10 | | | ns |
| $t_{OEH}$ | $\overline{\text{OE}}$ Hold Time | 10 | | | ns |
| $t_{OE}$ | $\overline{\text{OE}}$ to Output Delay[2] | | | | ns |
| $t_{OEHP}$ | $\overline{\text{OE}}$ High Pulse | 150 | | | ns |
| $t_{WR}$ | Write Recovery Time | 0 | | | ns |

Notes: 1. These parameters are characterized and not 100% tested.

2. See AC Read Characteristics

## 22. Toggle Bit Waveforms
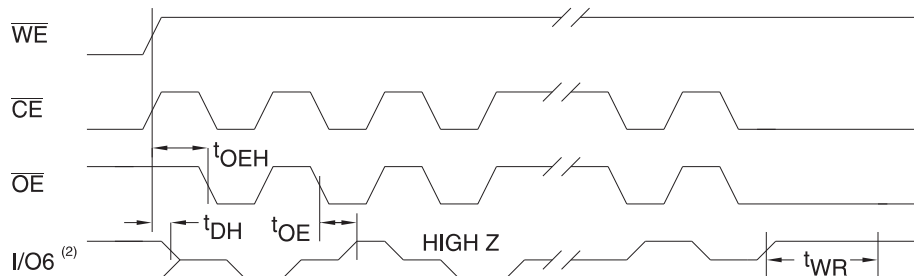


Notes: 1. Toggling either $\overline{\text{OE}}$ or $\overline{\text{CE}}$ or both $\overline{\text{OE}}$ and $\overline{\text{CE}}$ will operate toggle bit.

2. Beginning and ending state of I/O6 will vary.

3. Any address location may be used but the address should not vary.

## 23. Ordering Information

### 23.1    Green Package Option (Pb/Halide-free)

| t_ACC (ns) | I_CC (mA) | | Ordering Code | Package | Operation Range |
|---|---|---|---|---|---|
| | Active | Standby | | | |
| 200 | 15 | 0.05 | AT28LV010-20JU | 32J | Industrial (-40° to 85°C) |
| | | | AT28LV010-20TU | 32T | |

| Package Type | |
|---|---|
| **32J** | 32-lead, Plastic J-leaded Chip Carrier (PLCC) |
| **32T** | 32-lead, Plastic Thin Small Outline Package (TSOP) |

### 23.2    Die Products

Contact Atmel Sales for die sales options.

# 24. Packaging Information

## 24.1  32J – PLCC



1.14(0.045) X 45°

PIN NO. 1
IDENTIFIER

1.14(0.045) X 45°

0.318(0.0125)
0.191(0.0075)

B1   E2

E1   E

B

e

A2

A1

A

D1

D

0.51(0.020)MAX
45° MAX (3X)

D2
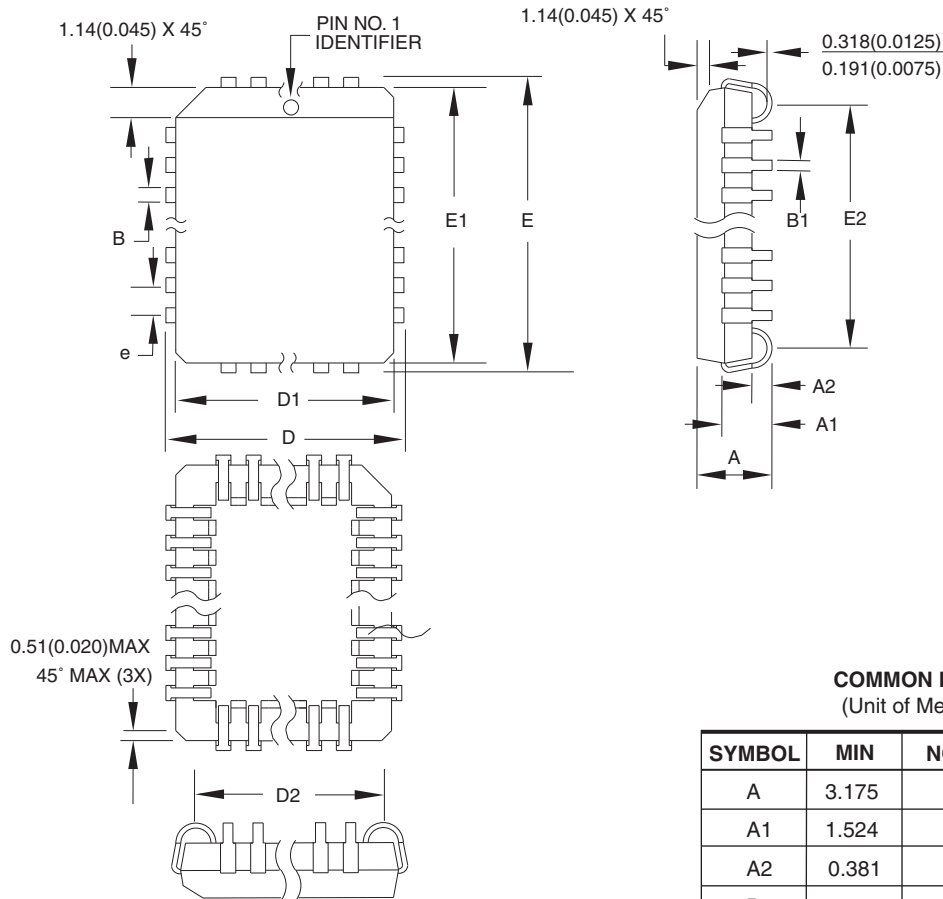
**COMMON DIMENSIONS**
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|-----|-----|-----|------|
| A | 3.175 | – | 3.556 | |
| A1 | 1.524 | – | 2.413 | |
| A2 | 0.381 | – | – | |
| D | 12.319 | – | 12.573 | |
| D1 | 11.354 | – | 11.506 | Note 2 |
| D2 | 9.906 | – | 10.922 | |
| E | 14.859 | – | 15.113 | |
| E1 | 13.894 | – | 14.046 | Note 2 |
| E2 | 12.471 | – | 13.487 | |
| B | 0.660 | – | 0.813 | |
| B1 | 0.330 | – | 0.533 | |
| e | 1.270 TYP | | | |

10/04/01

Notes:  1. This package conforms to JEDEC reference MS-016, Variation AE.
 2. Dimensions D1 and E1 do not include mold protrusion.
    Allowable protrusion is .010"(0.254 mm) per side. Dimension D1
    and E1 include mold mismatch and are measured at the extreme
    material condition at the upper or lower parting line.
 3. Lead coplanarity is 0.004" (0.102 mm) maximum.

| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| 2325 Orchard Parkway San Jose, CA  95131 | **32J**, 32-lead, Plastic J-leaded Chip Carrier (PLCC) | 32J | B |

0395E–PEEPR–2/09

## 24.2  32T – TSOP



PIN 1

Pin 1 Identifier

D1  D

e

b

E

A2  A

A1

0° ~ 8°

c

L

L1

SEATING PLANE

GAGE PLANE
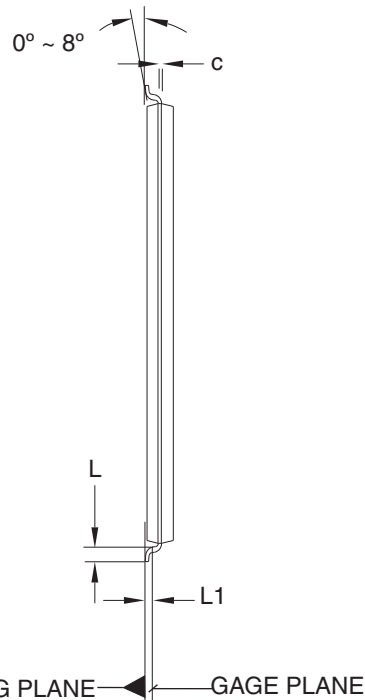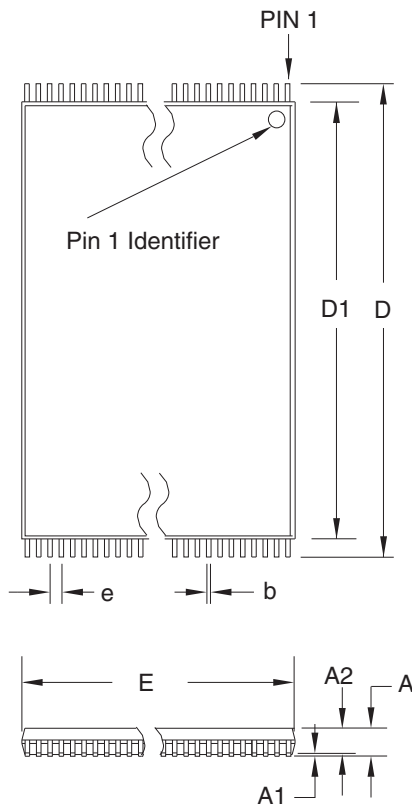
**COMMON DIMENSIONS**
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|-----|-----|-----|------|
| A | – | – | 1.20 | |
| A1 | 0.05 | – | 0.15 | |
| A2 | 0.95 | 1.00 | 1.05 | |
| D | 19.80 | 20.00 | 20.20 | |
| D1 | 18.30 | 18.40 | 18.50 | Note 2 |
| E | 7.90 | 8.00 | 8.10 | Note 2 |
| L | 0.50 | 0.60 | 0.70 | |
| L1 | 0.25 BASIC | | | |
| b | 0.17 | 0.22 | 0.27 | |
| c | 0.10 | – | 0.21 | |
| e | 0.50 BASIC | | | |

Notes:  1. This package conforms to JEDEC reference MO-142, Variation BD.
2. Dimensions D1 and E do not include mold protrusion.  Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
3. Lead coplanarity is 0.10 mm maximum.

10/18/01

| | | TITLE | DRAWING NO. | REV. |
|---|---|---|---|---|
| **AMEL** | 2325 Orchard Parkway San Jose, CA  95131 | **32T**, 32-lead (8 x 20 mm Package) Plastic Thin Small Outline Package, Type I (TSOP) | 32T | B |

## Headquarters

**Atmel Corporation**
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

## International

**Atmel Asia**
Unit 1-5 & 16, 19/F
BEA Tower, Millennium City 5
418 Kwun Tong Road
Kwun Tong, Kowloon
Hong Kong
Tel: (852) 2245-6100
Fax: (852) 2722-1369

**Atmel Europe**
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054 Saint-Quentin-en-
Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

**Atmel Japan**
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

## Product Contact

**Web Site**
www.atmel.com

**Technical Support**
p_eeprom@atmel.com

**Sales Contact**
www.atmel.com/contacts

**Literature Requests**
www.atmel.com/literature