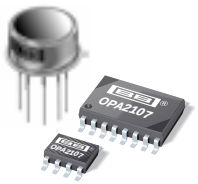
BURR - BROWN®



OPA2107

Precision Dual *Difet* ® OPERATIONAL AMPLIFIER

FEATURES

- VERY LOW NOISE: 8nV/√Hz at 10kHz
- LOW V_{os}: 1mV max
- LOW DRIFT: 10μV/°C max
- LOW I_B: 10pA max
- FAST SETTLING TIME: 2μs to 0.01%
- UNITY-GAIN STABLE

APPLICATIONS

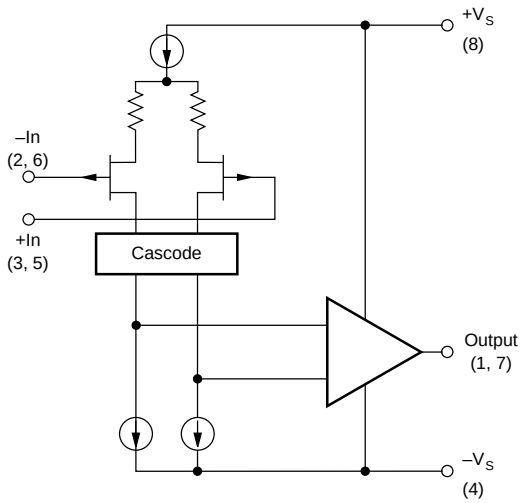
- DATA ACQUISITION
- DAC OUTPUT AMPLIFIER
- OPTOELECTRONICS
- HIGH-IMPEDANCE SENSOR AMPS
- HIGH-PERFORMANCE AUDIO CIRCUITRY
- MEDICAL EQUIPMENT, CT SCANNERS

DESCRIPTION

The OPA2107 dual operational amplifier provides precision ***Difet*** performance with the cost and space savings of a dual op amp. It is useful in a wide range of precision and low-noise analog circuitry and can be used to upgrade the performance of designs currently using BIFET® type amplifiers.

The OPA2107 is fabricated on a proprietary dielectrically isolated (***Difet***) process. This holds input bias currents to very low levels without sacrificing other important parameters, such as input offset voltage, drift and noise. Laser-trimmed input circuitry yields excellent DC performance. Superior dynamic performance is achieved, yet quiescent current is held to under 2.5mA per amplifier. The OPA2107 is unity-gain stable.

The OPA2107 is available in plastic DIP and SOIC packages. Industrial temperature range versions are available.



Difet® Burr-Brown Corp.
BIFET® National Semiconductor

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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-863E
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SPECIFICATIONS

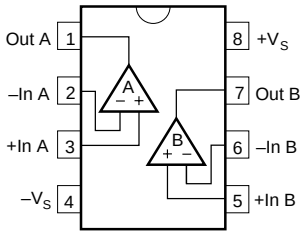
At T_A = +25°C, V_S = ±15V, unless otherwise noted.

PARAMETER	CONDITION	OPA2107AP, AU			UNITS
		MIN	TYP	MAX	
OFFSET VOLTAGE[1]					
Input Offset Voltage	V_{CM} = 0V		100	1	mV
Over Specified Temperature			0.5	2	mV
Average Drift Over Specified Temperature			3	10	µV/°C
Power Supply Rejection	V_S = ±10 to ±18V	80	96		dB
INPUT BIAS CURRENT[1]					
Input Bias Current	V_{CM} = 0V		4	10	pA
Over Specified Temperature			0.25	1.5	nA
Input Offset Current	V_{CM} = 0V		1	8	pA
Over Specified Temperature				1	nA
INPUT NOISE					
Voltage: f = 10Hz	R_S = 0		30		nV/√Hz
f = 100Hz			12		nV/√Hz
f = 1kHz			9		nV/√Hz
f = 10kHz			8		nV/√Hz
BW = 0.1 to 10Hz			1.2		µVp-p
BW = 10 to 10kHz			0.85		µVrms
Current: f = 0.1Hz thru 20kHz			1.2		fA/√Hz
BW = 0.1Hz to 10Hz			23		fAp-p
INPUT IMPEDANCE					
Differential			10^{13} || 2		Ω || pF
Common-Mode			10^{14} || 4		Ω || pF
INPUT VOLTAGE RANGE					
Common-Mode Input Range		±10.5	±11		V
Over Specified Temperature		±10.2	±10.5		V
Common-Mode Rejection	V_{CM} = ±10V	80	94		dB
OPEN-LOOP GAIN					
Open-Loop Voltage Gain	V_O = ±10V, R_L = 2kΩ	82	96		dB
Over Specified Temperature		80	94		dB
DYNAMIC RESPONSE					
Slew Rate	G = +1	13	18		V/µs
Settling Time: 0.1%	G = –1, 10V Step		1.5		µs
0.01%			2		µs
Gain Bandwidth Product	G = 100		4.5		MHz
THD + Noise	G = +1, f = 1kHz		0.001		%
Channel Separation	f = 100Hz, R_L = 2kΩ		120		dB
POWER SUPPLY					
Specified Operating Voltage			±15		V
Operating Voltage Range		±4.5			V
Current			±4.5		mA
OUTPUT					
Voltage Output	R_L = 2kΩ	±11	±12		V
Over Specified Temperature		±10.5	±11.5		V
Short Circuit Current		±10	±40		mA
Output Resistance, Open-Loop	1MHz		70		Ω
Capacitive Load Stability	G = +1		1000		pF
TEMPERATURE RANGE					
Specification		–25		+85	°C
Operating		–25		+85	°C
Storage		–40		+125	°C
Thermal Resistance (θ_{J-A})					
8-Pin DIP			90		°C/W
8-Lead Surface Mount			175		°C/W

NOTE: (1) Specified with devices fully warmed up.

PIN CONFIGURATION

Top View **DIP, SOIC**



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage	±18V
Input Voltage Range	$\pm V_S$ ±2V
Differential Input Voltage	Total V_S ±4V
Operating Temperature	
P and U Packages	–25°C to + 85°C
Storage Temperature	
P and U Packages	–40°C to +125°C
Output Short Circuit to Ground (T_A = +25°C)	Continuous
Junction Temperature	+175°C
Lead Temperature	
P Package (soldering, 10s)	+300°C
U Package, SOIC (3s)	+260°C

NOTE: Stresses above these ratings may cause permanent damage.

PACKAGE/ORDERING INFORMATION

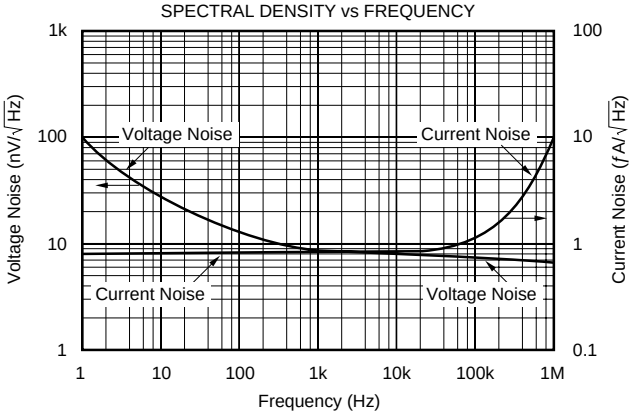
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)	TEMPERATURE RANGE
OPA2107AP	Plastic DIP	006	–25 to +85°C
OPA2107AU	SO-8 SOIC	182	–25 to +85°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

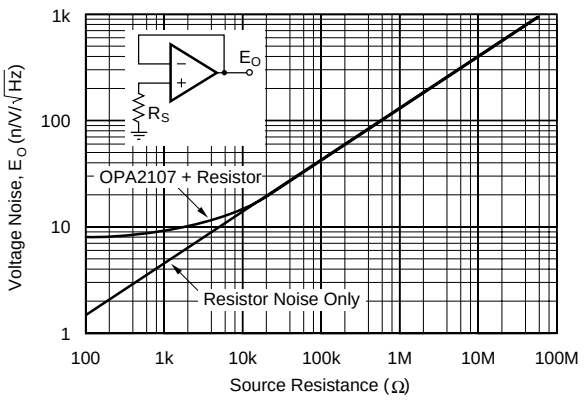
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15V unless otherwise noted.

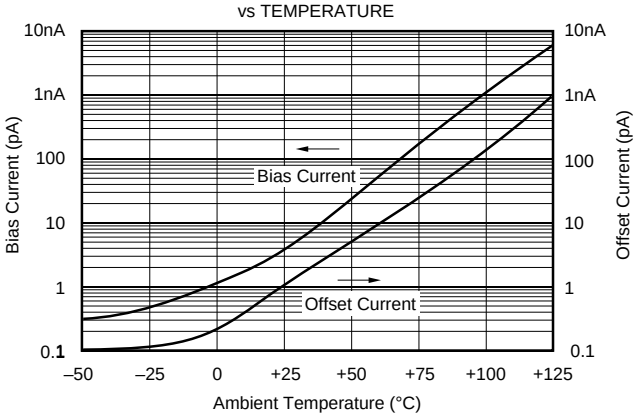
INPUT VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY



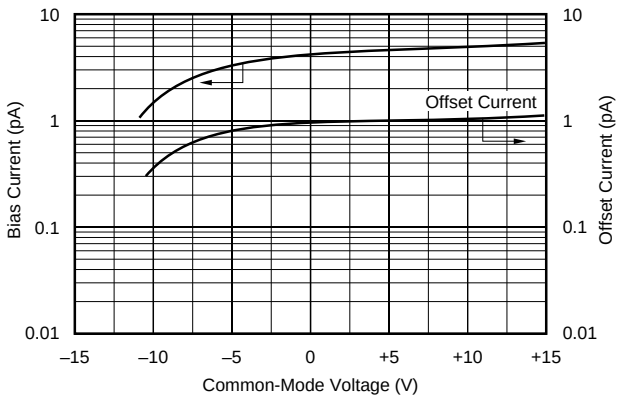
TOTAL INPUT VOLTAGE NOISE SPECTRAL DENSITY at 1kHz vs SOURCE RESISTANCE



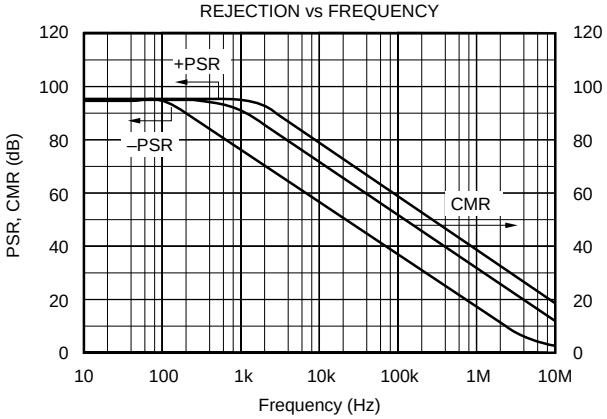
INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE



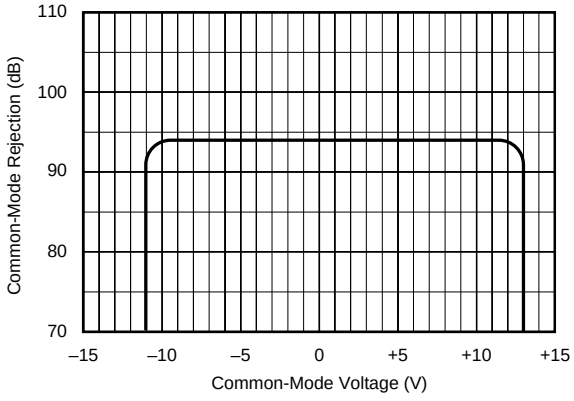
INPUT BIAS AND OFFSET CURRENT vs INPUT COMMON-MODE VOLTAGE



POWER SUPPLY AND COMMON-MODE REJECTION vs FREQUENCY



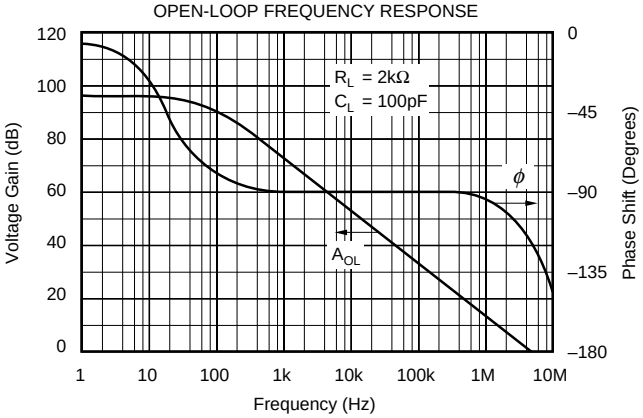
COMMON-MODE REJECTION vs INPUT COMMON-MODE VOLTAGE



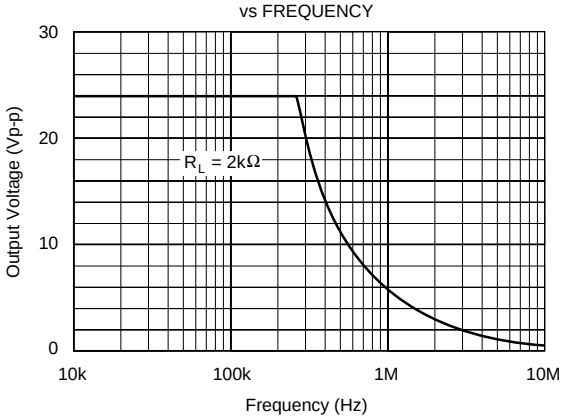
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

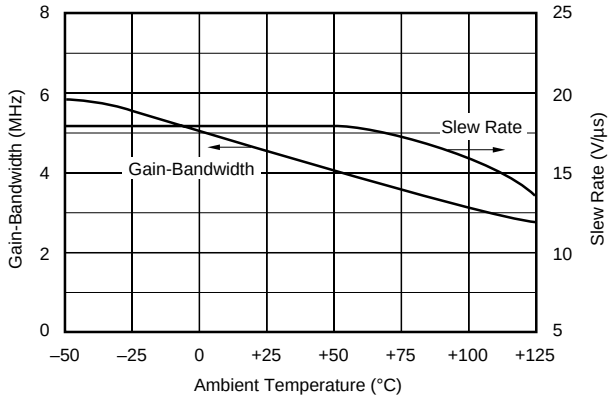
OPEN-LOOP FREQUENCY RESPONSE



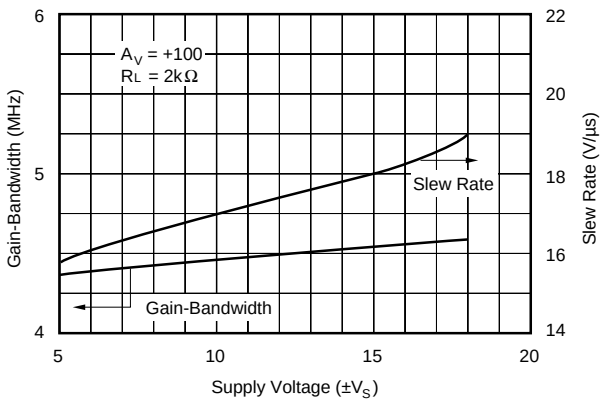
MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY



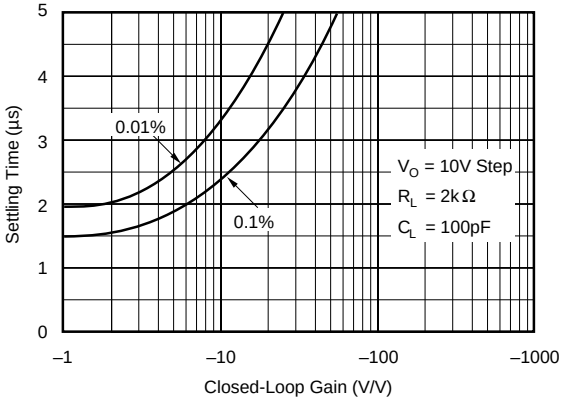
GAIN-BANDWIDTH AND SLEW RATE vs TEMPERATURE



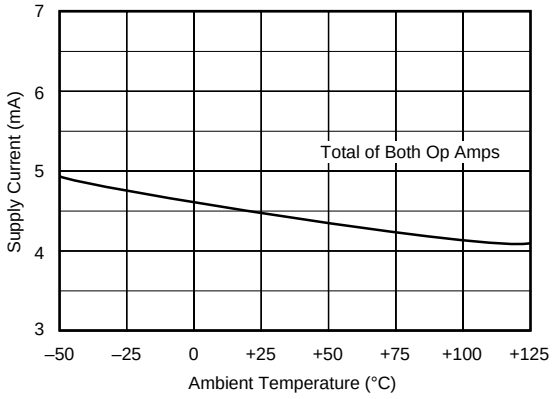
GAIN-BANDWIDTH AND SLEW RATE vs SUPPLY VOLTAGE



SETTLING TIME vs CLOSED-LOOP GAIN



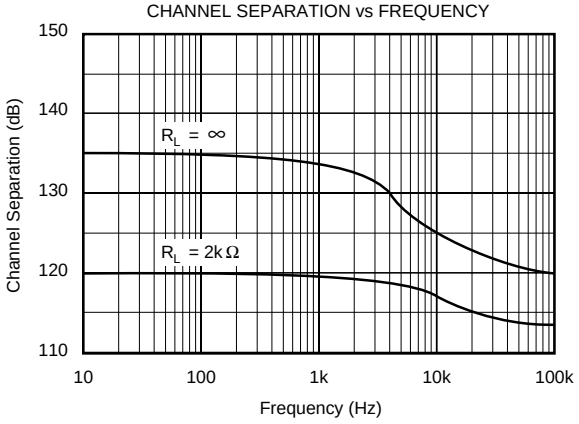
SUPPLY CURRENT vs TEMPERATURE



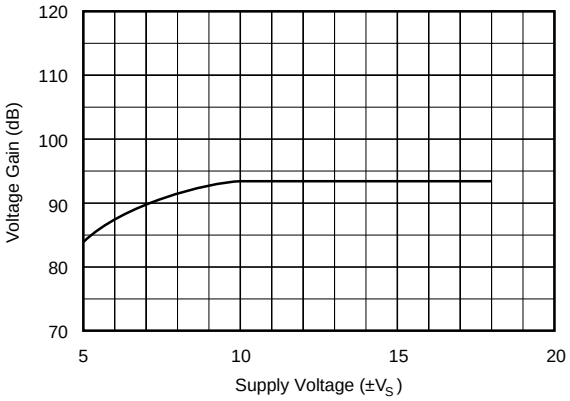
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

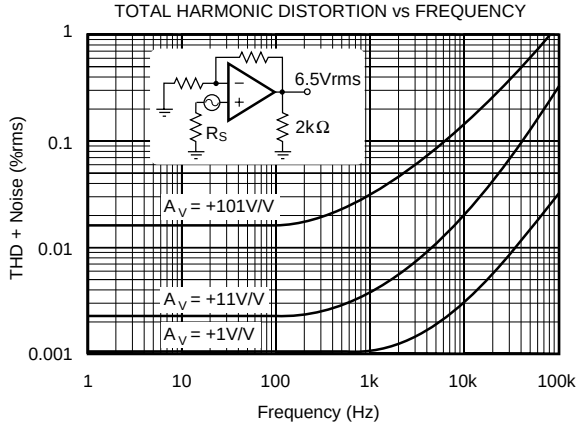
CHANNEL SEPARATION vs FREQUENCY



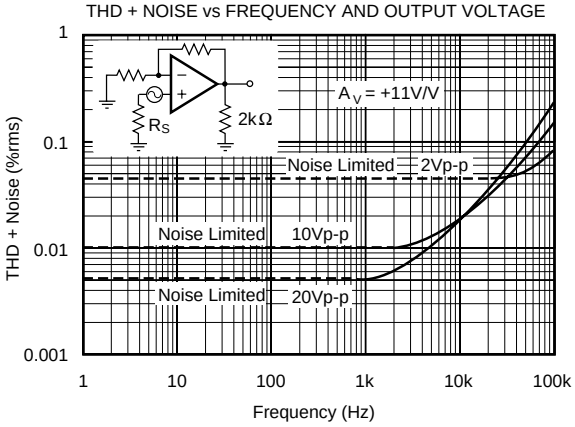
OPEN-LOOP GAIN vs SUPPLY VOLTAGE



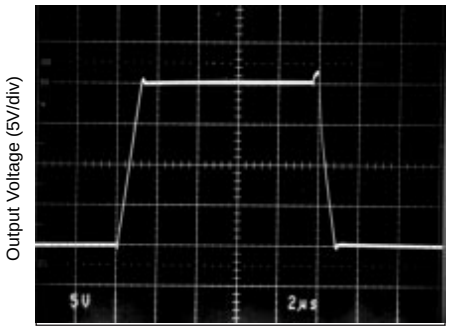
TOTAL HARMONIC DISTORTION vs FREQUENCY



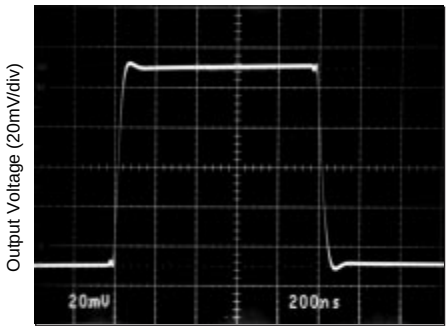
THD + NOISE vs FREQUENCY AND OUTPUT VOLTAGE



OPA2107 LARGE-SIGNAL RESPONSE



OPA2107 SMALL-SIGNAL RESPONSE



APPLICATIONS INFORMATION AND CIRCUITS

The OPA2107 is unity-gain stable and has excellent phase margin. This makes it easy to use in a wide variety of applications.

Power supply connections should be bypassed with capacitors positioned close to the amplifier pins. In most cases, 0.1µF ceramic capacitors are adequate. Applications with larger load currents and fast transient signals may need up to 1µF tantalum bypass capacitors.

INPUT BIAS CURRENT

The OPA2107's ***Difet*** input stages have very low input bias current—an order of magnitude lower than BIFET op amps. Circuit board leakage paths can significantly degrade performance. This is especially evident with the SO-8 surface-mount package where pin-to-pin dimensions are particularly small. Residual soldering flux, dirt, and oils, which conduct leakage current, can be removed by proper cleaning. In most instances a two-step cleaning process is adequate using a clean organic solvent rinse followed by de-ionized water. Each rinse should be followed by a 30-minute bake at 85°C.

A circuit board guard pattern effectively reduces errors due to circuit board leakage (Figure 1). By encircling critical high impedance nodes with a low impedance connection at the same circuit potential, any leakage currents will flow harmlessly to the low impedance node. Guard traces should be placed on all levels of a multiple-layer circuit board.

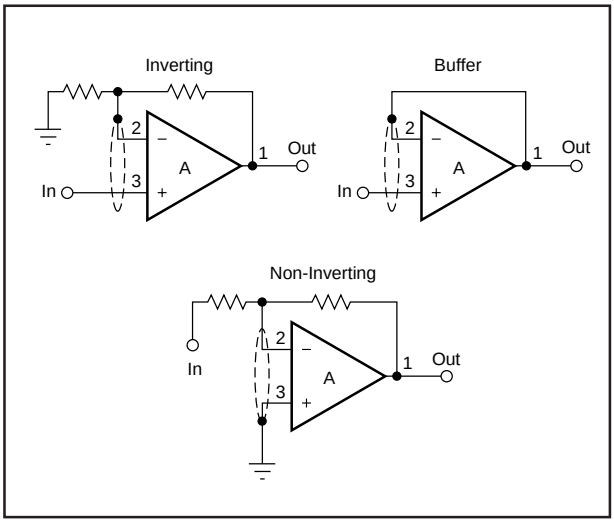


FIGURE 1. Connection of Input Guard.

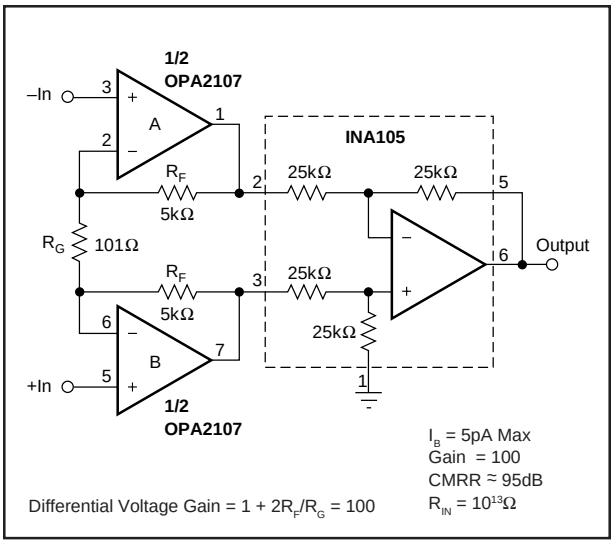


FIGURE 2. FET Input Instrumentation Amplifier.

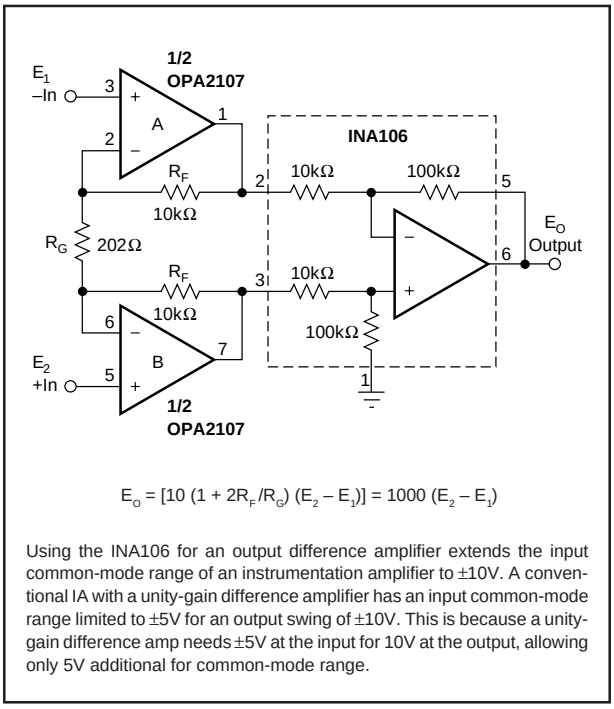


FIGURE 3. Precision Instrumentation Amplifier.