

HM62W256 Series

256 k SRAM (32-kword × 8-bit)

HITACHI

ADE-203-084H (Z)

Rev. 8.0

Nov. 1997

Features

- Low voltage operation SRAM
Operating Supply Voltage: 3.0 V to 3.6 V
- 0.8 μm Hi-CMOS process
- High speed
Access time: 55/70/85 ns (max)
- Low power
Standby: 0.33 μW (typ)
- Completely static memory
No clock or timing strobe required
- Directly LVTTL compatible: All inputs and outputs

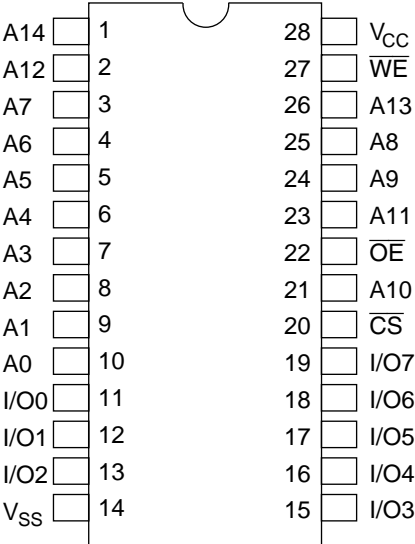
Ordering Information

Type No.	Access Time	Package
HM62W256LFP-7T	70 ns	450 mil 28-pin plastic SOP (FP-28DA)
HM62W256LFP-5SLT	55 ns	
HM62W256LFP-7SLT	70 ns	
HM62W256LFP-8SLT	85 ns	
HM62W256LFP-7ULT	70 ns	8 mm × 14 mm 32-pin TSOP (normal type) (TFP-32DA)
HM62W256LT-7	70 ns	
HM62W256LT-7SL	70 ns	
HM62W256LT-8SL	85 ns	
HM62W256LTM-7	70 ns	8 mm × 13.4 mm 28-pin TSOP (normal type) (TFP-28DA)
HM62W256LTM-5SL	55 ns	
HM62W256LTM-7SL	70 ns	
HM62W256LTM-8SL	85 ns	
HM62W256LTM-7UL	70 ns	

HM62W256 Series

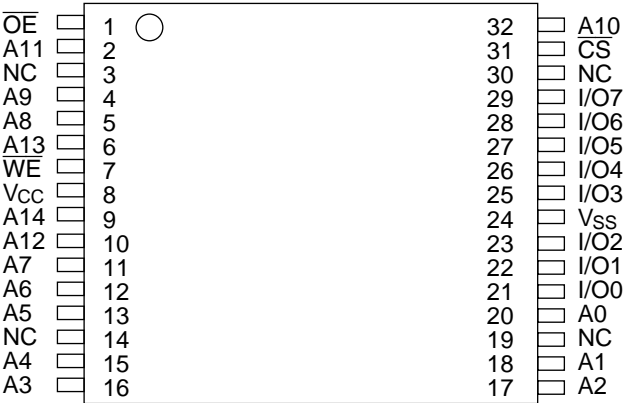
Pin Arrangement

HM62W256LFP Series



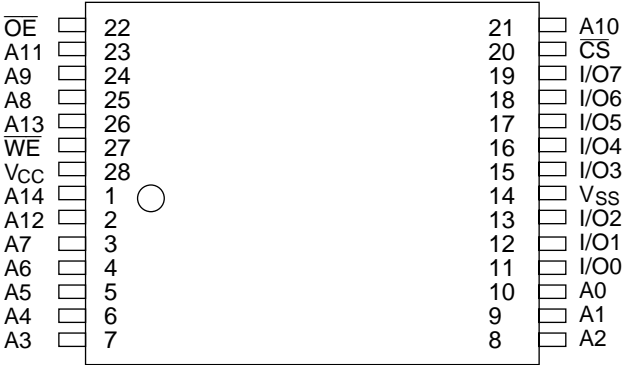
(Top view)

HM62W256LT Series



(Top view)

HM62W256LTM Series

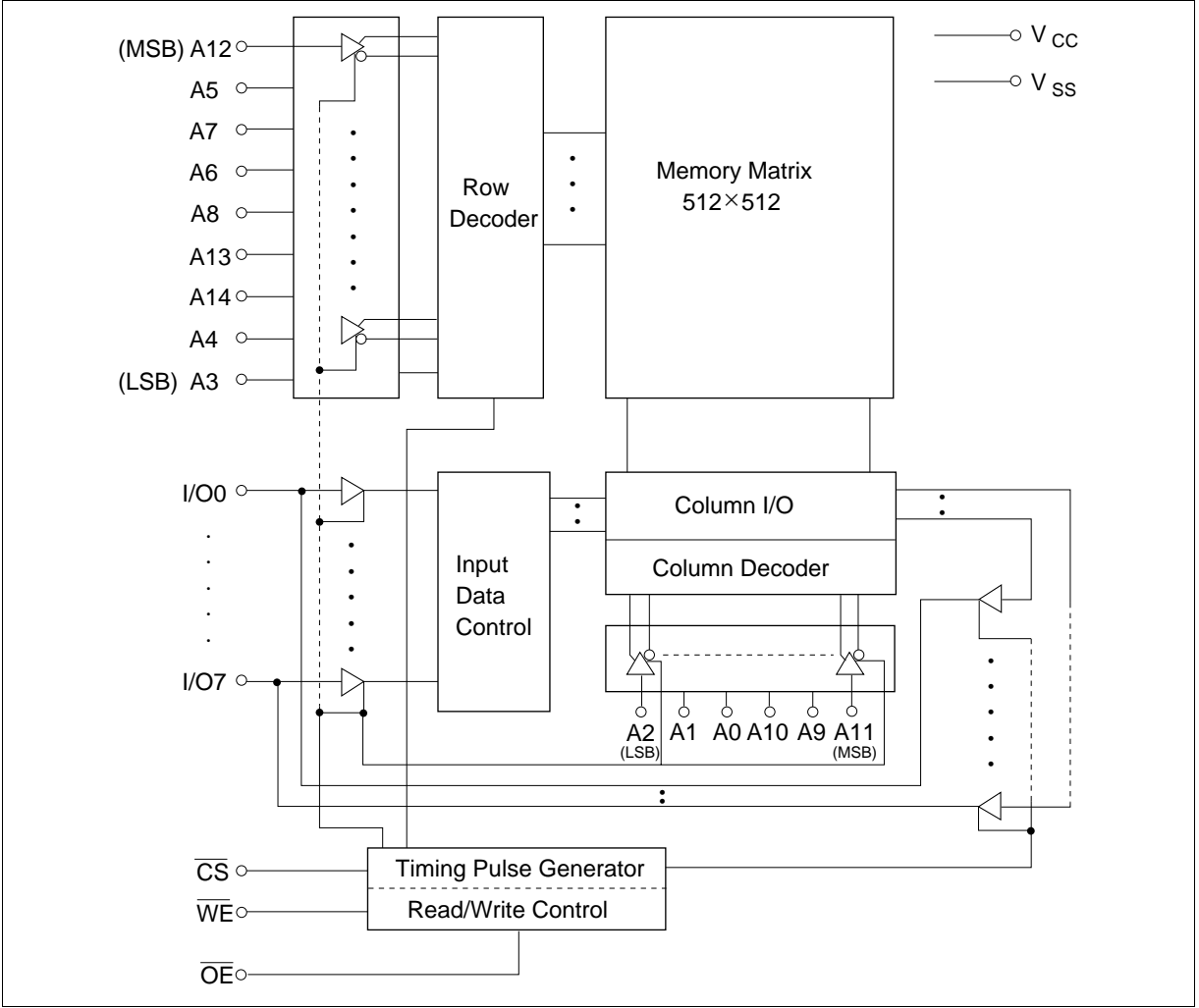


(Top view)

Pin Description

Pin name	Function
A0 – A14	Address inputs
I/O0 – I/O7	Input/output
\overline{CS}	Chip select
\overline{WE}	Write enable
\overline{OE}	Output enable
NC	No connection
V _{CC}	Power supply
V _{SS}	Ground

Block Diagram



Function Table

WE	CS	OE	Mode	V _{CC} Current	I/O Pin	Ref. Cycle
X	H	X	Not selected	I _{SB} , I _{SB1}	High-Z	—
H	L	H	Output disable	I _{CC}	High-Z	—
H	L	L	Read	I _{CC}	Dout	Read cycle (1)–(3)
L	L	H	Write	I _{CC}	Din	Write cycle (1)
L	L	L	Write	I _{CC}	Din	Write cycle (2)

Note: X: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage ^{*1}	V _{CC}	−0.5 to 4.6	V
Terminal voltage ^{*1}	V _T	−0.5 ^{*2} to V _{CC} + 0.5 ^{*3}	V
Power dissipation	P _T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C
Storage temperature under bias	Tbias	−10 to +85	°C

- Notes: 1. Relative to V_{SS}
2. V_T min: −3.0 V for pulse half-width ≤ 50 ns
3. Maximum voltage is 4.6 V

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	3.0	3.3	3.6	V
	V _{SS}	0	0	0	V
Input high(logic 1) voltage	V _{IH}	2.0	—	V _{CC} +0.3	V
Input low(logic 0) voltage	V _{IL}	−0.3 ^{*1}	—	0.8	V

Note: 1. V_{IL} min: −3.0 V for pulse half-width ≤ 50 ns

DC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Min	Typ ^{*1}	Max	Unit	Test conditions
Input leakage current	$ I_{LI} $	—	—	1	μA	V_{SS} V_{in} V_{CC}
Output leakage current	$ I_{LO} $	—	—	1	μA	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$, V_{SS} V_{IO} V_{CC}
Operating power supply current (DC)	I_{CCDC1}	—	—	15	mA	$\overline{CS} = V_{IL}$, others = V_{IH}/V_{IL} $I_{IO} = 0\text{ mA}$
	I_{CCDC2}	—	—	10	mA	$\overline{CS} \leq 0.2\text{ V}$, $V_{IH} \geq V_{CC} - 0.2\text{ V}$, $V_{IL} \leq 0.2\text{ V}$, $I_{IO} = 0\text{ mA}$
Average operating power supply current	HM62W256-5 I_{CCAC1}	—	—	30	mA	min cycle, duty = 100 %, $\overline{CS} = V_{IL}$, others = V_{IH}/V_{IL} $I_{IO} = 0\text{ mA}$
	HM62W256-7 I_{CCAC1}	—	—	30		
	HM62W256-8 I_{CCAC1}	—	—	27		
	I_{CCAC2}	—	—	15	mA	Cycle time 1 μs , duty = 100% $I_{IO} = 0\text{ mA}$, $\overline{CS} \leq 0.2\text{ V}$, $V_{IH} \geq V_{CC} - 0.2\text{ V}$, $V_{IL} \leq 0.2\text{ V}$
Standby power supply current	I_{SB}	—	0.1	1	mA	$\overline{CS} = V_{IH}$
	I_{SB1}	—	0.1	50	μA	$V_{in} \geq 0\text{ V}$, $\overline{CS} \geq V_{CC} - 0.2\text{ V}$,
		—	0.1	10^{-2}		
		—	0.1	5^{-3}		
Output low voltage	V_{OL}	—	—	0.4	V	$I_{OL} = 2.0\text{ mA}$
		—	—	0.2	V	$I_{OL} = 100\text{ }\mu\text{A}$
Output high voltage	V_{OH}	$V_{CC} - 0.2$	—	—	V	$I_{OH} = -100\text{ }\mu\text{A}$
		2.4	—	—	V	$I_{OH} = -2.0\text{ mA}$

Notes: 1. Typical values are at $V_{CC} = 3.3\text{ V}$, $T_a = +25^\circ\text{C}$ and not guaranteed.

2. This characteristic is guaranteed only for L-SL version.

3. This characteristic is guaranteed only for L-UL version.

Capacitance ($T_a = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$)

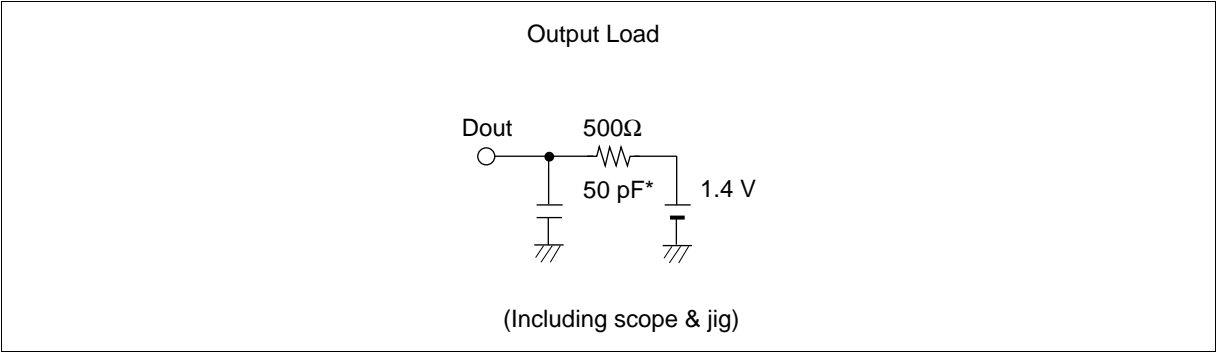
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance ^{*1}	C_{in}	—	—	5	pF	$V_{in} = 0\text{ V}$
Input/output capacitance ^{*1}	C_{IO}	—	—	8	pF	$V_{IO} = 0\text{ V}$

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, VCC = 3.3 V ± 0.3 V, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0.4 V to 2.4 V
- Input rise and fall time: 5 ns
- Input reference level: 1.4 V
- Output timing reference level: HM62W256-5: 1.4 V
HM62W256-7/8: 0.8 V/2.0 V



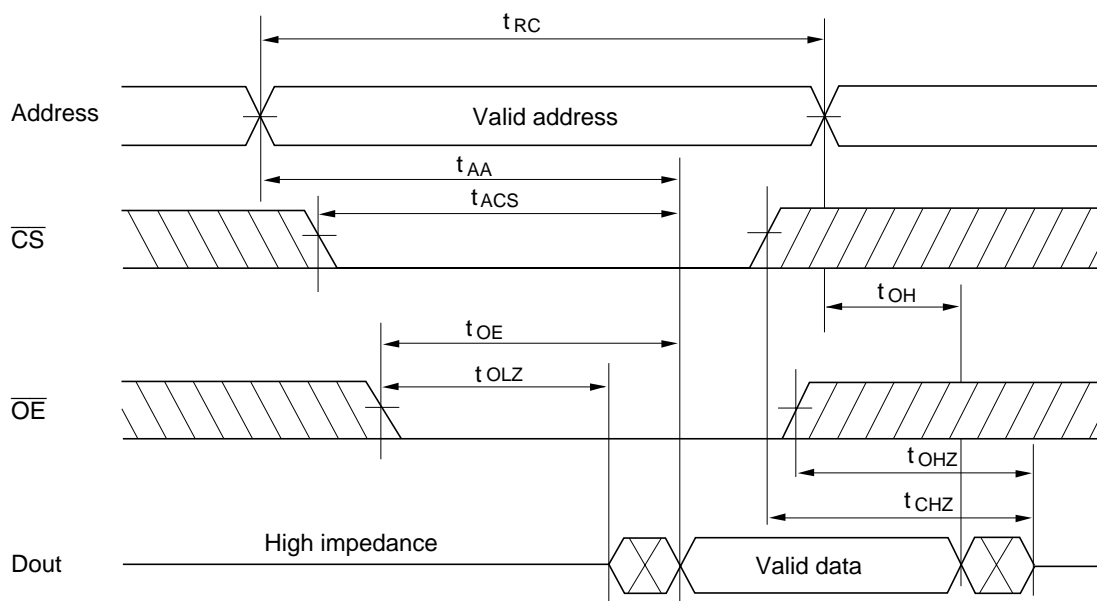
Read Cycle

HM62W256									
Parameter	Symbol	-5		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read cycle time	t _{RC}	55	—	70	—	85	—	ns	
Address access time	t _{AA}	—	55	—	70	—	85	ns	
Chip select access time	t _{ACS}	—	55	—	70	—	85	ns	
Output enable to output valid	t _{OE}	—	30	—	35	—	45	ns	
Chip selection to output in low-Z	t _{CLZ}	5	—	10	—	10	—	ns	2
Output enable to output in low-Z	t _{OLZ}	5	—	5	—	5	—	ns	2
Chip deselection to output in high-Z	t _{CHZ}	0	20	0	25	0	30	ns	1, 2
Output disable to output in high-Z	t _{OHZ}	0	20	0	25	0	30	ns	1, 2
Output hold from address change	t _{OH}	10	—	10	—	10	—	ns	

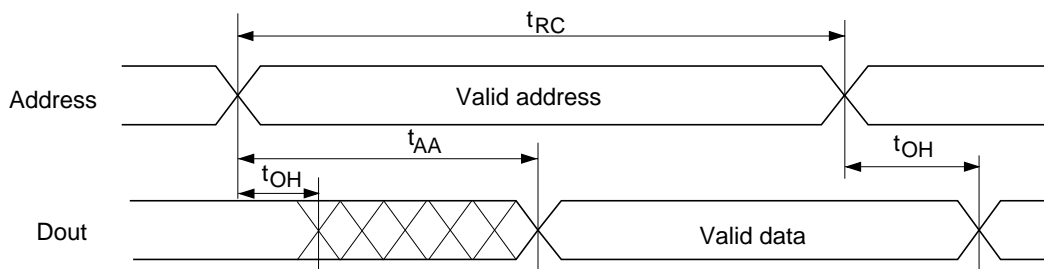
Notes: 1. t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.

2. This parameter is sampled and not 100% tested.

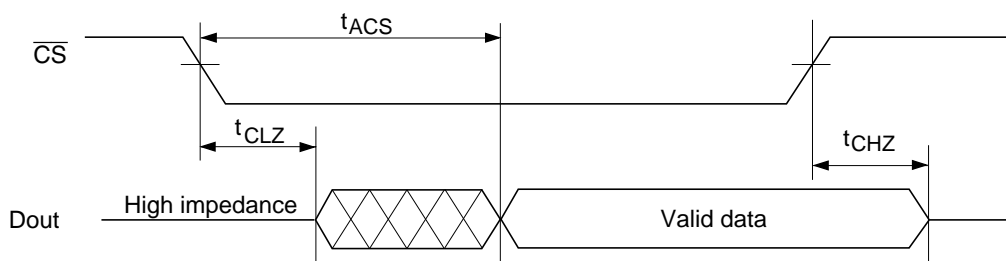
Read Timing Waveform (1) ($\overline{WE} = V_{IH}$)



Read Timing Waveform (2) ($\overline{WE} = V_{IH}$, $\overline{CS} = V_{IL}$, $\overline{OE} = V_{IL}$)



Read Timing Waveform (3) ($\overline{WE} = V_{IH}$, $\overline{OE} = V_{IL}$)*1



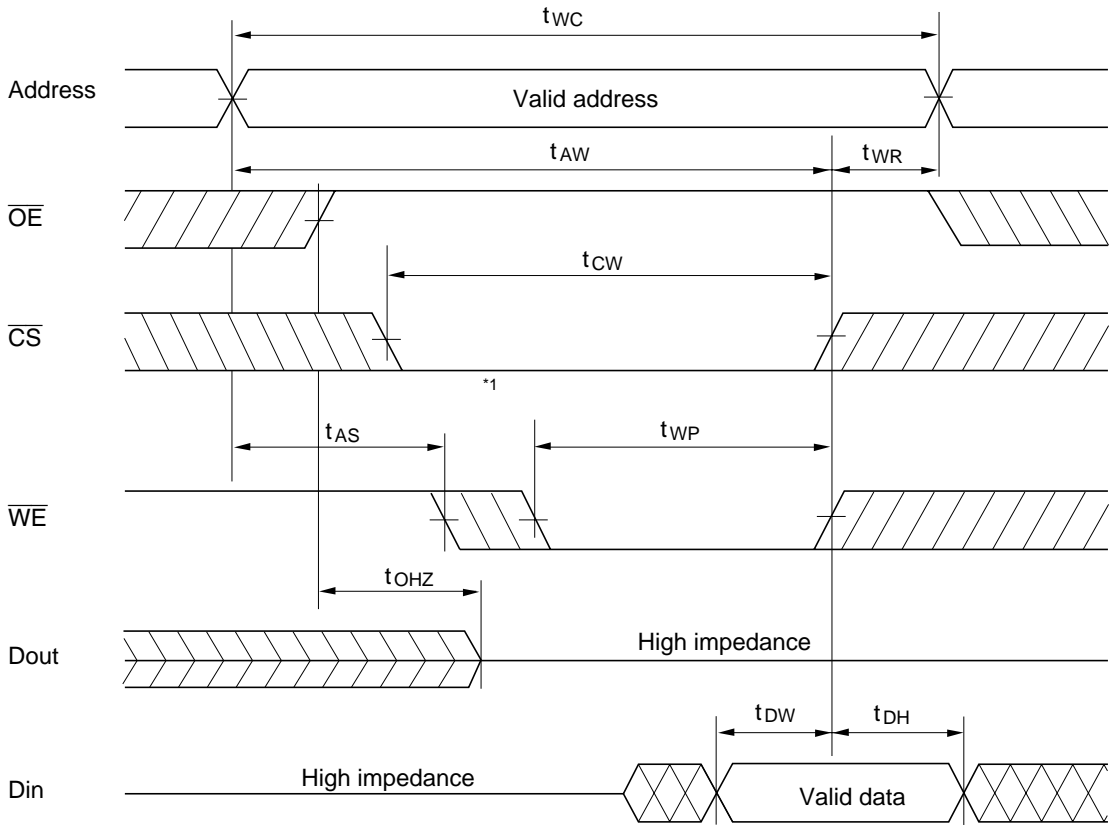
Note: 1. Address must be valid prior to or simultaneously with \overline{CS} going low.

Write Cycle

		HM62W256							
		-5		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Write cycle time	t _{WC}	55	—	70	—	85	—	ns	
Chip selection to end of write	t _{CW}	45	—	60	—	75	—	ns	4
Address setup time	t _{AS}	0	—	0	—	0	—	ns	5
Address valid to end of write	t _{AW}	45	—	60	—	75	—	ns	
Write pulse width	t _{WP}	40	—	50	—	55	—	ns	3, 8
Write recovery time	t _{WR}	0	—	0	—	0	—	ns	6
Write to output in high-Z	t _{WHZ}	0	25	0	25	0	30	ns	1, 2, 7
Data to write time overlap	t _{DW}	30	—	30	—	35	—	ns	
Data hold from write time	t _{DH}	0	—	0	—	0	—	ns	
Output active from end of write	t _{OW}	10	—	10	—	10	—	ns	2
Output disable to output in high-Z	t _{OHZ}	0	20	0	25	0	30	ns	1, 2, 7

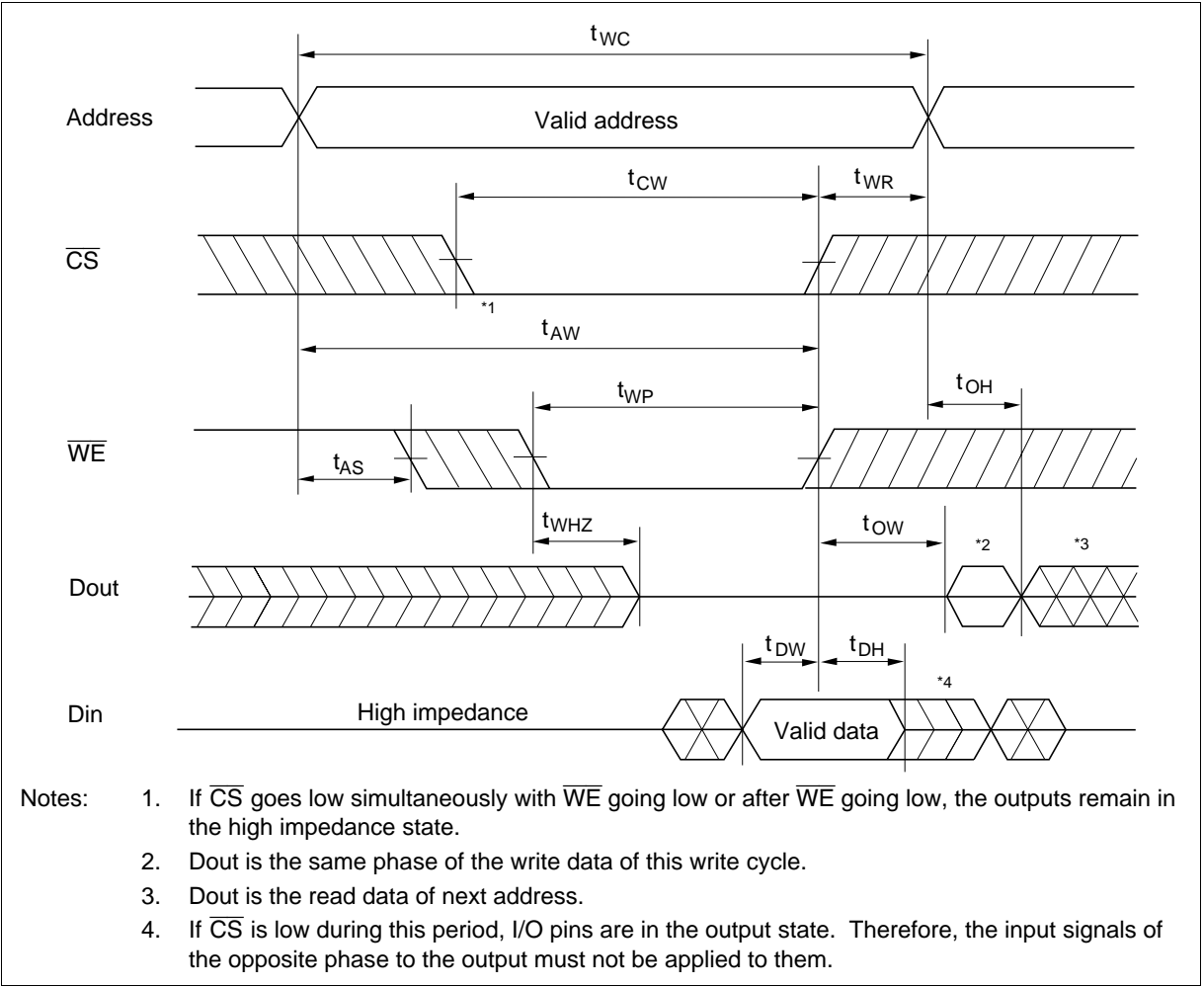
- Notes:
- t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
 - This parameter is samples and not 100% tested.
 - A write occurs during the overlap (t_{WP}) of a low \overline{CS} and a low \overline{WE} . A write begins at the later transition of \overline{CS} going low or \overline{WE} going low. A write ends at the earlier transition of \overline{CS} going high or \overline{WE} going high. t_{WP} is measured from the beginning of write to the end of write.
 - t_{CW} is measured from \overline{CS} going low to the end of write.
 - t_{AS} is measured from the address valid to the beginning of write.
 - t_{WR} is measured from the earlier of \overline{WE} or \overline{CS} going high to the end of write cycle.
 - During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.
 - In the write cycle with \overline{OE} low fixed, t_{WP} must satisfy the following equation to avoid a problem of data bus contention, t_{WP} t_{WHZ} max + t_{DW} min.

Write Timing Waveform (1) ($\overline{\text{OE}}$ Clock)



- Notes:
1. If $\overline{\text{CS}}$ goes low simultaneously with $\overline{\text{WE}}$ going low or after $\overline{\text{WE}}$ going low, the outputs remain in the high impedance state.

Write Timing Waveform (2) ($\overline{\text{OE}}$ Low Fixed)

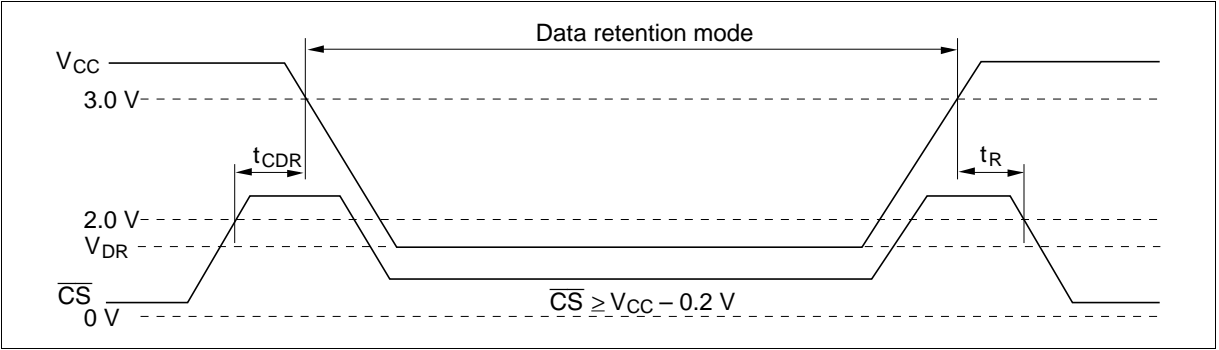


Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ ^{*1}	Max	Unit	Test conditions ^{*6}
V _{CC} for data retention	V _{DR}	2.0	—	3.6	V	$\overline{CS} \geq V_{CC} - 0.2\text{ V}$, Vin ≥ 0 V
Data retention current	I _{CDDR}	—	0.05	30 ^{*2}	μA	$V_{CC} = 3.0\text{ V}$, Vin ≥ 0 V $\overline{CS} \geq V_{CC} - 0.2\text{ V}$,
		—	0.05	8 ^{*3}		
		—	0.05	3 ^{*4}		
Chip deselect to data retention time	t _{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t _R	t _{RC} ^{*5}	—	—	ns	

- Notes: 1. Typical values are at V_{CC} = 3.0 V, Ta = 25°C and not guaranteed.
2. 10 μA max. at Ta = 0 to +40°C.
3. This characteristics guaranteed for only L-SL version. 2.5 μA max. at Ta = 0 to +40°C.
4. This characteristics guaranteed for only L-UL version. 0.6 μA max. at Ta = 0 to +40°C.
5. t_{RC} = read cycle time.
6. \overline{CS} controls address buffer, \overline{WE} buffer, \overline{OE} buffer, and Din buffer. If \overline{CS} controls data retention mode, other input levels (address, \overline{WE} , \overline{OE} , I/O) can be in the high impedance state.

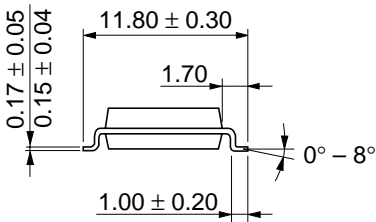
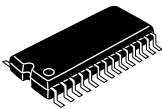
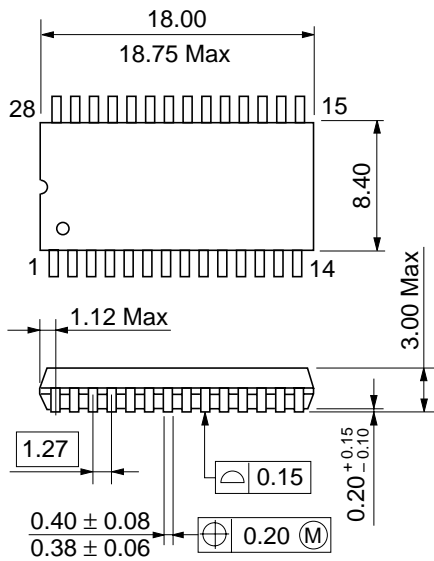
Low V_{CC} Data Retention Timing Waveform



Package Dimensions

HM62W256LFP Series (FP-28DA)

Unit: mm



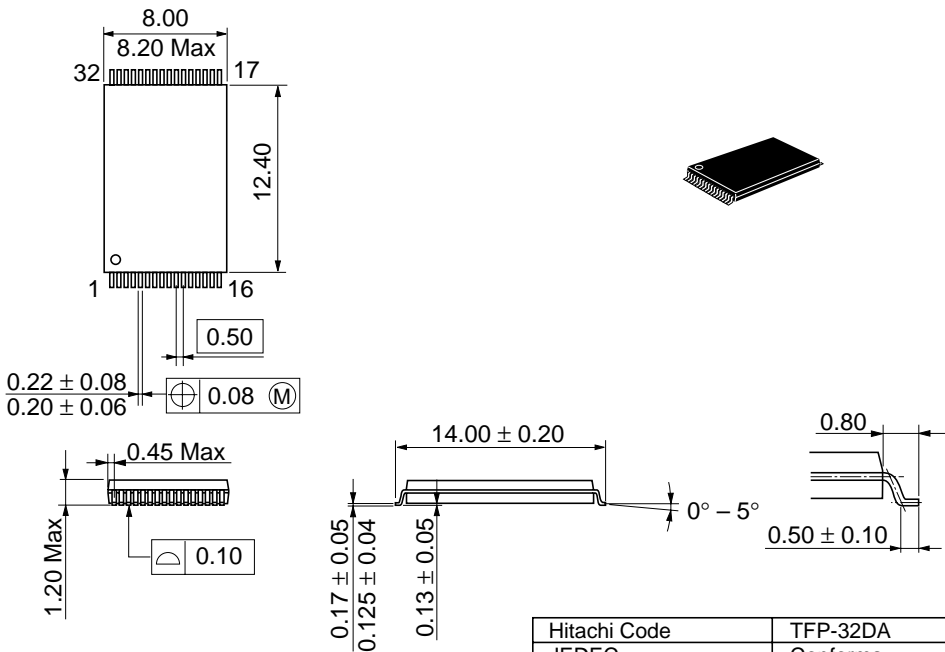
Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-28DA
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.82 g

Package Dimensions

HM62W256LT Series (TFP-32DA)

Unit: mm



Dimension including the plating thickness
Base material dimension

Hitachi Code	TFP-32DA
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.26 g

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HITACHI

Hitachi, Ltd.

Semiconductor & IC Div.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100, Japan
Tel: Tokyo (03) 3270-2111
Fax: (03) 3270-5109

For further information write to:

Hitachi Semiconductor
(America) Inc.
2000 Sierra Point Parkway
Brisbane, CA. 94005-1897
U S A
Tel: 800-285-1601
Fax: 303-297-0447

Hitachi Europe GmbH
Continental Europe
Dornacher Straße 3
D-85622 Feldkirchen
München
Tel: 089-9 91 80-0
Fax: 089-9 29 30-00

Hitachi Europe Ltd.
Electronic Components Div.
Northern Europe Headquarters
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA
United Kingdom
Tel: 01628-585000
Fax: 01628-585160

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia (Hong Kong) Ltd.
Unit 706, North Tower,
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon
Hong Kong
Tel: 27359218
Fax: 27306071

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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Mar. 27, 1992	Initial issue	Y. Saito	Y. Kawashima
1.0	Dec. 20, 1992	Full specification	Y. Saito	Y. Kawashima
2.0	Feb. 25, 1993	Addition of HM62W256LT Series	Y. Saito	Y. Kawashima
3.0	Apr. 1, 1993	Operation Supply Voltage: 3.0V – 3.6 V to Single 3.3 V Supply f = 2 MHz to f = 1 MHz Function Table Not selected to Standby Absolute Maximum Rating Relative to V _{CC} to Relative to V _{SS} DC Characteristics I _{CCAC2} Cycle time: 500 ns to 1 μs Low V _{CC} Data Retention Timing Waveforms Change of Notes	K. Imato	T. Matumoto
4.0	Sep. 10, 1993	Absolute Maximum Rating V _T = –0.5 to V _{CC} + 0.5 V to –0.5 to V _{CC} + 0.3 V DC Characteristics I _{CCDC1} (max): 5.0 mA to 15 mA I _{CCDC2} (max): 2.5 mA to 10 mA AC Characteristics tDW (min): 30/40 ns to 30/35 ns Addition of notes for Low V _{CC} Data retention Timing Waveform	Y. Saito	K. Yoshizaki
5.0	Mar. 18, 1994	DC Characteristics I _{CCAC2} (max): 10 mA to 15 mA	Y. Saito	K. Yashizaki
6.0	Oct. 31, 1994	Addition of HM62W256LTM Series (TFP-28DA) Addition of Block Diagram AC Characteristics Addition of note 12 Low V _{CC} data retention characteristics I _{CCDR} (typ): —/— μA to 0.2/0.2 μA Note 2: 20 μA max at Ta = 0 to 40°C to 10 μA max at Ta = 0 to 40°C	Y. Saito	K. Yoshizaki
7.0	Jun. 19, 1995	Feature Low power (standby): 0.66 μW to 0.33 μW Deletion of HM62W256LFP-8T Deletion of HM62W256LT-8 Deletion of HM62W256LTM-8 Addition of HM62W256LFP-5SLT/7ULT Addition of HM62W256LTM-5SLT/7ULT Chage of Block Diagram Absolute maximum Ratings Terminal voltage V _T : –0.5 to V _{CC} + 0.3 V to –0.5 to V _{CC} + 0.5 V	M. Higuchi	K. Yoshizaki

Revision Record (cont)

Rev.	Date	Contents of Modification	Drawn by	Approved by
7.0	Jun. 19, 1995	DC Characteristics Addition of note 3. I_{CCAC1} (max): 30/27 mA to 30/30/27 mA I_{SB1} (typ): 0.2/0.2/ μ A to 0.1/0.1/0.1 μ A I_{SB1} (max): 50/10 μ A to 50/10/5 μ A Capacitance C_{in} (max): 8 pF to 5 pF C_{IO} (max): 10 pF to 8 pF AC Characteristics Addition of Output timing reference level: HM62W256-5: 1.4 V Change order of notes t_{RC} (min): 70/85 ns to 55/70/85 ns t_{AA} (max): 70/85 ns to 55/70/85 ns t_{ACS} (max): 70/85 ns to 55/70/85 ns t_{OE} (max): 35/45 ns to 30/35/45 ns t_{CLZ} (min): 10/10 ns to 5/10/10 ns t_{OLZ} (min): 5/5 ns to 5/5/5 ns t_{CHZ} (max): 25/30 ns to 20/25/30 ns t_{OHZ} (max): 25/30 ns to 20/25/30 ns t_{OH} (min): 10/10 ns to 10/10/10 ns t_{WC} (min): 70/85 ns to 55/70/85 ns t_{CW} (min): 60/75 ns to 45/60/75 ns t_{AW} (min): 60/75 ns to 45/60/75 ns t_{WP} (min): 50/55 ns to 40/50/55 ns t_{WHZ} (max): 25/30 ns to 25/25/30 ns t_{DW} (min): 30/35 ns to 30/30/35 ns t_{OW} (min): 10/10 ns to 10/10/10 ns Low VCC Data Retention Characteristics I_{CCDR} (typ): 0.2/0.2 μ A to 0.05/0.05/0.05 μ A I_{CCDR} (max): 30/8 μ A to 30/8/3 μ A	M. Higuchi	K. Yoshizaki
8.0	Nov. 1997	Change of Format Change of Subtitle		