MC100EPT21

Differential LVPECL to LVTTL Translator

The MC100EPT21 is a Differential LVPECL to LVTTL translator. Because LVPECL (Positive ECL) levels are used only +3.3V and ground are required. The small outline 8–lead SOIC package makes the EPT21 ideal for applications which require the translation of a clock or data signal.

The VBB output allows the EPT21 to also be used in a single–ended input mode. In this mode the VBB output is tied to the $\overline{D0}$ input for a non–inverting buffer or the D0 input for an inverting buffer. If used, the VBB pin should be bypassed to ground via a 0.01µF capacitator.

- 1.4ns Typical Propagation Delay
- 275MHz Fmax (Clock bit stream, not pseudo–random)
- Differential LVPECL inputs
- Small Outline SOIC Package
- 24mA TTL outputs
- Flow Through Pinouts
- Internal Input Resistors: Pulldown on D, Pulldown and Pullup on $\overline{D}$
- Q Output will default LOW with inputs open or at GND
- ESD Protection: >1500V HBM, >100V MM
- V_{BB} Output
- New Differential Input Common Mode Range
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack. For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
- Transistor Count = 81 devices

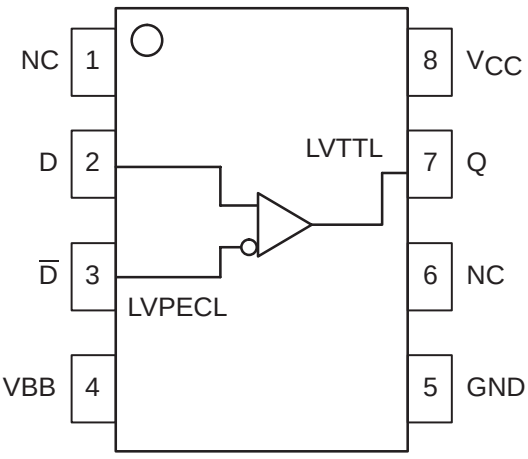
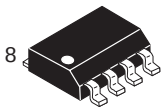


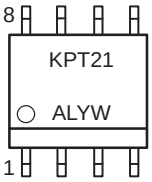
Figure 1. 8–Lead Pinout (Top View) **and Logic Diagram**

ON Semiconductor
Formerly a Division of Motorola
http://onsemi.com



SO–8
D SUFFIX
CASE 751

MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

PIN DESCRIPTION	
PIN	**FUNCTION**
Q	LVTTL Output
D, $\overline{D}$	Differential LVPECL Input Pair
V_{CC}	Positive Supply
V_{BB}	Output Reference Voltage
GND	Ground

ORDERING INFORMATION

Device	Package	Shipping
MC100EPT21D	SOIC	98 Units/Rail
MC100EPT21DR2	SOIC	2500 Tape & Reel

© Semiconductor Components Industries, LLC, 1999

okDatasheet.com - Free Datasheet Search Engine

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply (GND = 0V)	0 to 3.8	VDC
V_I	Input Voltage (GND = 0V, V_I not more positive than V_{CC})	0 to 3.8	VDC
I_{out}	Output Current — Continuous Surge	50 100	mA
I_{BB}	V_{BB} Sink/Source Current†	± 0.5	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature	–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) — Still Air 500lfpm	190 130	°C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	41 to 44 ± 5%	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

† Use for inputs of same package only.

DC CHARACTERISTICS (V_{CC} = 3.3V ± 0.3V; GND = 0V; T_A = –40°C to 85°C)

Symbol	Characteristic	Min	Typ	Max	Unit
I_{CCH}	Power Supply Current (Outputs set to HIGH)	5.0	12	20	mA
I_{CCL}	Power Supply Current (Outputs set to LOW)	8.0	18	26	mA
V_{IH}	Input HIGH Voltage (V_{CC} = 3.3) (Note 1.)	2135		2420	mV
V_{IL}	Input LOW Voltage (V_{CC} = 3.3) (Note 1.)	1490		1825	mV
I_{IH}	Input HIGH Current			150	µA
I_{IL}	Input LOW Current — D $\overline{D}$	 –150		0.5	µA
V_{OH}	Output HIGH Voltage (I_{OH} = –3.0mA) (Note 2.)	2.4			V
V_{OL}	Output LOW Voltage (I_{OL} = 24mA) (Note 2.)			0.5	V
I_{OS}	Output Short Circuit Current	–130		–80	mA
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 3.)	2.0		3.3	V
V_{BB}	Output Voltage Reference		2.0		V

NOTE: 100EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. All values vary 1:1 with V_{CC}.
2. All loading with 500 ohms to GND, CL = 20pF.
3. V_{IHCMR} min varies 1:1 with GND, max varies 1:1 with V_{CC}.

AC CHARACTERISTICS (V_{CC} = 3.3V ± 0.3V; GND = 0V)

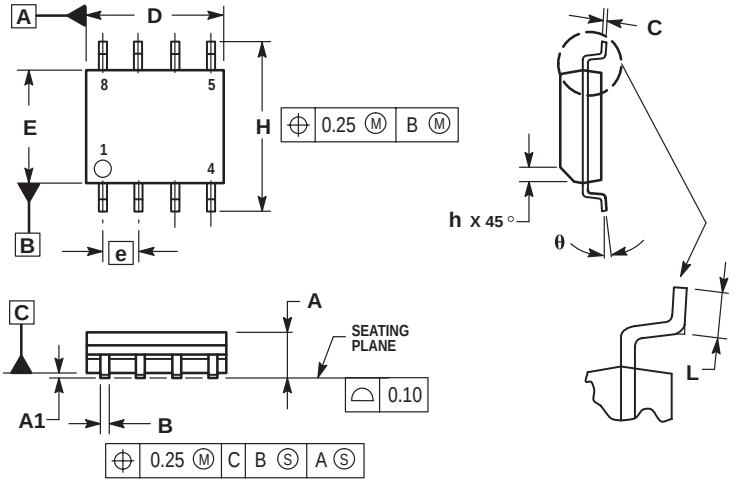
		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{max}	Maximum Toggle Frequency (Note 4.)	275	350		275	350		275	350		MHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential	1000 1000	1450 1400	1800 1800	1000 1000	1450 1400	1800 1800	1000 1000	1450 1400	1900 1900	ps
t_{SK++} t_{SK--} t_{SKPP}	Output–to–Output Skew++ Output–to–Output Skew– – Part–to–Part Skew (Note 5.)		60 25 500			60 25 500			60 25 500		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Voltage Swing (Diff.)	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Times (0.8V – 2.0V) — Q, $\overline{Q}$	330	500	900	330	500	900	330	500	900	ps

4. F_{max} guaranteed for functionality only. V_{OL} and V_{OH} levels are guaranteed at DC only.
5. Skews are measured between outputs under identical transitions.

okDatasheet.com - Free Datasheet Search Engine

PACKAGE DIMENSIONS

SO–8
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751–06
ISSUE T



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

okDatasheet.com - Free Datasheet Search Engine

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

PUBLICATION ORDERING INFORMATION

USA/EUROPE Literature Fulfillment:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303–675–2175 or 800–344–3860 Toll Free USA/Canada
Fax: 303–675–2176 or 800–344–3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com

Fax Response Line*: 303–675–2167
800–344–3810 Toll Free USA/Canada
*To receive a Fax of our publications

N. America Technical Support: 800–282–9855 Toll Free USA/Canada

ASIA/PACIFIC: LDC for ON Semiconductor – Asia Support
Phone: 303–675–2121 (Tue–Fri 9:00am to 1:00pm, Hong Kong Time)
Email: ONlit–asia@hibbertco.com

JAPAN: ON Semiconductor, Japan Customer Focus Center
4–32–1 Nishi–Gotanda, Shinagawa–ku, Tokyo, Japan 141–8549
Phone: 81–3–5487–8345
Email: r14153@onsemi.com

ON Semiconductor Website: http://onsemi.com

For additional information, please contact your local Sales Representative.

okDatasheet.com - Free Datasheet Search Engine