ICs for Communications

DUAL CHANNEL SLICOFI-2, SLIC
DuSLIC

PEB 3265 Version 1.1
PEB 4265 Version 1.1
PEB 4266 Version 1.1

Preliminary Product Overview 10.99

DS 1

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Table of Contents **Page**

Table of Contents **Page**

List of Figures

List of Figures

Page

Preface

The DuSLIC chip set consists of a programmable dual channel SLICOFI®-2 CODEC and two single channel high-voltage SLIC chips.

Organization of this Document

This Preliminary Product Overview is divided into six chapters. It is organized as follows:

- Chapter 1, Overview
  A general description of the product, list of its key features and some typical applications.

- Chapter 2, Functional Description
  The main functions are presented following a functional block diagram.

- Chapter 3, Operational Description
  A brief description of the three operating modes: power down, active and ringing (plus signal monitoring techniques).

- Chapter 4, Interfaces
  Connection information including standard IOM®-2 and PCM interface timing frames and pins.

- Chapter 5, Electrical Characteristics
  Parameters, symbols and limit values.

- Chapter 6, Application Circuits
  Illustrations of balanced ringing, unbalanced ringing and protection circuits.

1 Overview

DuSLIC is a chip set, comprising one dual channel SLICOFI-2 CODEC and two single-channel SLIC chips. It is a highly flexible CODEC/SLIC solution for an analog line circuit and is widely programmable. Users can now access different markets with a single hardware design that meets all different standards worldwide.
The interconnections between the single channel high-voltage SLIC (170 V process) and the dual channel SLICOFI-2 CODEC (advanced CMOS process) are a seamless fit. This guarantees maximum transmission performance with a minimum of necessary components.

Currently there are three DuSLIC chip sets available:
DuSLIC-S (Standard), DuSLIC-E (Extended) and DuSLIC-P (Power Management). Optimized for different applications the main differences are in ringing features, power management and additional functions like DTMF recognition, Caller ID generation or Universal Tone Detection (UTD).
For DuSLIC-E and DuSLIC-S additionally the different performance versions DuSLIC-E2 and DuSLIC-S2 are available.
This document describes the DuSLIC-E and DuSLIC-P chip sets. For the other chip sets see our "DuSLIC Chip Set Selection Guide".

All line circuit functions are implemented on the chip set:

- BORSCHT functions
- Max. 85 V_{RMS} sinusoidal ringing generation
- Metering by Polarity Reversal and by 12/16 kHz Sinusoidal Bursts
- Dual-Tone Multifrequency (DTMF) detection and generation
- Caller ID generation.
- Universal Tone Detection (UTD) unit for fax-/modemtone detection
- Line Echo Cancellation unit

Integrated battery switches guarantee minimum power consumption during the off-hook, on-hook and ringing modes. Test and diagnosis functions have been integrated to simplify testing. No external test equipment except one relay is needed for either subscriber line testing in the field or board testing during production or in the field.
The employment of SLIC-E or SLIC-P depends on the application. SLIC-E (PEB 4265) is optimized for access network requirements, while the power management SLIC-P (PEB 4266) is an enhanced version for extremely power-sensitive applications or when internal unbalanced ringing is required.

DuSLIC Architecture

Unlike traditional designs, DuSLIC splits the SLIC function into high-voltage SLIC functions and low-voltage SLIC functions.
The low voltage functions are handled in the SLICOFI-2 device. The partitioning of the functions is shown in **Figure 1-1**. For further information see **Chapter 2.2**.

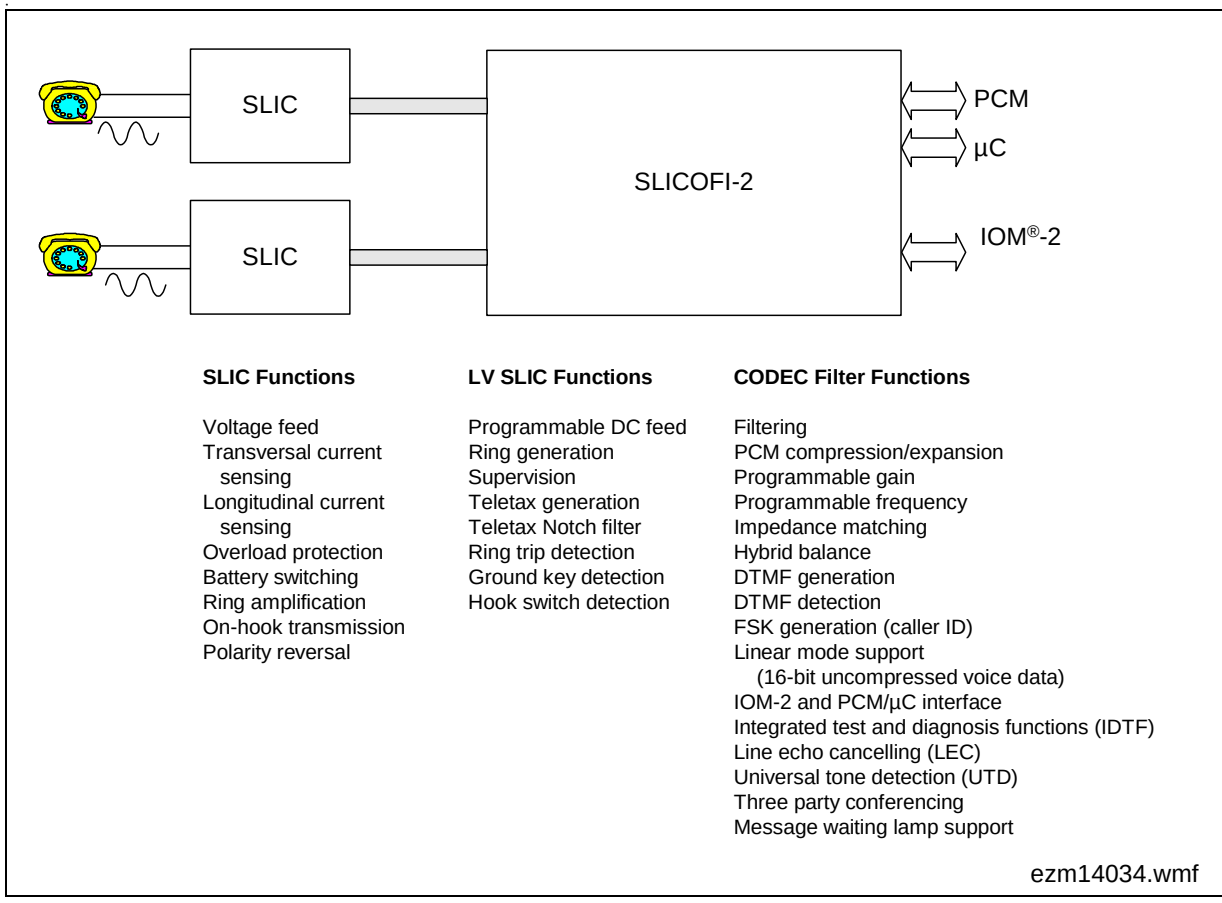


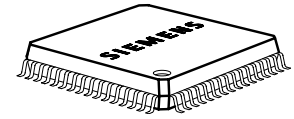
Figure 1-1 DuSLIC-E and DuSLIC-P Chip Set

DUAL CHANNEL SLICOFI-2, SLIC
DuSLIC

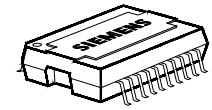
PEB 3265
PEB 4265
PEB 4266

Version 1.0

1.1 Features



P-MQFP-64-1



P-DSO-20-5

- Internal unbalanced/balanced ringing capability up to 50 V_{RMS}/85 V_{RMS}
- Programmable Teletax (TTX) generation
- Programmable battery feed with cabability for driving longer loops
- Fully programmable dual-channel CODEC
- Ground/loop start signaling
- Polarity reversal
- Integrated test and diagnosis functions
- On-hook transmission
- Integrated DTMF generator
- Integrated DTMF decoder
- Integrated caller ID (FSK) generator
- Optimized filter structure for modem transmission
- Integrated Line Echo Cancellation unit
- Integrated fax/modem detection
- Three party conferencing (in PCM/µC mode)
- Message waiting lamp support (PBX)
- Power optimized architecture
- Power Management capability (integrated battery switches)
- 8 and 16 kHz PCM Transmission
- Specification in accordance with
  ITU-T Recommendation Q.552 for Z-interface and applicable LSSGR

Type	Package
PEB 3265 (SLICOFI-2)	P-MQFP-64-1
PEB 4265 (SLIC-E)	P-DSO-20-5
PEB 4266 (SLIC-P)	P-DSO-20-5

1.2 Typical Applications

The Infineon Technologies DuSLIC family is particularily designed for all access network applications but adresses all major telephone applications including:

- Digital Loop Carrier
- Wireless Local Loop
- Fiber in the Loop
- Private Branch Exchange
- Intelligent NT (Network Terminations) for ISDN
- ISDN Terminal Adapters
- Central Office
- Voice over IP

1.3 Logic Symbols

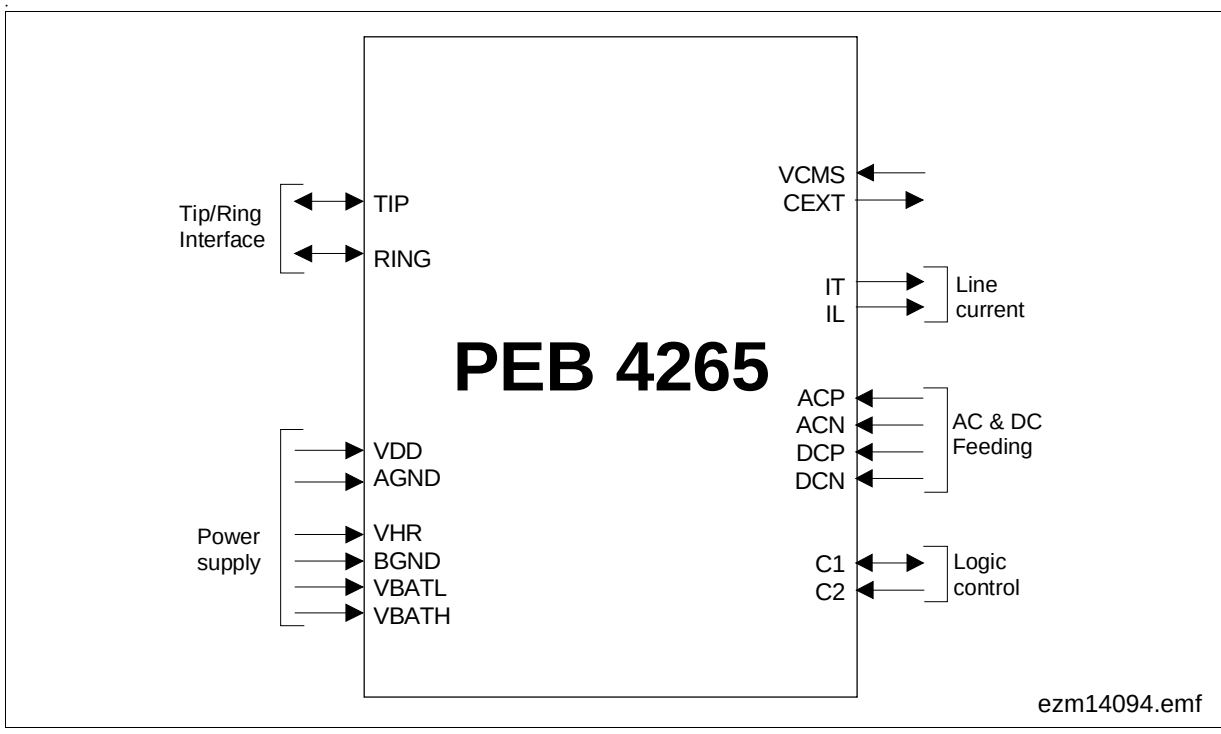


Figure 1-2 Logic Symbol SLIC-E

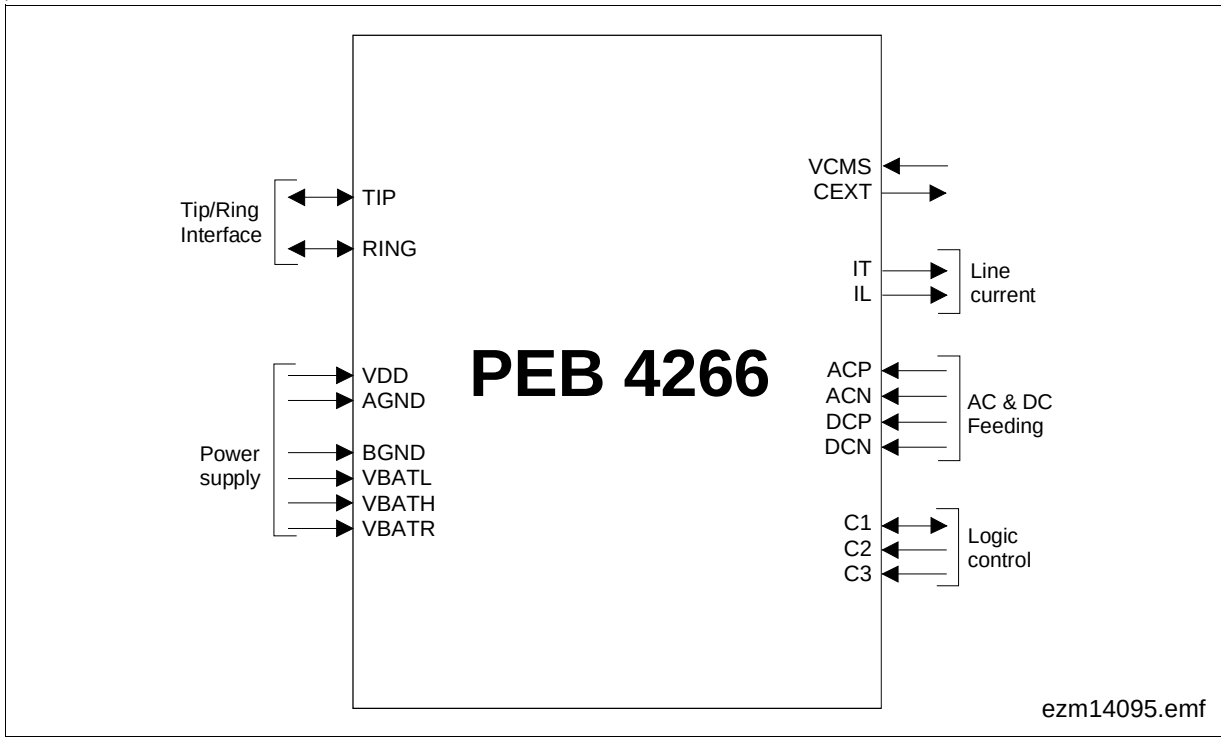


Figure 1-3 Logic Symbol SLIC-P

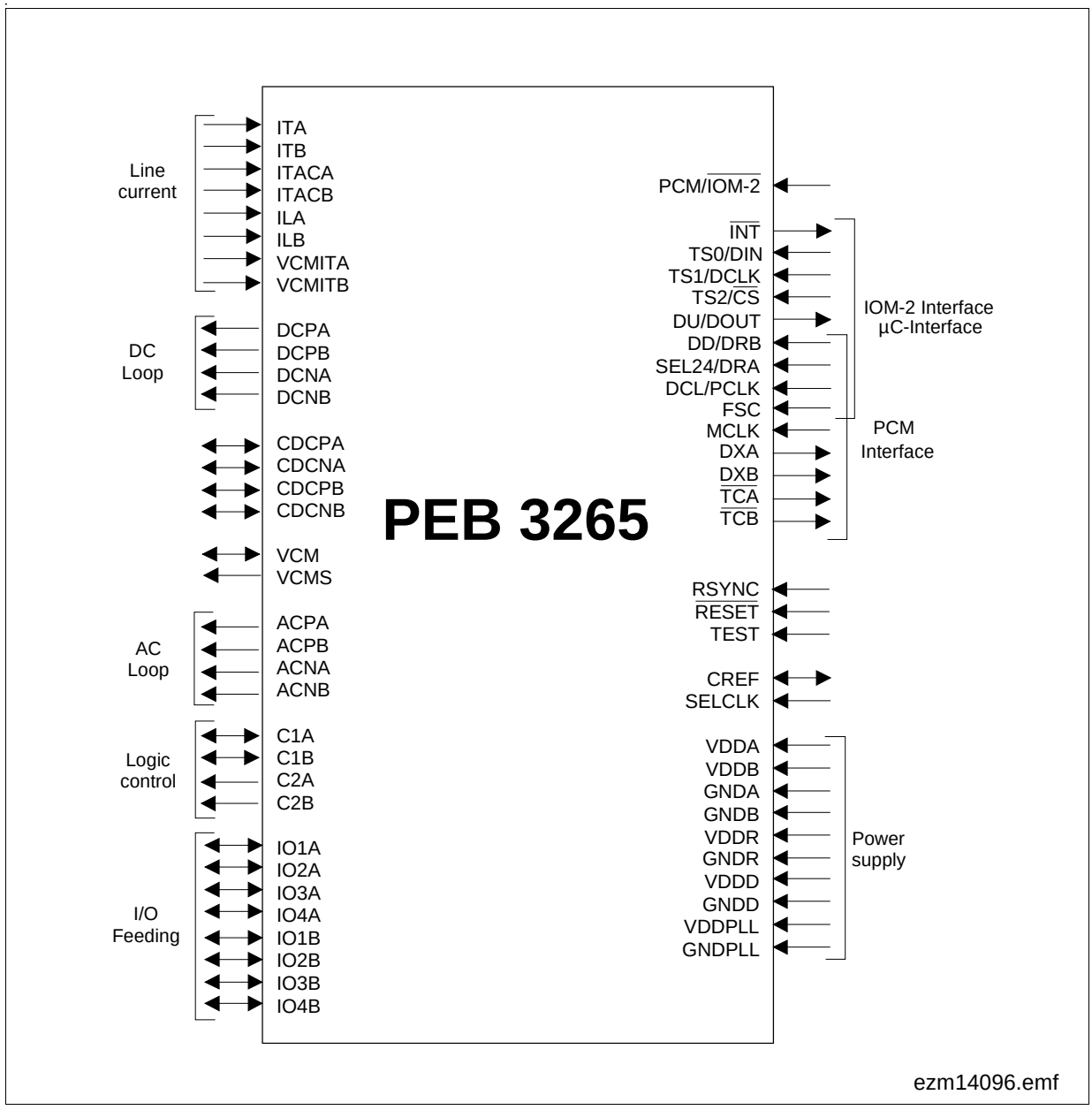


Figure 1-4 Logic Symbol SLICOFI-2

2 Functional Description

2.1 Functional Overview

The DuSLIC chip set is a cost-effective, high-performance solution that provides the BORSCHT functions of an analog line circuit. DuSLIC has the advantage of offering all the functions integrated in a single channel high-voltage SLIC and in a dual channel DSP-based CODEC.

An important feature of the DuSLIC design is the fact that all the SLIC and CODEC functions are programmable via the dual-channel CODEC device. Conventional designs need a number of external components to adapt the circuit for use in different countries and applications. In contrast, the configuration software DuSLICOS can be used to program the following functions of the DuSLIC chip set:

- DC (battery) feed characteristics
- AC impedance matching
- Transmit gain
- Receive gain
- Hybrid balance
- Frequency response in transmit and receive direction
- Ring frequency and amplitude
- Hook thresholds
- DTMF and FSK
- Universal Tone Detection
- Line Echo Cancellation
- Testfunctions
- TTX modes

One of the main challenges of linecard development is to adapt the above-mentioned functions to country-specific requirements. These adaptations used to be handled by hardware, an approach that required a different linecard board for every modification to a specification.

Because signal processing within the SLICOFI-2 is completely digital, it is possible to adapt to the requirements listed above by simply updating the coefficients that control DSP processing of all data. This means, for example, that changing impedance matching or hybrid balance no longer requires hardware modifications. The same hardware is now capable of meeting the requirements of different markets. The digital nature of the filters and gain stages also assures high reliability, no drifts (over temperature or time) and minimal variations between different lines.

The characteristics for the two voice channels within SLICOFI-2 can be programmed independently of each other. The DuSLICOS software is provided to automate calculation of coefficients to match different requirements. DuSLICOS also verifies the calculated coefficients.

2.2 BORSCHT Functions

B Battery feed

O Overvoltage protection

R Ringing

S Signaling (supervision)

C Coding

H Hybrid for 2/4-wire conversion

T Testing

Figure 2-1 shows the BORSCHT functions with the other function blocks normally required for an analog line circuit.

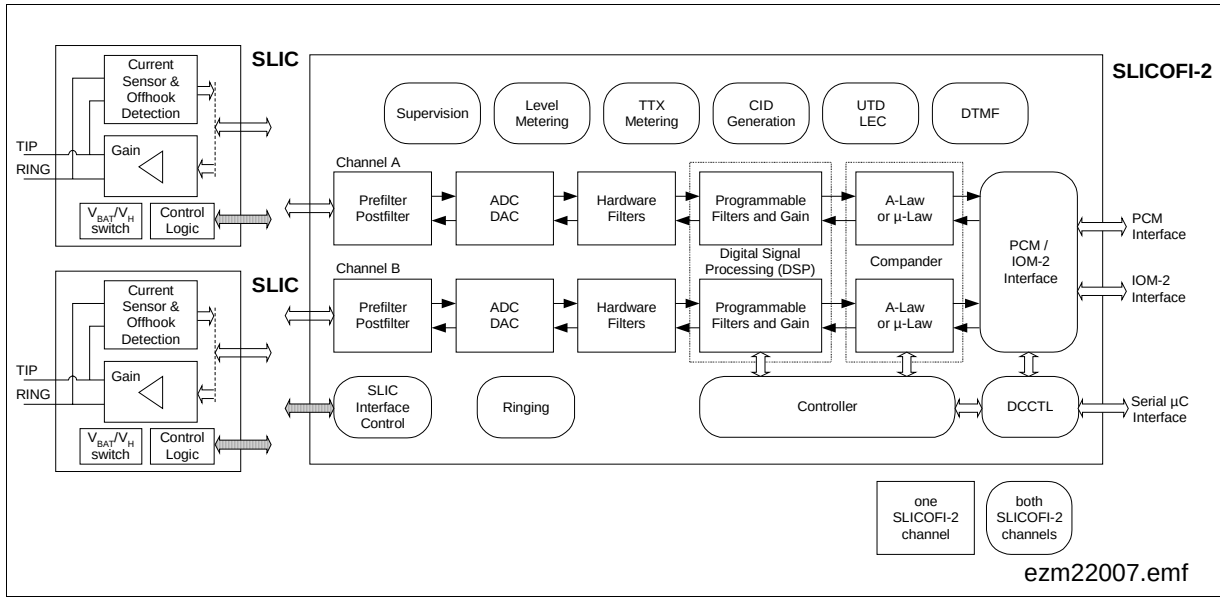


Figure 2-1 Typical Line Circuit Functions

The following paragraphs explain the advantages of using DuSLIC to implement the BORSCHT functions.

Battery Feed

An analog line circuit provides the voltage and current for subscriber equipment. In conventional line circuits, extra hardware is needed to adapt the battery feed characteristics to the requirements for different applications and countries. With the DuSLIC chip set, the battery feed (DC) characteristics can be programmed in the SLICOFI-2 (low-voltage SLIC function, see **Figure 1-1**) and applied to the line via the SLIC.

Overvoltage Protection

Overvoltage protection is indispensable to prevent damage to the line circuit if the system is exposed to high voltages that can result from power lines crossing or lightning strikes. The robust 170 V SLIC technology together with the external low cost protection network, consisting of varistors, resistors and thyristor diodes, form a reliable overvoltage protection solution. If an overvoltage occurs, the protection network separates the DuSLIC from the Tip and Ring lines.

Ringing

The ringing signal is a low-frequency, high-voltage signal to the subscriber equipment. In conventional line circuits, the ringing voltage (40 V_{RMS} to 85 V_{RMS}) is generated in an external ringing generator and applied to the Tip and Ring lines by a relay. With the DuSLIC chip set, the ringing generator is integrated and this relay is not needed. This saves space and costs in the line circuit design. The ringing signal is generated in the low-voltage SLICOFI-2 and amplified in the high-voltage SLIC. DuSLIC supports balanced and unbalanced ringing. With balanced ringing, the ringing voltage is applied differentially to the Tip and Ring lines. With unbalanced ringing, the ringing voltage is applied single-ended to either the Tip or Ring line against a potential which is near ground (for details see "Ringing Modes" on page 3-15). Balanced ringing is generated by SLIC-E, while SLIC-P can generate both balanced and unbalanced ringing.

Signaling (Supervision)

DuSLIC must detect when a subscriber changes from on-hook mode to off-hook mode in both non-ringing (hook switch detection) and ringing modes (ring trip detection). With this chip set, the thresholds for ring trip detection can be programmed in SLICOFI-2 to suit applications without using external components.

Coding

SLICOFI-2 encodes an analog input signal to a digital PCM signal and decodes a PCM signal to an analog signal. Both A-law and µ-law coding is supported and can be selected via software.

Hybrid for 2/4-wire Conversion

The subscriber equipment is connected to a 2-wire interface (Tip and Ring) where information is transmitted bidirectionally. For digital transmission through the switching network, the information must be split into separate transmit and receive paths (4 wires). To avoid generating echoes, the hybrid function requires a balanced network matched to the line impedance. Hybrid balancing can be programmed in the DuSLIC device without using any external components.

Testing

Access to the analog loop is necessary to perform the regular measurements involved in monitoring the local loop. Line circuit functions must also be tested. In conventional line circuit solutions, test units have to be switched to perform loop and line circuit tests. A remote testing unit and relays are normally necessary to perform a full range of tests. DuSLIC already offers a number of internal test features to check both the local loop and the line circuit.

Additional Line Circuit Functions:

Teletax Metering

In many countries, Teletax metering signals (TTX signals) are sent to the subscriber for billing purposes. A 12/16 kHz sinusoidal metering burst has to be transmitted. As soon as metering pulses are applied to the subscriber line, they also divert to the transmit signal path which means that a notch filter has to block the 12/16 kHz signal to prevent overloading the transmit A/D converter. In contrast to conventional line circuits, the DuSLIC chip set generates the metering signal internally. The fact that the notch filter is integrated is one of the big advantages of DuSLIC.

DTMF

A DTMF signal is used for touchtone signaling from a subscriber to the Central Office. Each digit is represented by a pair of tones. DuSLIC has an integrated DTMF decoder. The decoder monitors the transmit path for valid tone pairs and outputs the corresponding digital code for each pair. DuSLIC also has an integrated DTMF generator comprising two tone generators.

Caller ID Frequency Shift Keying (FSK) Modulator

Caller ID is used to provide caller information to the subscriber during on-hook transmission. DuSLIC has an integrated FSK modulator capable of sending caller ID information. The caller ID modulator complies with all requirements of ITU-T recommendation V.23 and Bell 202.

Universal Tone Detection Unit (UTD)

An Universal Tone Detection unit can be used to detect special tones, e.g. fax- or modem-tones. This is e.g. useful for activating the optimized filter coefficient set for modem transmission.

Line Echo Cancellation Unit (LEC)

An adaptive Line Echo Cancellation unit can be used for the cancellation of near end echos.

2.3 DC Feeding

Analog telephones need a DC current in the off-hook state. AC speech signals in the receive and transmit directions are superimposed on this DC current.

Once the off-hook state has been detected, the SLIC must supply a DC current to the subscriber line. The current is typically in the range of 14 to 40 mA, depending on local country specifications. Conventional linecard solutions require additional hardware to adjust the DC feed current to meet different country specifications.

By contrast, DC feeding with the SLICOFI-2 is fully programmable. Special digital filter technology offers an extremely cost-effective solution that is far more flexible than analog DC feeding circuits. The DC feeding characteristic in SLICOFI-2 is programmed using software coefficients. **Figure 2-2** shows the signal paths for DC feeding between the SLIC´s and SLICOFI-2:

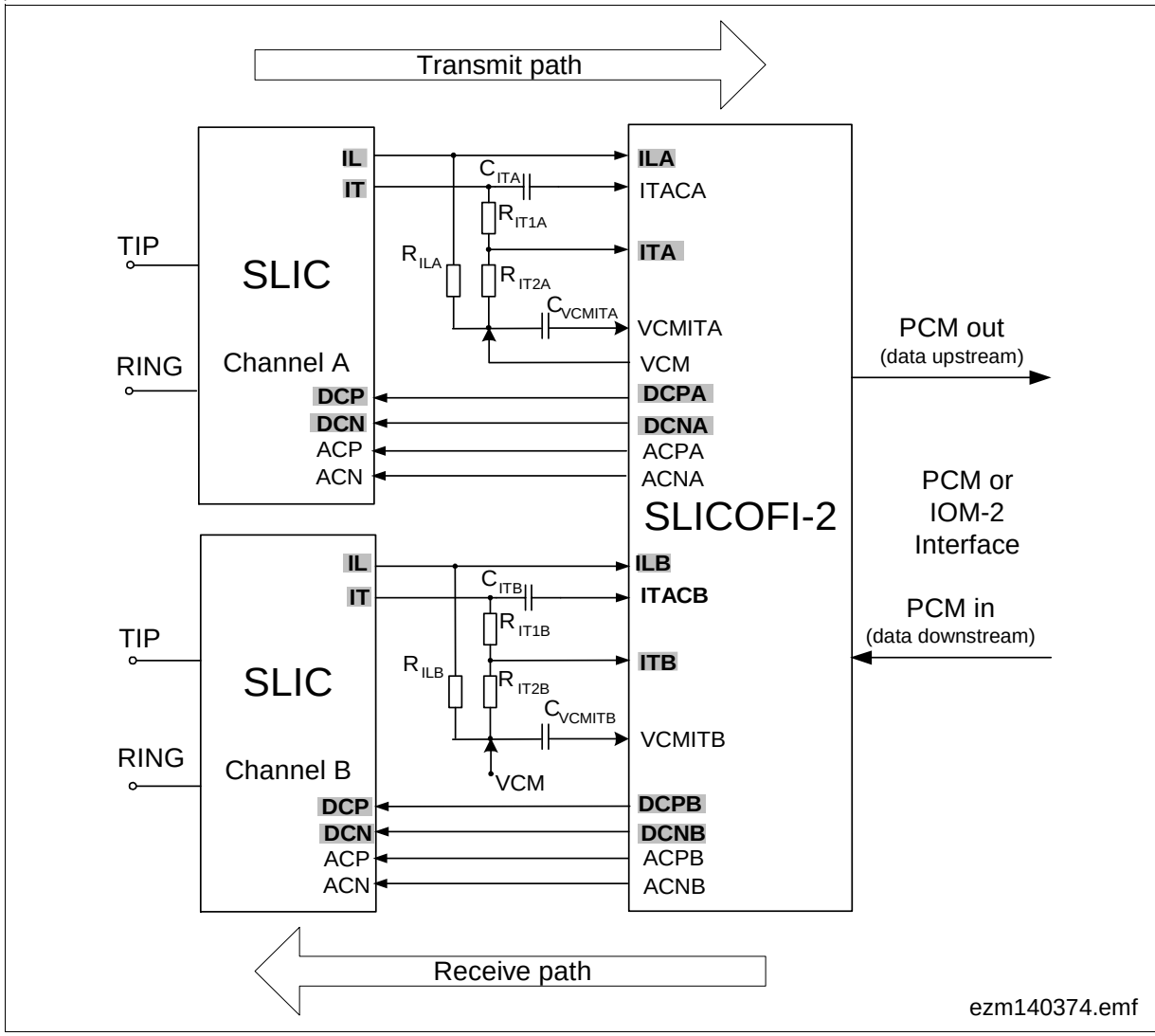


Figure 2-2 Signal Paths - DC Feeding

DC Characteristic Feeding Zones

The DuSLIC DC feeding characteristic has three different zones: the constant current zone, the resistive zone and the constant voltage zone. A programmable voltage reserve can be selected to avoid clipping the high AC signals (e.g. TTX) and to take into account the voltage drop of the SLIC (see **Chapter 2.3.5**). The DC feeding characteristic is shown in **Figure 2-3**.

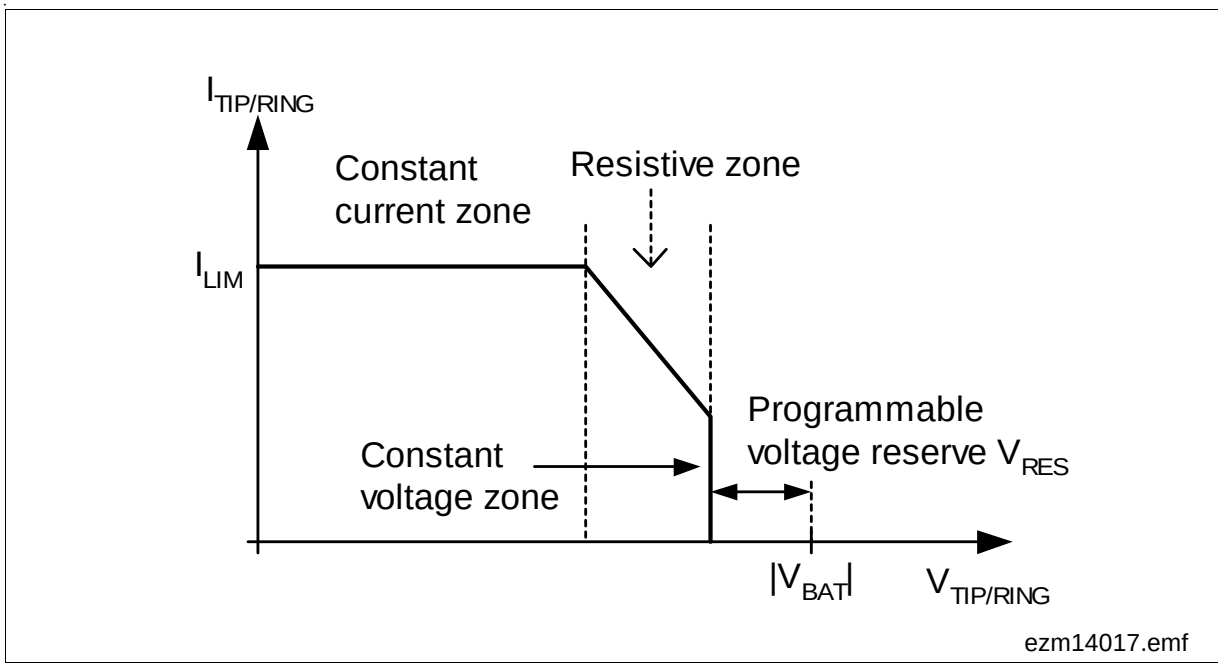


Figure 2-3 DC Feeding Characteristic

The simplified diagram shows the constant current zone as an ideal current source with an infinite internal resistance, while the constant voltage zone is shown as an ideal voltage source with an internal resistance of 0 Ω. For the specification of the internal resistances see **Chapter 2.3.4**

2.3.1 Constant Current Zone

In the off-hook state, the feed current must usually be kept at a constant value independent of load (see **Figure 2-4**). The SLIC senses the DC current and supplies this information to SLICOFI-2 via the IT pin (input pin for DC control). SLICOFI-2 compares the actual current with the programmed value and adjusts the SLIC drivers as necessary. $I_{TIP/RING}$ in the constant current zone is programmable from 0 to 32 mA.

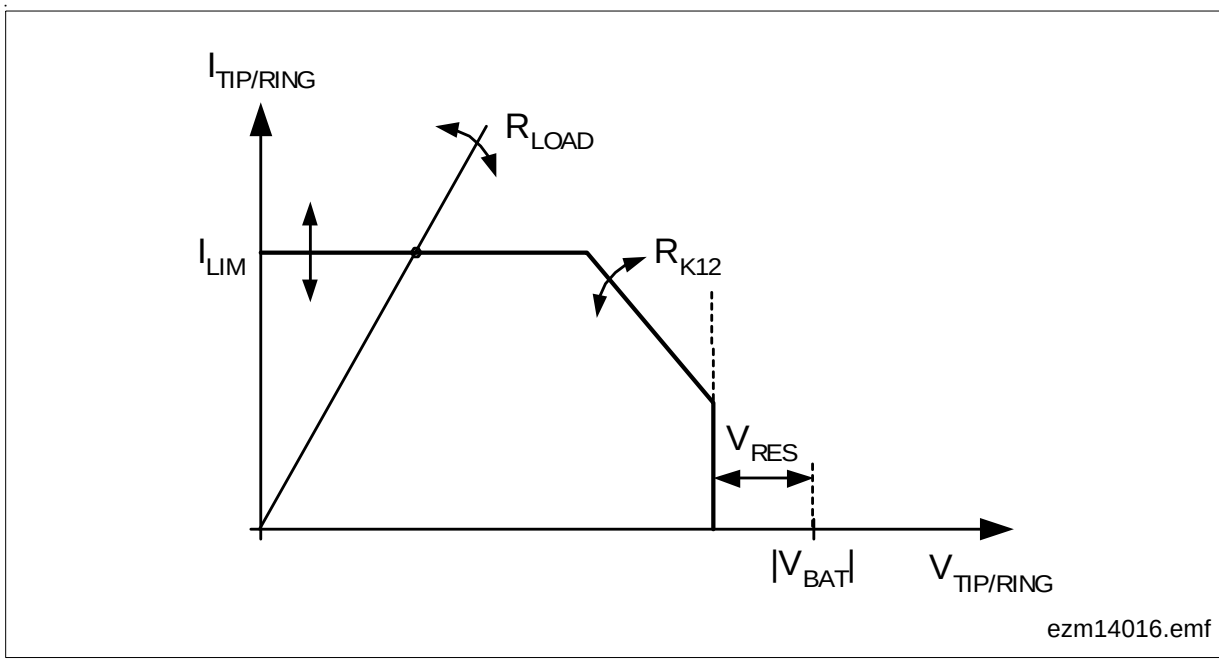


Figure 2-4 Constant Current Zone

Depending on the load, the operating point is determined by $V_{TIP/RING}$ between the Tip and Ring pins.

The operating point is calculated from:

$V_{TIP/RING} = R_{LOAD} \times I_{TIP/RING}$

where

$R_{LOAD} = R_{PRE} + R_{LINE} + R_{PHONE,OFFHOOK}$

$R_{PRE} = R_{PROT} + R_{STAB}$ (see **Figure 6-1**, page 6-1 and **Figure 6-2**, page 6-2).

The lower the load resistance, the lower the voltage between the Tip and Ring pins.

2.3.2 Resistive Zone

The programmable resistive zone of SLICOFI-2 provides extra flexibility over a wide range of applications. The resistive zone is used for very long lines where the battery is incapable of feeding a constant current into the line.
The operating point in this case crosses from the constant current zone for low and medium impedance loops to the resistive zone for high impedance loops (see **Figure 2-5**). The resistance of the zone R_{K12} is programmable from R_{PRE} to 1000 Ω.

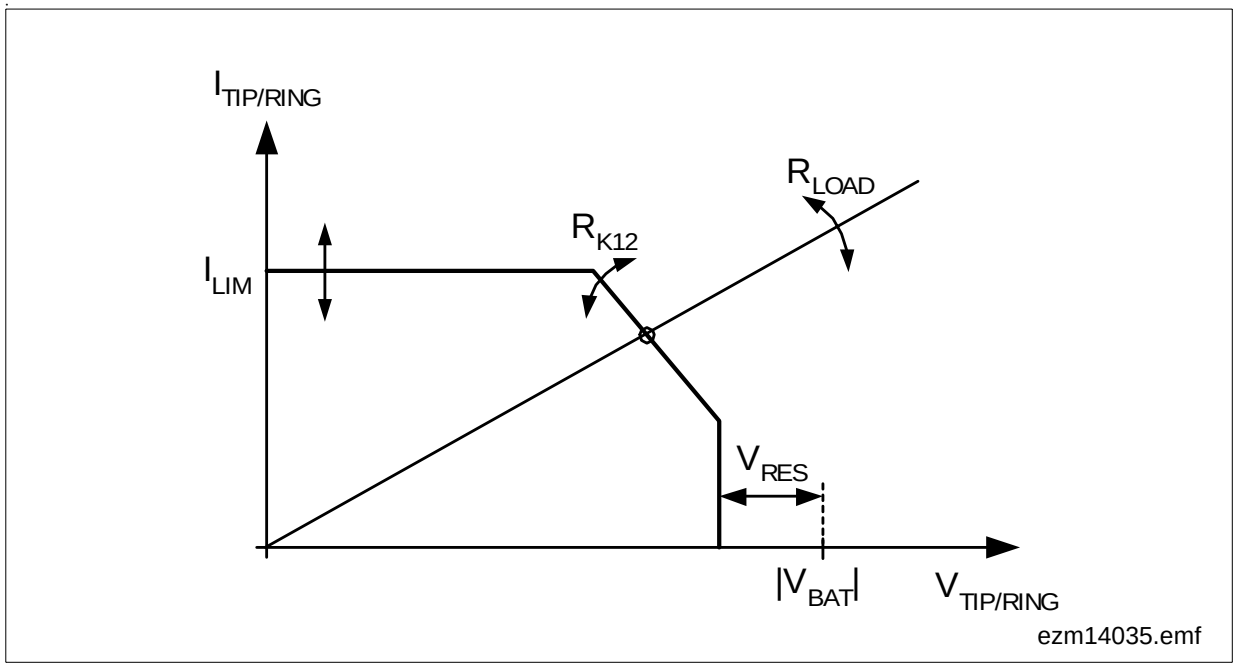


Figure 2-5 Resistive Zone

2.3.3 Constant Voltage Zone

The constant voltage zone is used in some applications to supply current through the line. In this case $V_{TIP/RING}$ is constant (see **Figure 2-6**) and the current depends on the load between the Tip and Ring pins.

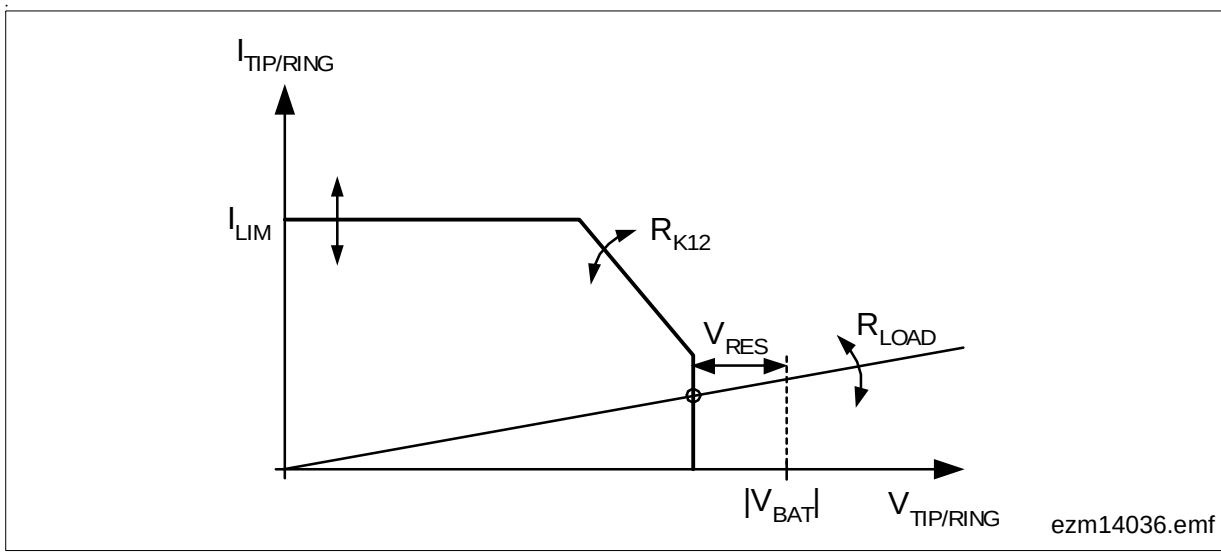


Figure 2-6 Constant Voltage Zone

2.3.4 Programmable Voltage and Current Range of DC Characteristic

In the above chapters the idealized DC characteristics were shown. A detailed description is given in **Figure 2-7**.

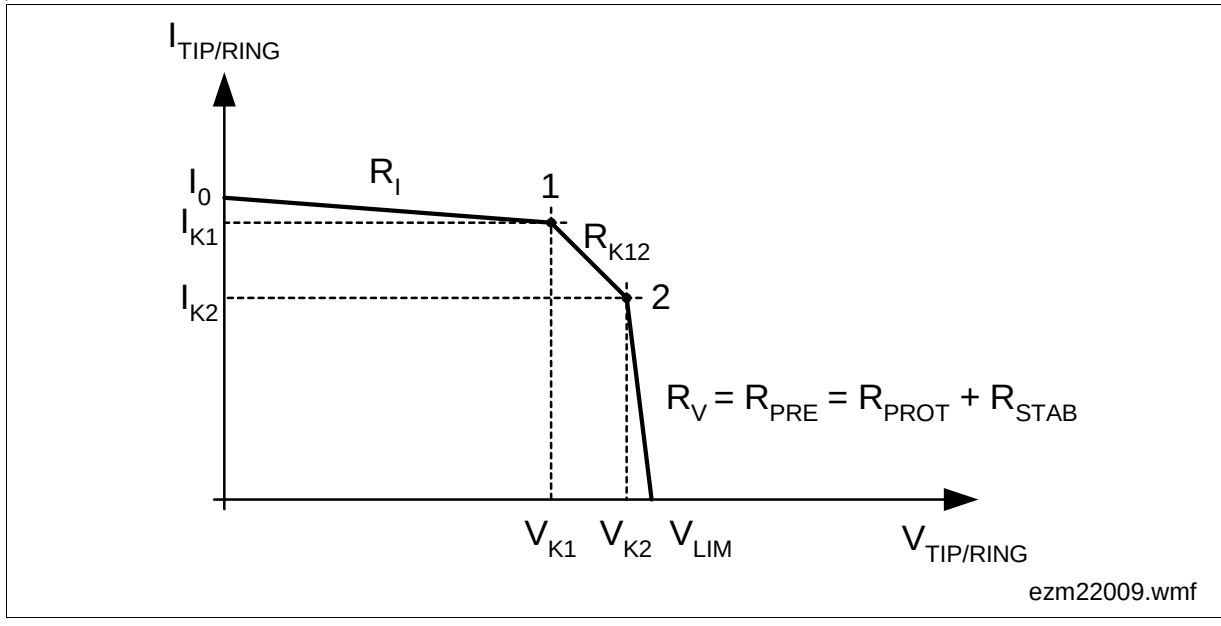


Figure 2-7 DC Characteristic (Detailed Description)

In the constant current zone a finite resistor value of typically R_I = 10 kΩ is usually applied for stability reasons.
In the constant voltage zone an internal resistor value of 0 Ω is applied.
The external resistors $R_{PRE} = R_{Stab} + R_{Prot}$ necessary for stability and protection define the resistance R_V seen at the RING and TIP wires of the application.
The programmable range of the parameters R_I, I_0, I_{K1}, V_{K1}, R_{K12} and V_{LIM} is given in **Table 2-1**.

Table 2-1 DC Characteristic

Symbol	Programmable Range	Condition
R_I	1.8 kΩ ... 40 kΩ	
I_0	0 ... 32 mA	
I_{K1}	0 ... 32 mA	
V_{K1}	0 ... 50 V	
	$V_{K1} < V_{LIM} - I_{K1} \cdot R_{K12}$	only (V_{K1}, I_{K1})
	$V_{K1} < V_{LIM} - I_{K1} \cdot R_V$ $V_{K1} > V_{LIM} - I_{K1} \cdot R_{K12}$	(V_{K1}, I_{K1}) and (V_{K2}, I_{K2})
R_{K12}	R_V ... 1000 Ω	
V_{LIM}	0 ... 50 V	
	$V_{LIM} > V_{K1} + I_{K1} \cdot R_{K12}$	only (V_{K1}, I_{K1})

2.3.5 Programmable Voltage Reserve

To avoid clipping AC speech signals as well as AC metering pulses, a programmable voltage reserve V_{RES} (see **Figure 2-3**) has to be provided.

V_{RES} consists of:

- Voltage reserve of the SLIC output buffers: this voltage drop depends on the output current through the Tip and Ring pins. For a standard output current of 25 mA, this voltage reserve is a few volts (see **Table 3-5**).
- Voltage reserve for AC speech signals: 2 V
- Voltage reserve for AC metering pulses: The TTX signal amplitude V_{TTX} depends on local specifications and varies from 0.1 V_{RMS} to several V_{RMS} at a load of 200 Ω. To obtain V_{TTX} = 2 V_{RMS} at a load of 200 Ω and R_{PRE} = 50 Ω (R_{PRE} = R_{PROT} + R_{STAB} (see **Figure 6-2**, page 6-2)), 3 V_{RMS} = 4.24 V_{PEAK} are needed at the SLIC output.

V_{RES} must therefore be programmed to 10.24 V (= 4 V (SLIC drop for peak current of DC and speech and TTX) + 2 V (AC speech signals) + 4.24 V (TTX-signal)).

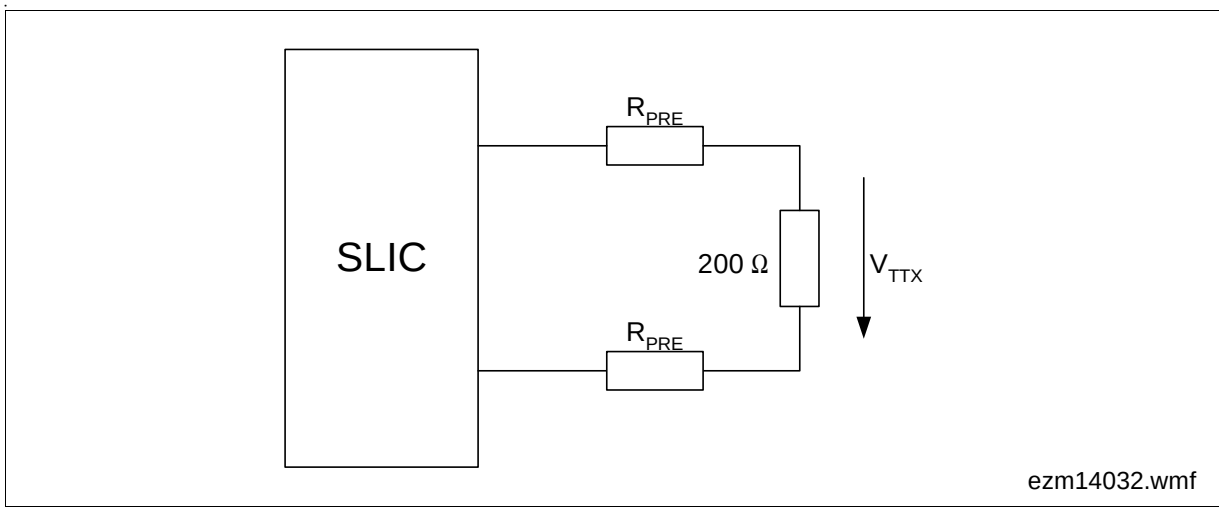


Figure 2-8 TTX Voltage Reserve Schematic

2.3.6 Extended Battery Feeding

If the battery voltage is not sufficient to supply the minimum required current through the line even in the resistive zone, an auxiliary positive battery voltage is used to expand the possible voltage amplitude between Tip and Ring. With this voltage (V_{HR} - V_{BATH}), it is possible to supply the constant current through very long lines. **Figure 2-9** shows the DC feeding impedances $R_{MAX,ACTH}$ in ACTH mode and $R_{MAX,ACTR}$ in ACTR mode (for ACTH and ACTR modes see **Chapter 3.1**).

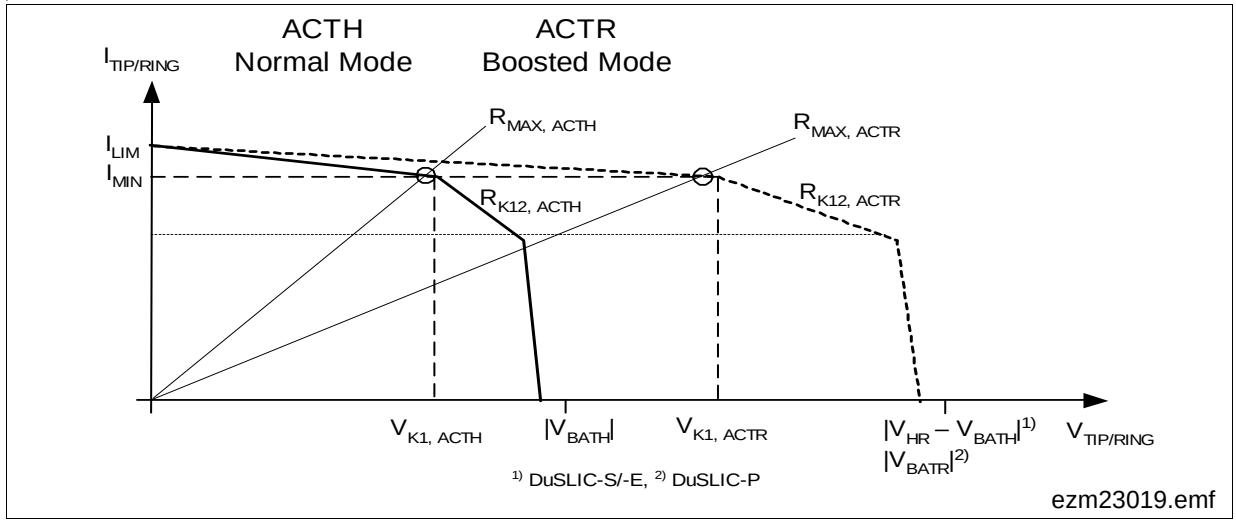


Figure 2-9 DC Feeding Characteristics (ACTH, ACTR)

2.3.7 SLIC Power Dissipation

The power dissipation in the SLIC can be estimated by the power dissipation in the output stages (see **Chapter 3.4.3**). The power dissipation can be calculated from:

$P_{SLIC} \sim (V_{BAT} - V_{TIP/RING}) \times I_{TIP/RING}$

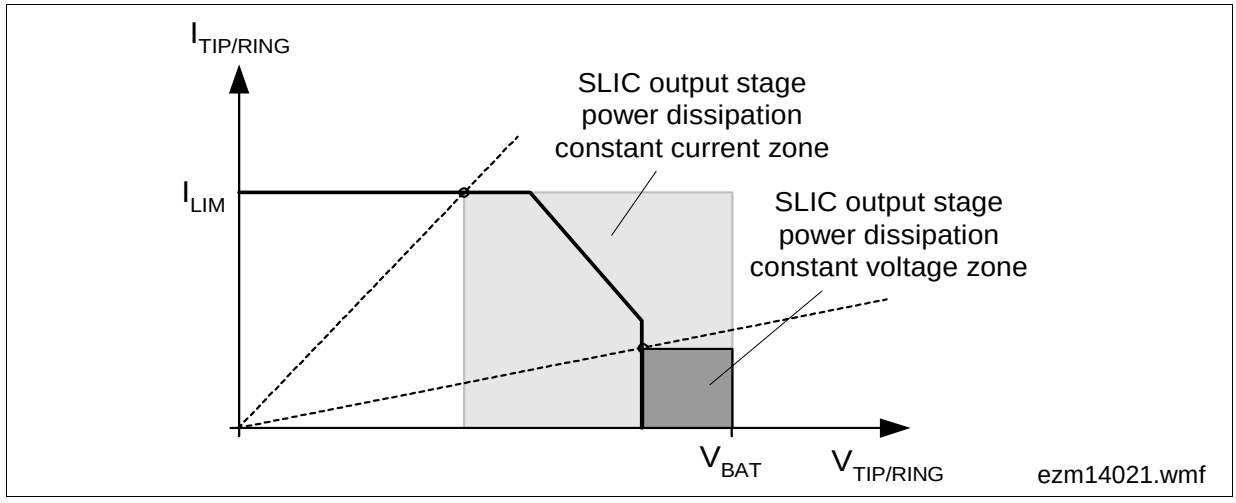


Figure 2-10 Power Dissipation

2.4 AC Transmission Characteristics

SLICOFI-2 connects to the digital world either via an IOM-2 or PCM interface. The SLIC performs the high voltage functions. In receive direction, SLICOFI-2 converts PCM data from the network and outputs a differential analog signal (ACP and ACN) to SLIC, that amplifies the signal and applies it to the subscriber line. In transmit direction, the transversal (IT) and longitudinal (IL) currents on the line are sensed by the SLIC and fed to SLICOFI-2. A capacitor separates the transversal line current into DC (IT) and AC (ITAC) components. As ITAC is the sensed transversal (also called metallic) current on the line, it includes both the receive and transmit components. SLICOFI-2 separates the receive and transmit components digitally, via a transhybrid circuit (see **Figure 2-13**). **Figure 2-11** shows the signal paths for AC transmission between the SLIC and SLICOFI-2:

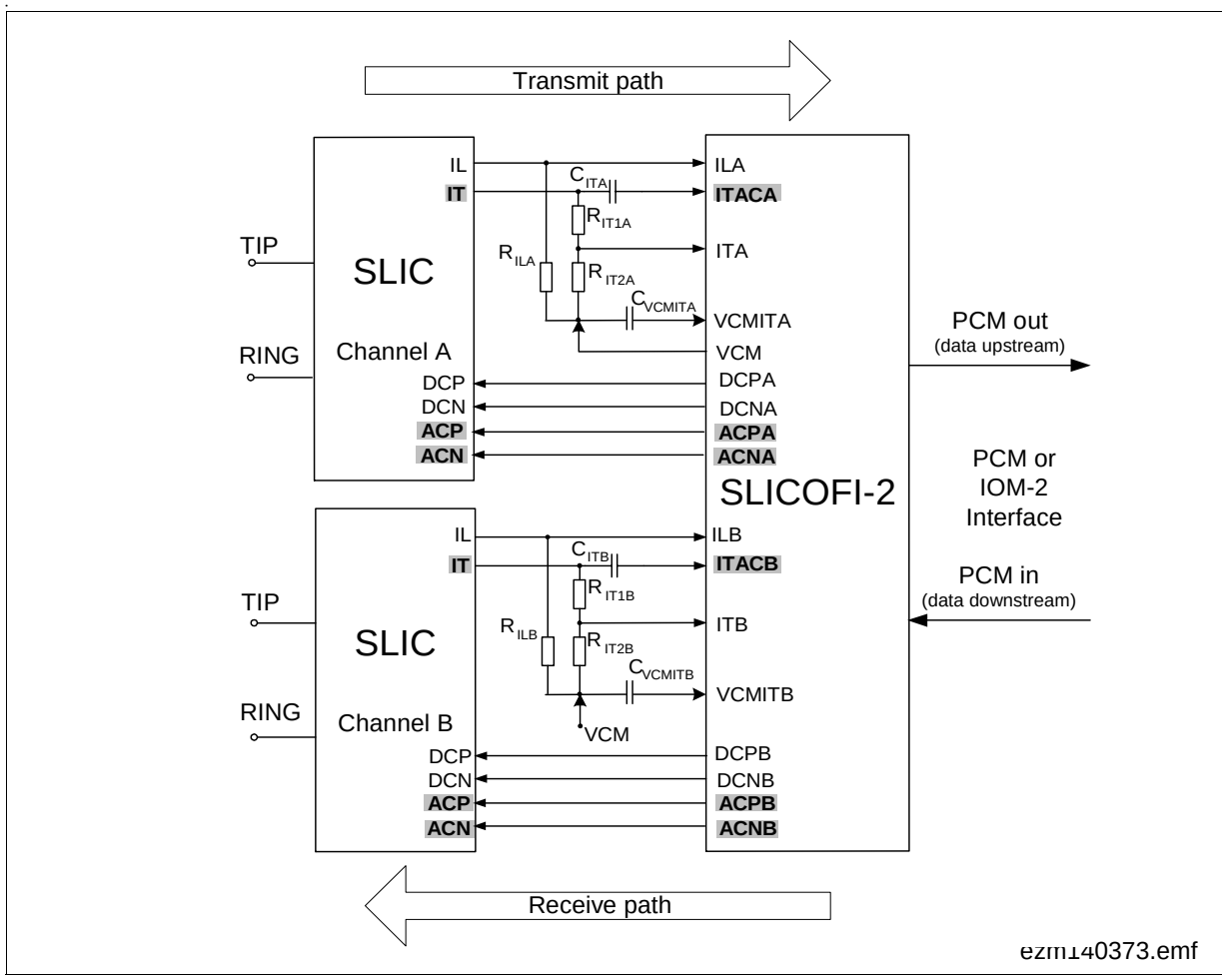


Figure 2-11 Signal Paths - AC Transmission

The signal flow within the SLICOFI-2 for one voice channel is shown in **Figure 2-12** by the following schematic circuitry. With the exception of a few analog filter functions, signal processing is performed digitally in the SLICOFI-2.

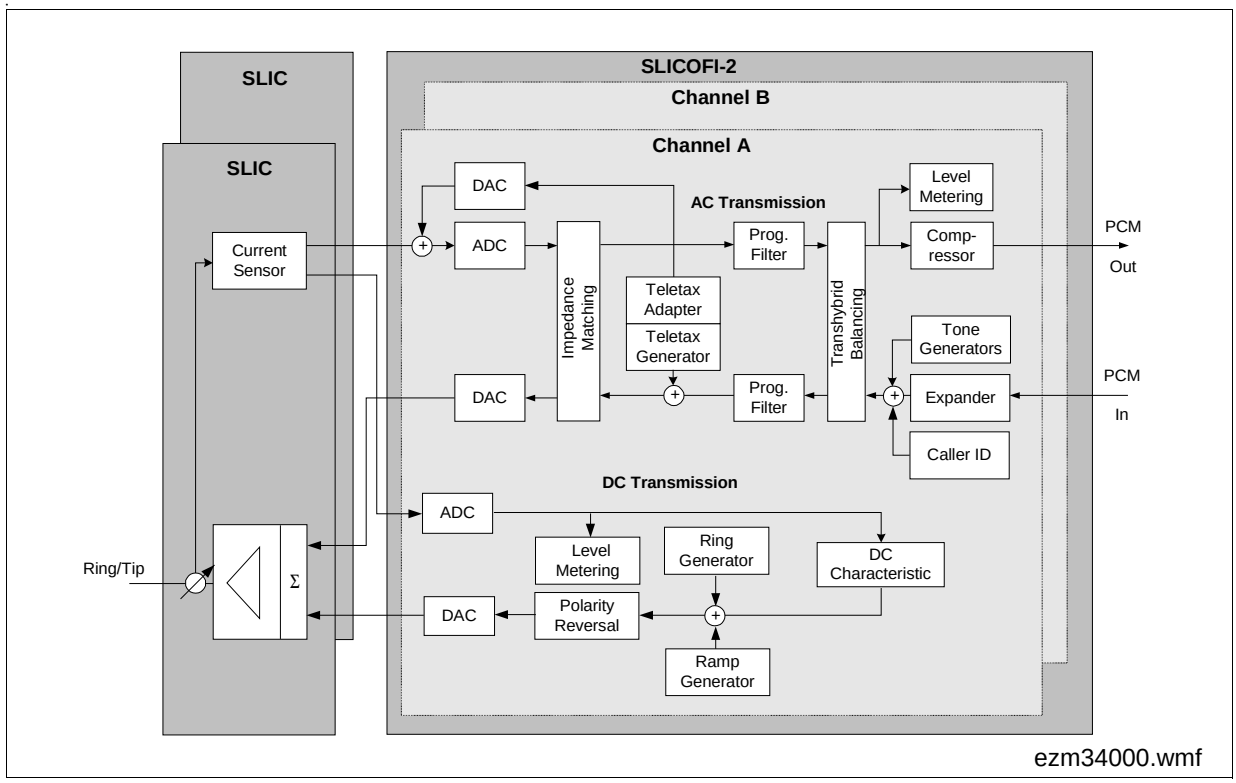


Figure 2-12 Signal Flow in Voice Channel (A)

2.4.1 Transmit Path

The current sense signal (ITAC) is converted to a voltage by an external resistor. This voltage is first filtered by a simple anti-aliasing filter (Prefilter, see **Figure 2-1**) that stops producing noise in the voiceband from signals near the A/D sampling frequency. A/D conversion is done by a 1-bit sigma-delta converter. The digital signal is down-sampled further and routed through programmable gain and filter stages. The coefficients for the filter and gain stages can be programmed to meet specific requirements. The processed digital signal goes through a compander (CMP) that converts the voice data into A-law or µ-law codes. A time slot assignment unit outputs the voice data to the programmed time slot. SLICOFI-2 can also operate in 16-bit linear mode for processing uncompressed voice data. In this case, two time slots are used for one voice channel.

2.4.2 Receive Path

The digital input signal is received via the IOM-2 or PCM interface. Expansion (EXP), PCM low-pass filtering, frequency response correction and gain correction are performed by the DSP. The digital data stream is up-sampled and converted to a corresponding analog signal. After smoothing by post-filters in the SLICOFI-2 (Postfilter, see **Figure 2-1**), the AC signal is fed to the SLIC, where it is superimposed on the DC

signal. The DC signal has been processed in a separate DC path. A TTX signal, generated digitally within SLICOFI-2, can also be added.

2.4.3 Impedance Matching

The SLIC outputs the voice signal to the line (receive direction) and also senses the voice signal coming from the subscriber. The AC impedance of the SLIC and the load impedance need to be matched in order to maximize power transfer and minimize 2-wire return loss. The 2-wire return loss is a measure of the impedance matching between a transmission line and the AC termination of the DuSLIC.

The actual line impedance however can vary considerably, depending on loop length, loaded/unloaded lines, cable type, etc. Reference networks have therefore been defined to represent the average characteristics of a country's local loop. These reference networks differ from country to country and need to be reflected by the linecard being used in that country.

Impedance matching is done digitally within SLICOFI-2 by providing three impedance matching feedback loops. The loops feed the transmit signal back to the receive signal simulating the programmed impedance through the SLIC. When calculating the feedback filter coefficients, the external resistors between protection network and SLIC ($R_{PRE} = R_{PROT} + R_{STAB}$, see **Figure 6-2**, page 6-2) have to be taken into account. Impedance can be programmed to any appropriate value (real and complex impedance values). This means the device can be adapted to requirements anywhere in the world without the hardware changes that are necessary with conventional line card designs.

2.4.4 Transhybrid Balance

Digital switching systems can handle voice data only if receive and transmit data are separated on distinctive channels. The analog voice signal on the local loop is 2-wire full duplex, so it needs to be converted from 2-wire to 4-wire (2 wires each for receive and transmit). The circuitry, that performs this task, is commonly referred to as a hybrid circuit (see **Figure 2-13**)

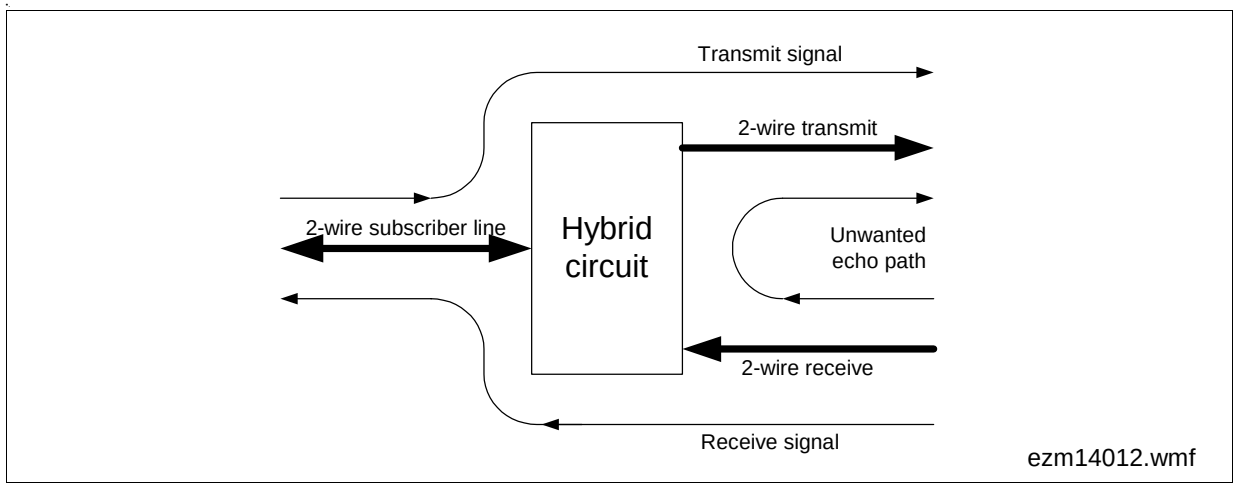


Figure 2-13 2/4-wire Conversion in the Hybrid Circuit

To prevent the receive voice signal being looped back (echoed) directly into the transmit voice path, the hybrid circuit has to separate the receive path signal from the transmit path signal.
In contrast with conventional line card designs, echo cancellation is implemented digitally within SLICOFI-2. **Figure 2-13** shows the transhybrid loop that subtracts the receive signal from the transmit signal. The hybrid function is also dependent on loop condition. It has to be adapted to country-specific requirements. In conventional line card designs, this is done by external hardware adaptation. With SLICOFI-2, adaptation is simply a matter of updating coefficients. No hardware changes are necessary.

2.5 Ringing

With the 170 V technology used by the SLIC, a ringing voltage of up to 85 V_{RMS} can be generated on-chip without the need for an external ringing generator. SLICOFI-2 generates a sinusoidal ringing signal that causes less noise and cross-talk in neighboring lines than a trapezoidal ringing signal. The ringing frequency is programmable from 15 to 100 Hz.
The advantage over traditional applications with a central ringing generator and decoupling resistors (approx. R = 400 Ω) is the very low source impedance of DuSLIC (approx. 60 Ω without R_{PROT}). Thus it is possible to supply the subscriber line with a lower ringing voltage from the SLIC. SLIC-E and SLIC-P support different ringing methods (see **Chapter 2.5.3**).

2.5.1 Ringer Load

A typical ringer load can be thought of as a resistor in series with a capacitor. Ringer loads are usually described as a REN (Ringer Equivalence Number) value. REN is used to describe the on-hook impedance of the terminal equipment, and is actually a dimensionless ratio that reflects a certain load. REN definitions vary from country to country. A commonly used REN is described in FCC part 68 that defines a single REN as either 5 kΩ, 7 kΩ or 8 kΩ of AC impedance at 20 Hz. The impedance of an n-multiple REN is equivalent to parallel connection of n single RENs. In this manual, all references to REN assume the 7 kΩ model.

For example, a 1 REN and 5 REN load would be:

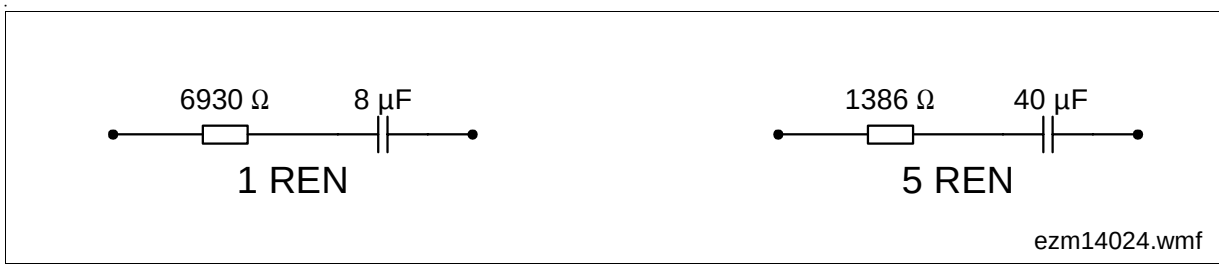


Figure 2-14 Typical Ringer Loads of 1 and 5 REN used in US

2.5.2 Ring Trip

Once the subscriber has gone off-hook, the ringing signal must be removed within a specified time, and power must start feeding to the subscriber's phone. There are two ring trip methods:

DC ring trip detection:

By applying a DC voltage together with the ringing signal, a transversal DC loop current starts to flow when the subscriber goes off-hook. This DC current is sensed and in this way used as an off hook criterion. The threshold for the ring trip DC current is set internally in SLICOFI-2, programmed via the digital interface.
The DC voltage for ring trip detection can be generated by the DuSLIC chip set and the internal ring trip function can be used, even if an external ringing generator is used.

AC ring trip detection:

For short lines (< 1 kΩ loop length) and low power applications, the DC offset can be avoided to reduce the battery voltage for a given ring amplitude. Ring trip detection is then performed by interpreting the AC impedance without using a DC offset voltage.

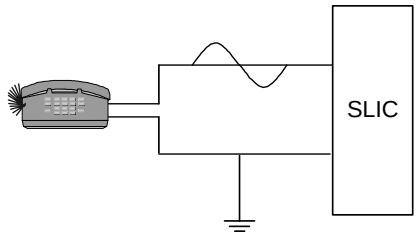
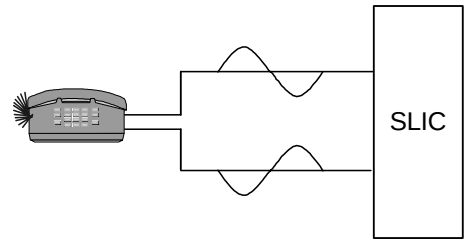
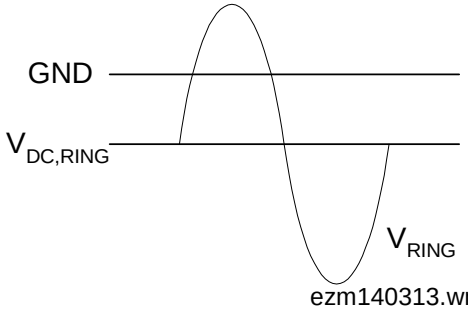
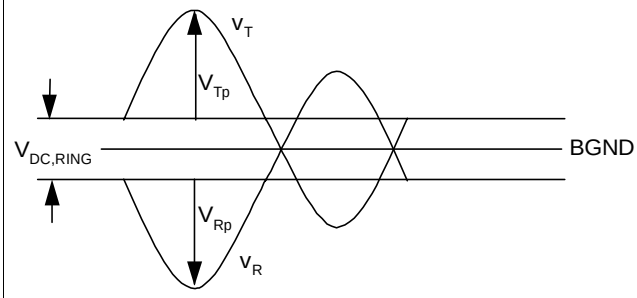
Most applications with DuSLIC are using DC ring trip detection, which is more reliable than AC ring trip detection.

2.5.3 Ringing Methods

There are two methods of ringing:

- Balanced ringing (bridged ringing)
- Unbalanced ringing (divided ringing)

Table 2-2 Unbalanced versus Balanced Ringing

Unbalanced Ringing:	Balanced Ringing:
The ringing signal is applied to only either the Tip or Ring line, whereas GND is applied to the other line.	An opposite-phase ringing signal is applied to both Tip and Ring lines. The resulting ringing signal is the differential signal between Tip and Ring line. $v_{RING} = v_T - v_R + V_{DC,RING}$ If $v_T = - v_R$ then $v_{RING} = 2 \cdot v_T + V_{DC,RING} = 2 \cdot v + V_{DC,RING}$
 ezm140311.wmf	 ezm140312.wmf
 ezm140313.wmf	 ezm140317.wmf

The resulting ringing amplitude in balanced mode is twice the amplitude of v_T or v_R. This is an advantage over the unbalanced mode because the ringing generator circuit in balanced mode has to handle voltages of only half the amplitude to generate the same amplitude of ringing signal. The SLIC process technology used is capable of generating balanced ringing signals with amplitudes of up to 85 V_{RMS}.

Internal balanced ringing generally offers more benefits compared to unbalanced ringing:

- Balanced ringing produces much less longitudinal voltage, which results in a lower amount of noise coupled into adjacent cable pairs
- By using a differential ringing signal, lower supply voltages become possible

The phone itself cannot distinguish between balanced and unbalanced ringing. Where unbalanced ringing is still used, it is often simply a historical leftover. For a comparison between balanced and unbalanced ringing see also ANSI document T1.401-1993.

Additionally, integrated ringing with the DuSLIC offers the following advantages:

- Internal ringing (no need for external ringing generator and relays)
- Reduction of board space because of much higher integration and fewer external components
- Programmable ringing amplitude, frequency and ringing DC offset without hardware changes
- Programmable ring trip thresholds
- Switching of the ringing signal at zero-crossing

2.5.4 DuSLIC Ringing Options

Application requirements differ with regard to ringing amplitudes, power requirements, loop length and loads. The DuSLIC options include two different SLICs to select the most appropriate ringing methods (see **Table 2-3**):

Table 2-3 Ringing Options with SLIC-E and SLIC-P

SLIC Version / Ringing facility, battery voltages	SLIC-E PEB 4265	SLIC-P PEB 4266
Internal balanced ringing Max voltage in V_{RMS} (sinusoidal) at 20 Vdc used for ring trip detection	85 V_{RMS}	85 V_{RMS}
DC-voltage for balanced ringing[1)]	programmable typically 0..50 V	programmable typically 0..50 V
Internal unbalanced ringing Max. voltage in V_{RMS} (sinusoidal)	NO	50 V_{RMS}
DC-voltage for unbalanced ringing	NO	V_{BATR} / 2
Required SLIC supply voltages for maximum ringing amplitude (typ.)	+5 V, -70 V, +80 V	+5 V, -150 V
Number of battery voltages for power saving	2	2 (internal ringing used) 3 (external ringing used)

1) In most applications 20 V DC are sufficient for reliable ring tip detection. A higher DC voltage will reduce the achievable maximum ringing voltage. In special applications the full range of the DC voltage (V_{HR} - V_{BATH} -10V) can be used and is programmable.

SLIC-E can be used for long-haul exchange requirements and has an integrated facility for balanced ringing up to 85 V_{RMS}. The low-power SLIC-P is optimized for power-critical applications (e.g. intelligent ISDN network termination). Internal ringing can be used up to 85 V_{RMS} balanced or 50 V_{RMS} unbalanced. For lowest power applications where external ringing is preferred, three different battery voltages can be used for optimizing the power consumption of the application.

SLIC-E and SLIC-P differ in supply voltage configuration and the ring voltages (v_T, v_R) in the SLICOFI-2. External ringing is supported by the programmable I/Os and the RSYNC pin in the SLICOFI-2 for both SLIC´s.

2.5.5 Internal Balanced Ringing via SLICs

SLIC-E and SLIC-P support internal balanced ringing up to 85 V_{RMS}. The ringing signal is generated digitally within SLICOFI-2.

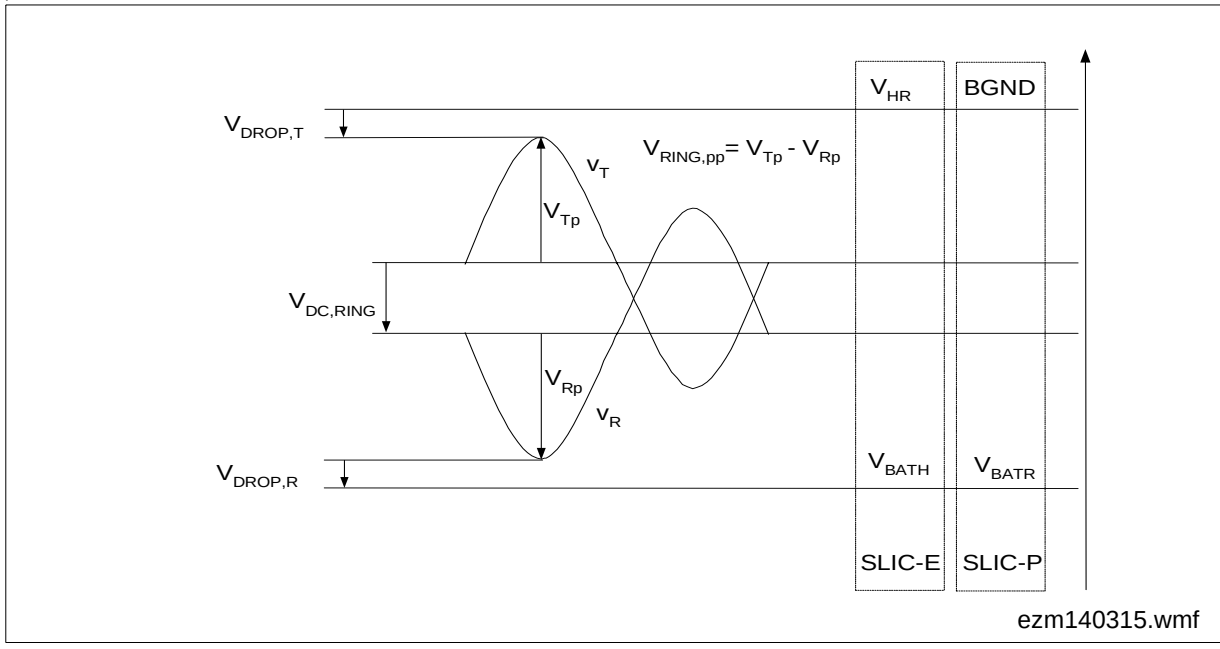


Figure 2-15 Balanced Ringing via SLIC-E and SLIC-P

In ringing mode, the DC feeding is not active. A programmable DC offset voltage is applied to the line instead. During ring bursts, the ringing DC offset and the ringing signal are summed digitally within SLICOFI-2 in accordance with the programmed values. This signal is then converted to an analog signal and applied to the SLIC. The SLIC amplifies the signal and supplies the line with ringing voltages up to 85 V_{RMS}. In balanced ringing mode, the SLICs use an additional supply voltage (V_{HR} for SLIC-E, V_{BATR} for SLIC-P). The total supply span is now V_{HR} - V_{BATH} for SLIC-E and -V_{BATR} for SLIC-P. The maximum ringing voltage that can be achieved is:

for SLIC-E: $V_{RING,RMS} = (V_{HR} - V_{BATH} - V_{DROP,\ RT} - V_{DC,RING}) / 1.41$
for SLIC-P: $V_{RING,RMS} = (- V_{BATR} - V_{DROP,RT} - V_{DC,RING}) / 1.41$
where: $V_{DROP,RT} = V_{DROP,T} + V_{DROP,R}$

With the DUSLIC ringing voltages up to 85 V_{RMS} sinusoidal can be applied, but also other ringing waveforms with other CREST-factors can be programmed.

The SLIC senses the transversal current on the line and supplies this information to the SLICOFI-2 at the IT pin. The IT current is monitored by SLICOFI-2. If the DC current exceeds the programmed ring trip threshold, SLICOFI-2 generates an interrupt. Ring trip is reliably detected and reported within two ring signal periods. The ringing signal is switched off during zero crossing by the SLICOFI-2. For a detailed application diagram of internal balanced ringing refer to the chapter on "Application Circuits" (see **Figure 6-1**, page 6-1).

2.5.6 Internal Unbalanced Ringing with SLIC-P

The internal unbalanced ringing together with SLIC-P can be used for ringing voltages up to 50 V_{RMS}. The SLICOFI-2 integrated ringing generator is used and the ringing signal is applied to either the Tip or Ring line. Ringing signal generation is the same as described above for balanced ringing. Since only one line is used for ringing, technology limits the ringing amplitude to about half the value of balanced ringing, to maximum 50 V_{RMS}.

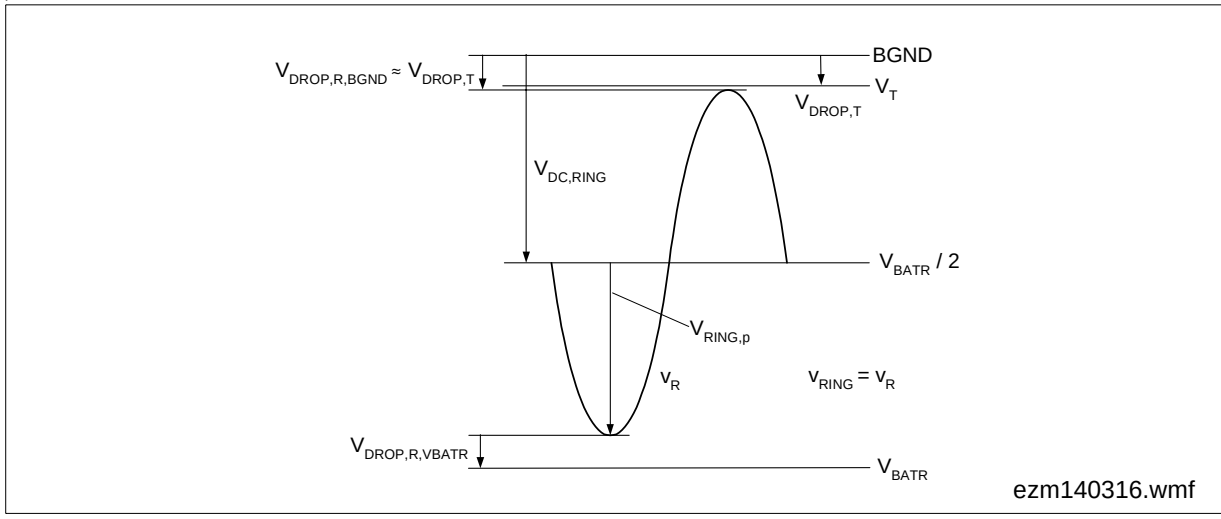


Figure 2-16 Unbalanced Ringing Signal

The above diagram shows an example with the ring line used for ringing and the tip line fixed at $- V_{DROP,T}$ which is the drop in the output buffer of the tip line of SLIC-P (typ. < 1 V). The ring line has a fixed DC voltage of $V_{BATR} / 2$ used for ring trip detection.

The maximum ringing voltage is:
$V_{RING,RMS} = (- V_{BATR} - V_{DROP,R,VBATR} - V_{DROP,T}) / 2.82$

When the called subscriber goes off-hook, a DC path is established from the Ring to the Tip line. The DC current is recognized by the SLICOFI-2 because it monitors the IT pin. An interrupt indicates ring trip if the line current exceeds the programmed threshold.

The same hardware can be used for integrated balanced or unbalanced ringing. The balanced or unbalanced modes are configured by software. The maximum achievable amplitudes depend on the values selected for V_{BATR}.

In both balanced and unbalanced ringing modes, SLICOFI-2 automatically applies and removes the ringing signal during zero-crossing. This reduces noise and cross-talk to adjacent lines.

2.5.7 External Unbalanced Ringing

SLICOFI-2 supports external ringing for higher unbalanced ringing voltage requirements above 50 V_{RMS} with both SLICs. For a detailed application diagram of unbalanced ringing see **Figure 6-5** and **Figure 6-6** on page 6-7 and page 6-8.

Since high voltages are involved, an external relay should be used to switch the RING line off and to switch the external ringing signal together with a DC voltage for ring trip to the line. This results in a DC offset between the Ring and Tip lines.

The SLICOFI-2 has to be set in the external ringing mode. A synchronisation signal of the external ringer is applied to the SLICOFI-2 via the RSYNC pin. The external relay is switched on or off synchronously to this signal via the IO1 pin of the SLICOFI-2 according to the actual mode of the DuSLIC. An interrupt is generated if the DC current exceeds the programmed ring trip threshold.

2.6 Metering

There are two different metering methods:

- Metering by sinusoidal bursts with either 12 or 16 kHz or
- Polarity reversal of Tip and Ring.

2.6.1 Metering by 12/16 kHz Sinusoidal Bursts

The required amplitude of the sinusoidal 12 or 16 kHz metering signals varies from a few hundred millivolts to 5 V_{RMS} and even more, depending on the country specifications and the application (long loop or short loop application). These signals are superimposed onto the speech signal. As soon as metering pulses are applied to the subscriber line, they also divert to the transmit signal path which means that a notch filter has to block the 12/16 kHz signal, to prevent overloading the transmit A/D converter. In contrast to conventional line circuits, the DuSLIC chip set generates the metering signal internally. The fact that the adaptive notch filter is integrated is one of the big advantages of DuSLIC.

Teletax Metering and Filtering

To satisfy worldwide application requirements, SLICOFI-2 offers integrated metering injection of either 12 or 16 kHz signals with programmable amplitudes. SLICOFI-2 also has an integrated adaptive TTX notch filter and can switch the TTX signal to the line in a smooth way. When switching the signal to the line, the switching noise is less than 1 mV. **Figure 2-17** shows the TTX bursts at certain points of the signal flow within SLICOFI-2.

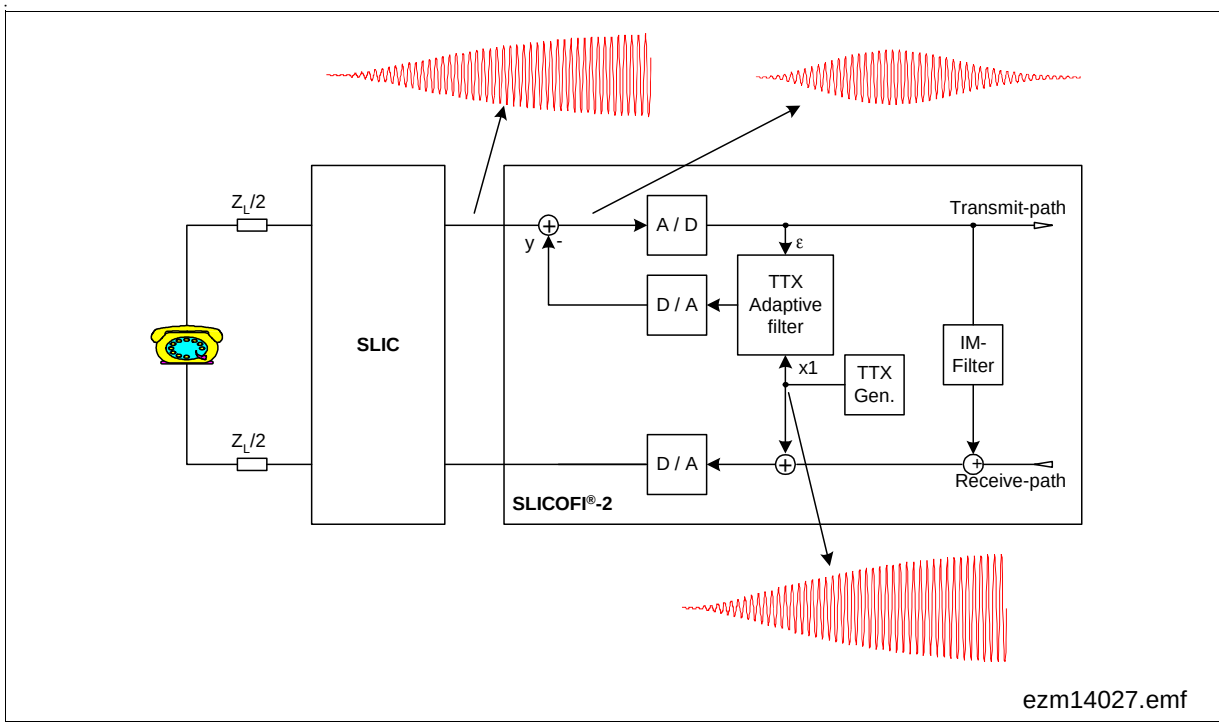


Figure 2-17 Teletax Injection and Metering

The integrated, adaptive TTX notch filter guarantees an attenuation of > 40 dB. No external components for filtering TTX bursts are required.

2.6.2 Metering by Polarity Reversal

SLICOFI-2 also supports metering by changing the actual polarity of the voltages on the TIP/RING lines. Metering with polarity reversal is usually used for pay phones (coin lines). Every time the polarity changes, a magnet in the pay phone releases a coin.

2.6.2.1 Soft reversal

Some applications require a smooth polarity reversal (soft reversal), as shown in **Figure 2-18**. Soft reversal helps to prevent negative effects like non-required ringing. Soft reversal is deactivated by the SOFT-DIS bit in register BCR2.

SOFT-DIS = 1	Immediate reversal is performed (hard reversal)
SOFT-DIS = 0	Soft reversal is performed. Transition time (time from START to SR-END1, see **Figure 2-18**) is programmable by CRAM-coefficients, default value 80 ms.

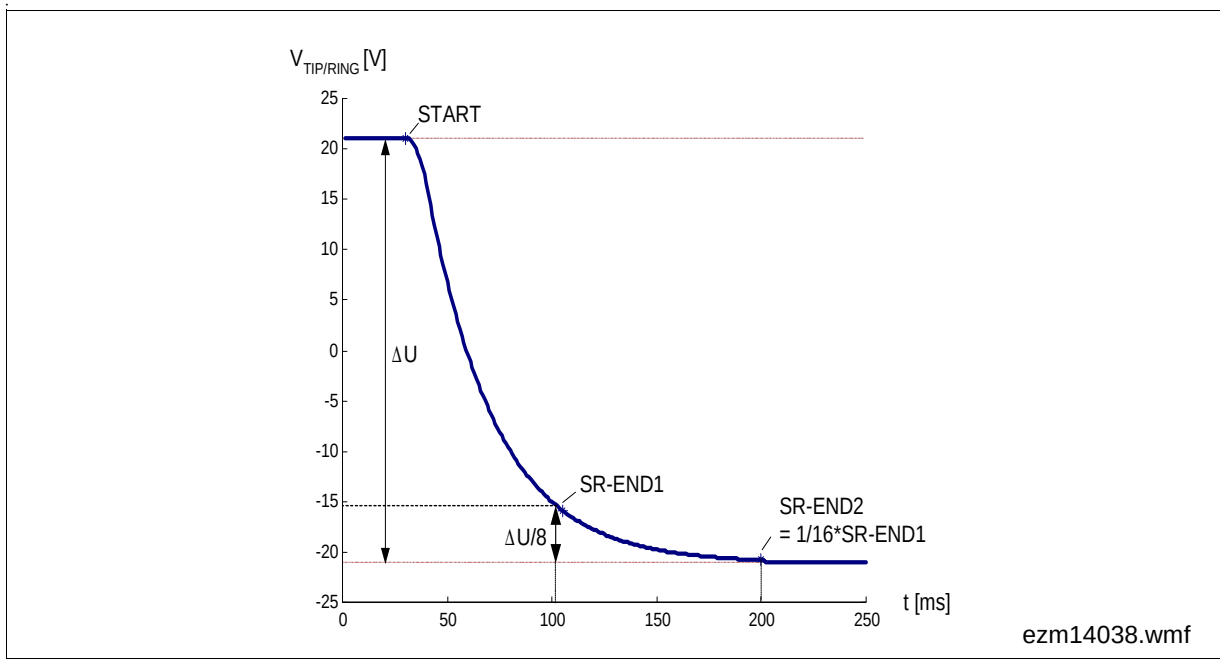


Figure 2-18 Soft Reversal (Example for Open Loop)

START: The soft ramp starts by setting the REVPOL bit in register BCR1 to 1. The DC characteristic is switched off.
SR-END1: At the soft reversal end one point, the DC characteristic is switched on again. Programmable by the DuSLICOS software, e.g. ΔU/8.
SR-END2: At the soft reversal end two point, the soft ramp is switched off. Programmable by the DuSLICOS software, e.g. 1/16*SR-END1.

2.7 Signaling (Supervision)

Signaling in the subscriber loop is monitored internally by the DuSLIC chip set.

Supervision is performed by sensing the longitudinal and transversal line currents on the Ring and Tip wires. The scaled values of these currents are generated in the SLIC and fed to the SLICOFI-2 via the IT and IL pins.

Transversal line current: $(I_R + I_T) / 2$
Longitudinal line current: $(I_R - I_T) / 2$
where I_R, I_T are the loop currents on the Ring and Tip wires.

Off-hook Detection

Loop start signaling is the most common type of signaling. The subscriber loop is closed by the hook switch inside the subscriber equipment. In active mode, the resulting transversal loop current is sensed by the internal current sensor in the SLIC. The IT pin of the SLIC indicates the subscriber loop current to the SLICOFI-2. An external resistor ($R_{IT1,}$ $R_{IT2,}$ see **Figure 6-1**) converts the current information to a voltage on the ITA (or ITB) pin. The analog information is first converted to a digital value. It is then filtered and processed further which effectively suppresses line disturbances. If the result exceeds a programmable threshold, an interrupt is generated to indicate off-hook detection.

A similar mechanism is used in Power Down mode. In this mode, the internal current sensor is switched off to minimize power consumption. The loop current is therefore fed and sensed through 5 kΩ resistors. The information is made available on the IT pin and interpreted by the SLICOFI-2.

In applications using ground start loop signaling, DuSLIC can be set in the ground start mode. In this mode, the Tip wire is switched to high impedance mode. Ring ground detection is performed by the internal current sensor in the SLIC and transferred to to the SLICOFI-2 via the IT pin.

Ground Key Detection

The scaled longitudinal current information is transferred from the SLIC via the IL pin and the external resistor R_{IL} to the SLICOFI-2. This voltage is compared with a fixed threshold value. For the specified R_{IL} (1.6 kΩ, see application circuit **Figure 6-1**) this threshold corresponds to 17 mA (positive and negative). After further post-processing, this information generates an interrupt and ground key detection is indicated.

The post-processing is performed to guarantee ground key detection, even if longitudinal AC currents with frequencies of 16 2/3, 50 or 60 Hz are superimposed. The time delay between triggering the ground key function and registering the ground key interrupt will in most cases (f = 50 Hz, 60 Hz) be less than 40 ms.

In Power Down mode, the SLIC's internal current sensors are switched off and ground key detection is disabled.

2.8 DuSLIC Enhanced Signalprocessing Capabilities

The signal processing capabilities described in this chapter are realized by an Extended Digital Signal Processor (EDSP) except DTMF generation. Each function can be individually enabled or disabled for each DuSLIC channel. Therefore power consumption can be reduced according the needs of the application.

Figure 2-19 shows the AC signal path for DuSLIC with the ADCs and DACs, impedance matching loop, thranshybrid filter, gain stages and the connection to the EDSP.

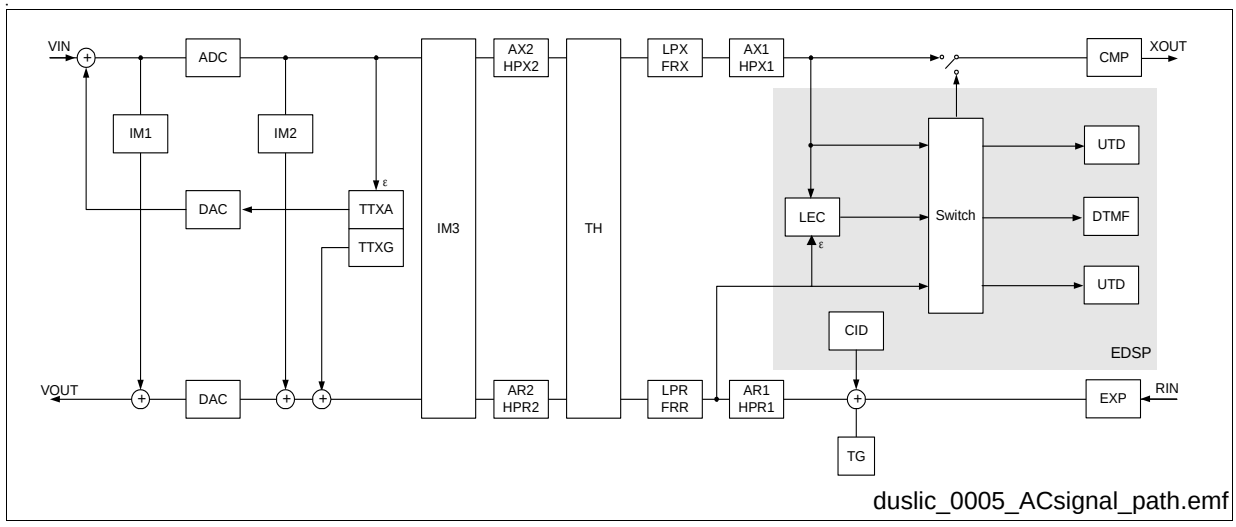


Figure 2-19 DuSLIC AC Signal Path

2.8.1 DTMF Generation and Detection

Dual Tone Multi-Frequency (DTMF) is a signaling scheme using voice frequency tones to signal dialing information. A DTMF signal is the sum of two tones, one from a low group (697-941 Hz) and one from a high group (1209-1633 Hz), with each group containing four individual tones. This scheme allows 16 unique combinations. Ten of these codes represent the numbers from zero through nine on the telephone keypad, the remaining six codes (*,#,A,B,C,D) are reserved for special signaling. The buttons are arranged in a matrix, with the rows determining the low group tones, and the columns determining the high group tone for each button.

In SLICOFI-2, all 16 standard DTMF tone pairs can be generated independent in each channel via two integrated tone generators. Alternatively the frequency and the amplitude of the tone generators can be programmed individually via the digital interface. Each tone generator can be switched on and off. The generated DTMF tone signals meet the frequency variation tolerances specified in the ITU-T Q.23 recommendation.

Both channels A and B of SLICOFI-2 have a powerful built-in DTMF decoder that will meet most national requirements. The receiver algorithm performance meets the quality criteria for central office / exchange applications. It complies with the requirements of ITU-T Q.24, "Deutsche Telekom" network (BAPT 223 ZV 5, Approval Specification of the

Federal Office for Post and Telecommunications, Germany) and Bellcore GR-30-CORE (TR-NWT-000506).

The performance of the algorithm can be adapted according the needs of the application via the digital interface (detection level, twist, bandwith and center frequency of the notch filter). **Table 2-4** shows the performance characteristics of the DTMF decoder algorithm:

Table 2-4 Performance Characteristic of SLICOFI-2 DTMF Decoder Algorithm

	Characteristics	Value	Notes
1	Valid input signal detection level	- 48 to 0 dBm0	Programmable
2	Input signal rejection level	- 5 dB of valid signal detection level	
3	Positive twist accept	< 8 dB	Programmable
4	Negative twist accept	< 8 dB	Programmable
5	Frequency deviation accept	< ± (1.5 % + 4 Hz) and <±1.8 %	Related to center frequency
6	Frequency deviation reject	> ± 3%	Related to center frequency
7	DTMF noise tolerance (could be the same as 14)	-12 dB	dB referenced to lowest amplitude tone
8	Minimum tone accept duration	40 ms	
9	Maximum tone reject duration	25 ms	
10	Signaling velocity	≥ 93 ms/digit	
11	Minimum inter-digit pause duration	40 ms	
12	Maximum tone drop-out duration	20 ms	
13	Interference rejection 30 Hz to 480 Hz for valid DTMF recognition	Level in frequency range 30 Hz...480 Hz ≤ Level of DTMF frequency - 22 dB	dB referenced to lowest amplitude tone
14	Gaussian noise influence Signal level -22 dBm0, SNR = 23 dB	Error rate better than 1 in 10000	
15	Pulse noise influence Impulse noise tape 201	Error rate better than 14 in 10000	

In the event of pauses < 20 ms:

- If the pause is followed by a tone pair with the same frequencies as before, this is interpreted as drop-out.
- If the pause is followed by a tone pair with different frequencies and if all other conditions are valid, this is interpreted as two different numbers.

DTMF decoders can be switched on or off individually to reduce power consumption. In normal operation, the decoder monitors the Tip and Ring wires via the ITAC pins (transmit path). Alternatively the decoder can be switched also in the receive path. On detecting a valid DTMF tone pair, SLICOFI-2 generates an interrupt via the appropriate INT pin and indicates a change of status. The DTMF code information is provided by a register read via the digital interface.

The DTMF decoder also has excellent speech-rejection capabilities and complies with Bellcore TR-TSY-000763. The algorithm has been fully tested with the speech sample sequences in the Series-1 Digit Simulation Test Tapes for DTMF decoders from Bellcore.

2.8.2 Caller ID Generation

A generator to send calling line identification (Caller ID, CID) is integrated in the DuSLIC chip set. Caller ID is a generic name for the service provided by telephone utilities that supply information like the telephone number or the name of the calling party to the called subscriber at the start of a call. In call waiting, the Caller ID service supplies information about a second incoming caller to a subscriber already busy with a phone call.

In typical Caller ID (CID) systems, the coded calling number information is sent from the central exchange to the called phone. This information can be shown on a display on the subscriber telephone set. In this case, the Caller ID information is usually displayed before the subscriber decides to answer the incoming call. If the line is connected to a computer, caller information can be used to search in databases and additional services can be offered.

There are two methods used for sending CID information depending on the application and country specific requirements:

- Caller ID generation using DTMF signaling (see **Chapter 2.8.1**)
- Caller ID generation using FSK

.

DuSLIC contains DTMF generation units and FSK generation units which can be used for both channels simultaneously.

DuSLIC FSK Generation

Different countries use different standards to send Caller ID information. The SLICOFI-2 chip set is compatible with the widely used standards, Bellcore GR-30-CORE, British Telecom (BT) SIN227, SIN242 or the UK Cable Communications Association (CCA) specification TW/P&E/312. A continuous phase binary frequency shift keying (FSK) modulation is used for coding which is compatible with BELL 202 (see **Table 2-5**) and ITU-T V.23, the most common standards. SLICOFI-2 can be easily adapted to these requirements by programming via the microcontroller interface. Coefficient sets are provided for the most common standards.

Table 2-5 FSK Modulation Characteristics

Characteristic	ITU-T V.23	Bell 202
Mark (Logic 1):	1300 ± 3 Hz	1200 ± 3 Hz
Space (Logic 0):	2100 ± 3 Hz	2200 ± 3 Hz
Modulation:	FSK	
Transmission rate:	1200 ± 6 baud	
Data format:	Serial binary asynchronous	

The Caller ID data of the calling party can be transferred via the microcontroller interface into a SLICOFI-2 buffer register. An FSK enable signal, together with the first write operation into the buffer register, will start sending the FSK data when the amount of data in the buffer register exceeds the buffer request size plus two. The data transfer into the buffer register is handled by a SLICOFI-2 interrupt signal. Caller data is transferred from the buffer via the interface pins to the SLIC and fed to the Tip and Ring wires.

DuSLIC offers two different levels of framing:

- A basic low level framing mode

  All the data necessary to implement the FSK data stream - including channel seizure, mark sequence and framing for the data packet or checksum - has to be configured by firmware. SLICOFI-2 transmits the data stream in the same order in which the data is written to the buffer register.

- A high level framing mode

  The number of cannel seizure and mark bits can be programmed and are automatically sent by the DuSLIC. Only the data packet information has to be written into the CID buffer.

The example below shows signaling of CID on-hook data transmission in accordance with Bellcore specifications. The Caller ID information applied on Tip and Ring is sent during the period between the first and second ring burst.

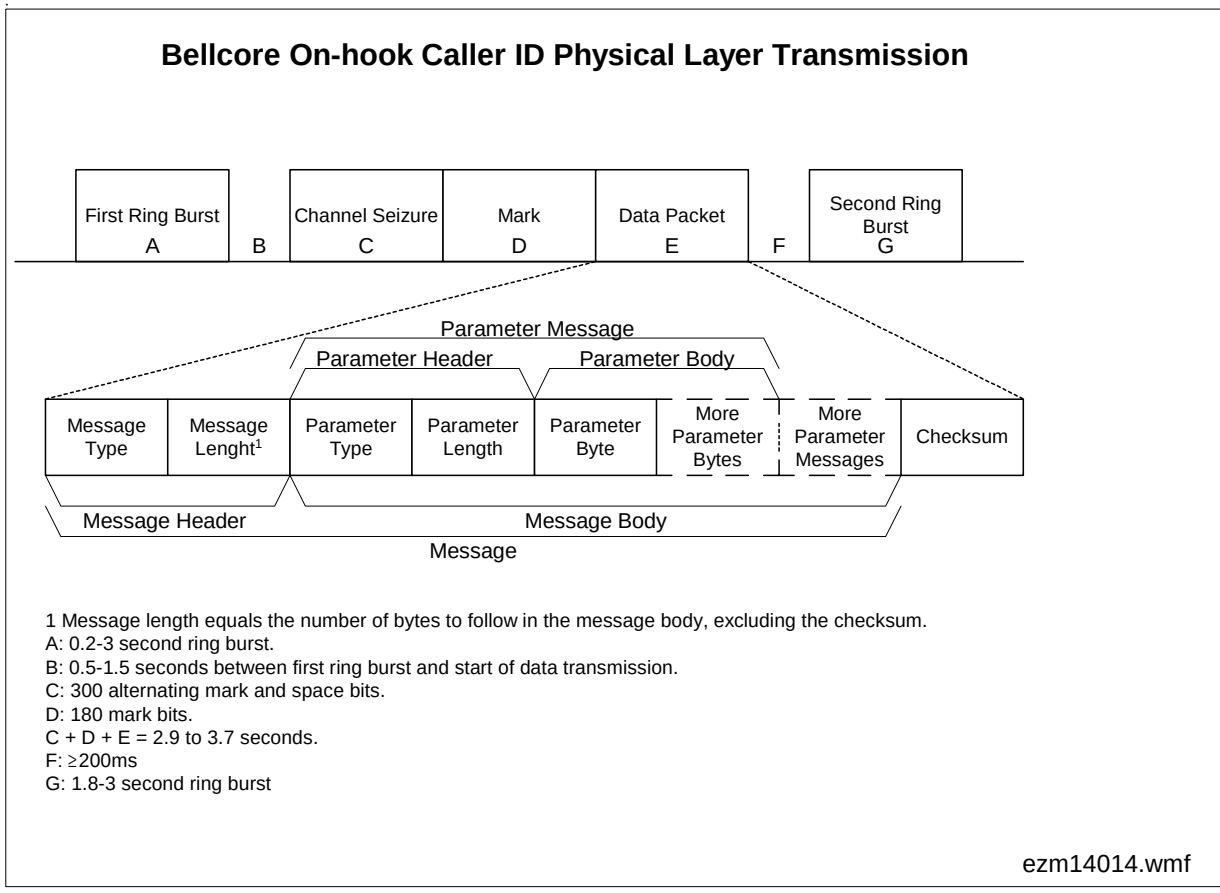


Figure 2-20 Bellcore On-hook Caller ID Physical Layer Transmission

2.8.3 Line Echo Cancelling (LEC)

The DuSLIC contains an adaptive line echo cancellation unit for the cancellation of near end echoes. With the adaptive balancing of the LEC unit the transhybrid loss can be improved up to a value of about 50 dB. The maximum echo length considered is 8 ms. The 8 ms cancellation is available for each channel only when no further signal processing functions of the EDSP are used. The line echo cancellation unit is especially useful in front of the DTMF detection unit. In critical situations the performance of the DTMF detection can be improved.

If for both DuSLIC channels DTMF detection and LEC are used the maximum line echo lenght for the LEC is reduced to 4 ms.

The DuSLIC line echo canceller is compatible with applicable standards ITU-T G.165 and G.168 with the restriction that a longer echo cancelling path than 8 ms cannot be realized.

The LEC unit consists basically of a FIR filter and a shadow FIR filter and a coefficient adaption mechanism between these two filters as shown in **Figure 2-21**.

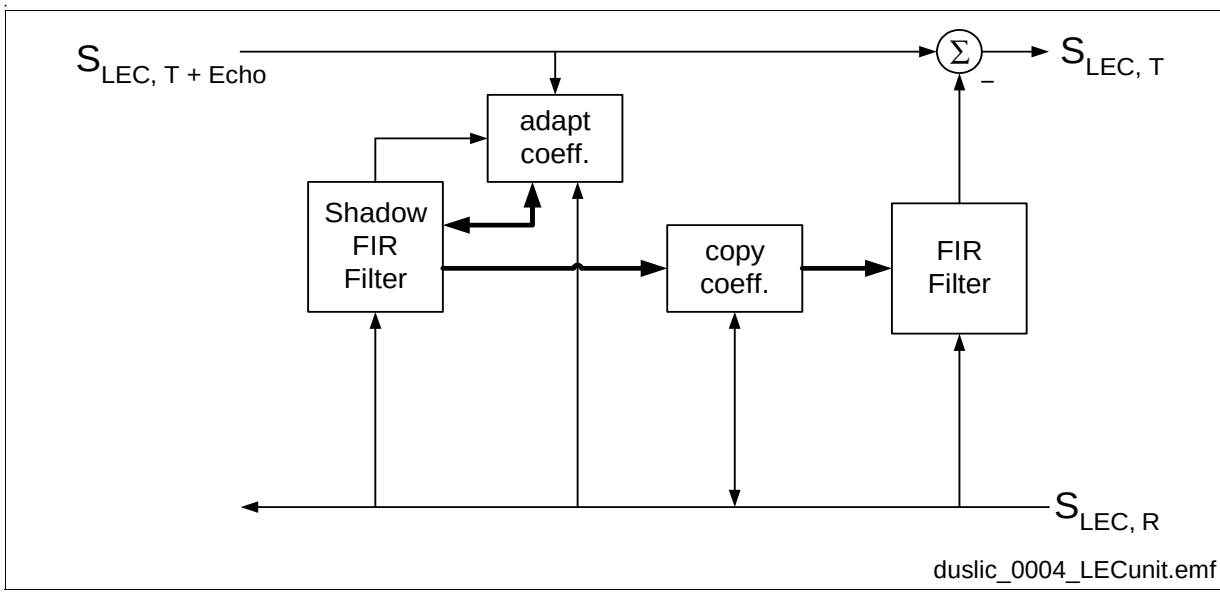


Figure 2-21 Line Echo Cancellation Unit - Block Diagram

The adaption process is controlled by the three parameters Pow_{LECR} (Power Detection Level Receive), $DeltaP_{LEC}$ (Delta Power) and DeltaQ (Delta Quality). Adaption takes place only if both of the following conditions hold:

1. $S_{LEC, R} > Pow_{LECR}$
2. $S_{LEC, R} - S_{LEC, T} > DeltaP_{LEC}$

With the first condition, adaption to small signals can be avoided. The second condition avoids adaption during double talk. The parameter $DeltaP_{LEC}$ represents the echo loss provided by external circuitry.

If the adaption of the shadow filter is performed better than the adaption of the actual filter by a value of more than DeltaQ then the shadow filter coefficients will be copied to the actual filter.

At the start of an adaption process the coefficients of the LEC unit can be set to default initial values or set to the old coefficient values. A freezing of the coefficients can also be performed.

2.8.4 Universal Tone Detection (UTD)

DuSLIC has an Universal Tone Detection (UTD) unit which can be used to detect special tones in the receive and transmit path especially fax or modem tones (e.g. see the modem startup sequence described in recommendation ITU-T V.8).

This allows to use modem optimized filter coefficients if an V.34 or V.90 connection takes place. If the DuSLIC UTD detects that a modem connection will take place, the optimized

filter coefficients for the modem connection can be downloaded before the modem connection is set up. With this mechanism implemented in the DuSLIC chipset always the optimum modem transmission rate can be achieved.

Figure 2-22 shows the functional block diagram of the UTD unit:

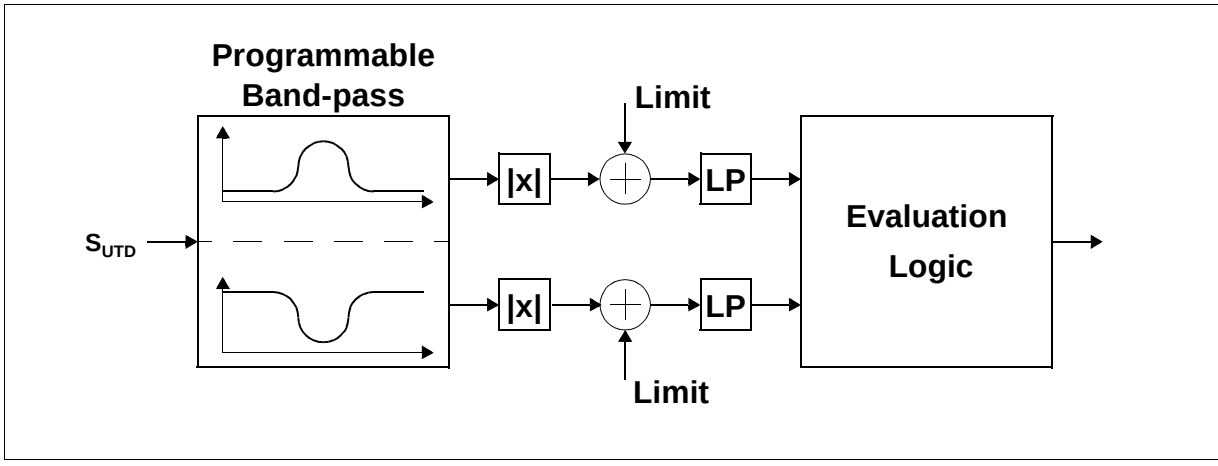


Figure 2-22 UTD Functional Block Diagram

Initially, the input signal is filtered by a programmable band-pass (center frequency f_C and band width f_{BW}). Both the in-band signal (upper path) and the out-of-band signal (lower path) are determined and the absolute value is calculated. Both signals are furthermore filtered by a limiter and a low-pass. All signal samples (absolute values) below a programmable limit Lev_N (Noise Level) are set to zero and all other signal samples are diminished by Lev_N. The purpose of this limiter is to increase noise robustness. After the limiter stages both signals are filtered by a fixed low pass.

The evaluation logic block determines when a tone interval or silence interval is detected and an interrupt is generated for the receive or transmit path.

The status bit will be set if both of the following conditions hold for at least time RTime without breaks exceeding time AGAPTime:

1. The in-band signal exceeds a programmable level Lev_S
2. The difference of the in-band and the out-of-band signal levels exceeds $Delta_{UTD}$

The status bit will be reset if at least one of these conditions is violated by at least time RGAPTime without breaks exceeding ABREAKTime.

The times AGAPTime and ABREAKTime help to reduce the effects of sporadic dropouts.

If the Bandwith parameter f_{BW} is programmed to a negative value the UTD unit can be used for the detection of silence intervals in the whole frequency range.

The DuSLIC UTD unit is compatible with ITU-T G.164.

The UTD is resistent against a modulation with 15 Hz sinusoidal signals and a phase reversal but is not able to detect the 15 Hz modulation and the phase reversal.

2.9 Message Waiting Indication

Message Waiting is a function that can be required by PBX applications. A Message Waiting Indication (MWI) lamp is activated indicating to the subscriber that a message has arrived.

The DuSLIC Message Waiting function uses a glow lamp at the subscriber phone. Current does not flow through a glow lamp until the voltage reaches a threshold value of approximately 80 V. At this threshold, the neon gas in the lamp will start to glow. When the voltage is reduced, the current falls under a certain threshold and the lamp is extinguished. DuSLIC has high-voltage SLIC technology (170 V) which is able to activate the glow lamp without any external components.

The hardware circuitry is shown in **Figure 2-23** below. The figure shows a typical telephone circuit with the hook switch in the on-hook mode, together with the impedances for the on-hook (Z_R) and off-hook (Z_L) modes.

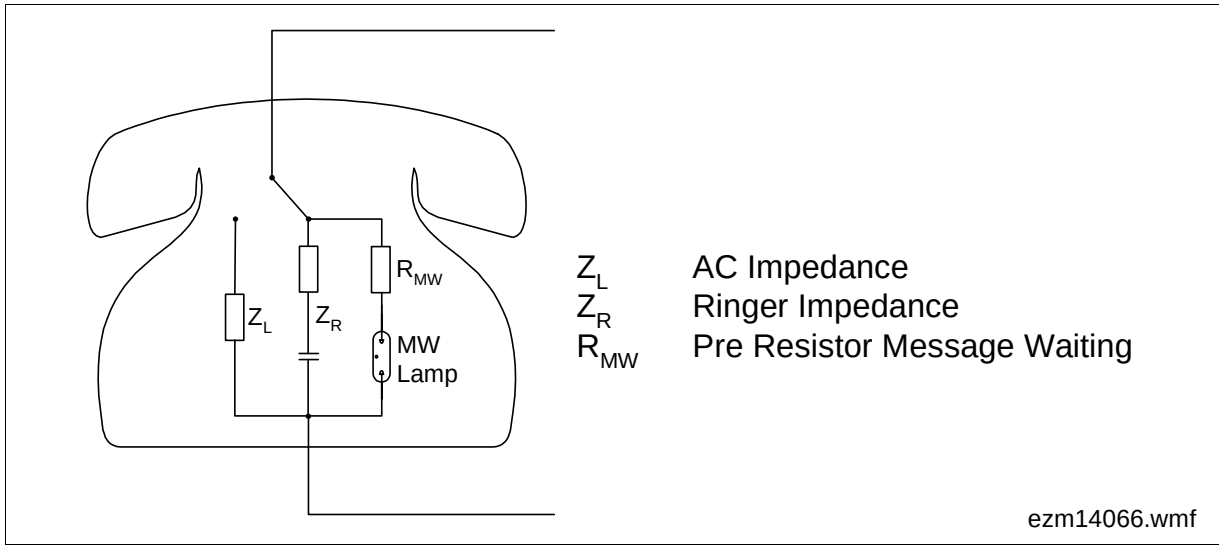


Figure 2-23 MWI Circuitry with Glow Lamp

The glow lamp circuit also requires a resistor (R_{MW}) and a lamp (MW Lamp) built into the phone. When activated, the lamp must be able to either blink or remain on constantly .

In non-DuSLIC solutions, the telephone ringer may respond briefly if the signal slope is too steep, which is not desirable. DuSLIC's integrated ramp generator increases the voltage slowly, to ensure activating the lamp and not the ringer.

2.10 Three-party Conferencing

Each DuSLIC channel has a three-party conferencing facility consisting of four PCM registers, adders and gain stages in the microprogram and the corresponding control registers (see **Figure 2-24**). Three-party conferencing is available in PCM/µC-mode only.

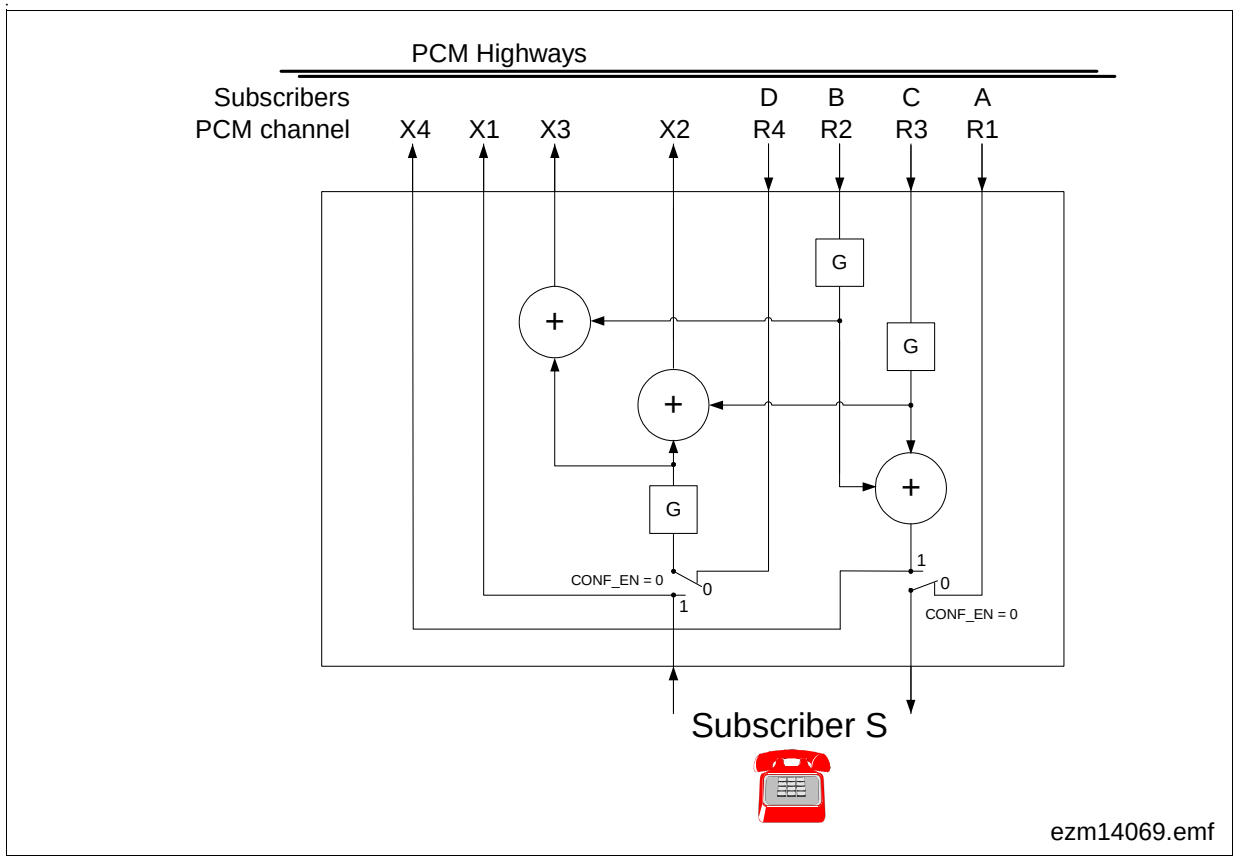


Figure 2-24 Conference Block for one DuSLIC Channel

Note: G...Gain Stage (Gain Factor),
X1-X4...PCM transmit channels, R1-R4...PCM receive channels,
A, B, C, D, S...examples for voice data on PCM channels X1-X4, R1-R4

Table 2-6 shows all possible three party conferencing modes and the corresponding selection of the PCM transmit and receive channels X1 to X4 and R1 to R4 (see also **Figure 2-24**). The timeslot assignment, the PCM-highway selection, the PCM line drivers and the behaviour of the conferencing facility itself are controled by various registers[1)]. A programmable gain stage G is able to adjust the gain of the conferencing voice data (B, C, D, S) in a range of -6 dB to +3 dB to prevent overload of the sum signals.

1) not to be explained in this document.

Table 2-6 Conference Modes

	Receive PCM Channels				Transmit PCM Channels				
Mode	**R1**	**R2**	**R3**	**R4**	**X1**	**X2**	**X3**	**X4**	**Subscriber S**
PCM Off					off	off	off	off	off
PCM Active	A				S	off	off	off	A
External Conference		B	C	D	off	G·(B+D)	G·(C+D)	G·(B+C)	off
External Conference + PCM Active	A	B	C	D	S	G·(B+D)	G·(C+D)	G·(B+C)	A
Internal conference		B	C		off	G·(B+S)	G·(C+S)	off	G·(B+C)

- **PCM Off**
  After reset or in power down mode no communication is performed via the PCM highways. Also when selecting new timeslots it is recommended to switch off the PCM line drivers by setting the control bits to zero.
- **PCM Active**
  This is the normal operating mode without conferencing. Only the PCM channels R1 and X1 are in use and voice data is transferred from subscriber A to analog subscriber S and vice versa.
- **External Conference**
  In this mode, SLICOFI-2 acts as a server for a three-party conference of subscribers B, C and D from any device connected to the PCM highways. The SLICOFI-2 channel can remain in the Power Down mode to lower power consumption.
- **External Conference + PCM Active**
  As with the external conference mode, any external three-party conference can be performed. At the same time an internal phone call is active using the PCM channels R1 and X1.
- **Internal Conference**
  If the analog subscriber S is one of the conference partners, the internal conference mode is selected. The partners (B, C) do not need any conference facility of their own, since SLICOFI-2 performs all the necessary additions.

2.11 16 kHz Modes on PCM Highway

In addition to the standard 8-kHz transmission PCM-interface modes, there also two 16-kHz modes for high data transmission performance. **Table 2-7** shows the configuration of the PCM channels for the different PCM interface modes.

Table 2-7 PCM/µC Interface Modes

Config. Bits		Receive PCM Channels					Transmit PCM Channels				
PCM16K	LIN	R1	R1L	R2	R3	R4	X1	X1L	X2	X3	X4
PCM Mode											
0	0	A	[1]	B	C	D	S		Depends on conference mode		
LIN Mode											
0	1	A-HB	A-LB	B	C	D	S-HB	S-LB	Depends on conference mode		
PCM16 Mode											
1	0	DS1			DS2		DS1			DS2	
LIN16 Mode											
1	1	DS1-HB		DS1-LB	DS2-HB	DS2-LB	DS1-HB		DS1-LB	DS2-HB	DS2-LB

[1] Empty cells in the table indicate unused data in the PCM receive channels and switched-off line drivers in the PCM transmit channels

The configuration bits PCM16K and LIN are used to select the following PCM interface modes:

- **PCM mode:**

Normal mode used for voice transmission via the PCM channels R1 and X1 (receive and transmit). The PCM input channels R2, R3 and R4 are always active for use in different conference configurations. The status of the PCM output channels depends on the conference mode configuration.

- **LIN mode:**

Similar to the PCM mode, but for 16-bit linear data at 8-kHz sample rate via the PCM channels R1, R1L (receive) and X1, X1L (transmit).

- **PCM16 Mode:**

Mode for higher data transmission rate of PCM-encoded data using a 16-kHz sample rate (only in PCM/µC interface mode). In this mode, the channels R1, R3 (X1, X3) are used to receive (transmit) two samples of data (DS1, DS2) in each 8-kHz frame.

- **LIN16 Mode:**

Like the PCM16 mode for the 16-kHz sample rate but for linear data. The channels R1 to R4 (X1 to X4) are used for receiving (transmitting) the high and low bytes of the two linear data samples DS1 and DS2.

3 Operational Description

3.1 Operating Modes for the DuSLIC Chipset

Sleep (SL)

In Sleep mode, off-hook is detected by an analog comparator in SLICOFI-2 and transferred via the INT or the DU-pin. The system clock can be stopped in this mode. This mode should be applied only to lines with less interference because in sleep mode no hook information filtering can take place in SLICOFI-2.

Power Down Resistive (PDR)

The Power Down resistive mode is the standard mode for non-active lines. Off-hook is detected by a current value fed to the DSP, compared with a programmable threshold and filtered by a data upstream persistence checker. The power management SLIC-P can be switched to a Power-Down-Resistive-High or a Power-Down-Resistive-Ring mode.

HIRT

In HIRT mode, SLICOFI-2 is able to perform an input offset measurement of the current sensors. The linedrivers in the SLIC are shut down and no resistors are switched to the line. Off-hook detection is not possible.

Power Down High Impedance (PDH)

In the Power Down High Impedance mode, the SLIC is totally powered down. No off-hook sensing can be performed. This mode can be used for an emergency shutdown of a line.

Active High (ACTH)

A regular call can be performed, voice and metering pulses can be transferred via the telephone line and the dc-loop is operational in the Active High mode.

Active Low (ACTL)

The Active Low mode is similar to the Active High mode. The only difference is that the SLIC uses a lower battery voltage V_{BATL} (bit ACTL = 1).

Active Ring (ACTR)

The Active Ring mode is different for SLIC-E and SLIC-P. The SLIC-E uses the addiitional positive voltage V_{HR} for extended feeding and the SLIC-P will switch to the negative battery voltage V_{BATR}.

Ringing

If SLICOFI-2 is switched to ringing mode, the SLIC is switched to ACTR mode. With SLIC-P connected to the SLICOFI-2, the Ring on Ring (ROR) mode allows unbalanced internal ringing on the Ring wire. The Tip wire is set to battery ground. The ring signal will be superimposed by V_{BATR} / 2. The Ring on Tip (ROT) mode is the equivalent to the ROR mode.

Active with HIT

This is a test mode where the Tip wire is set to a high impedance mode. It is used for special line testing. It is only available with Active on SLICOFI-2 to enable all necessary test features.

Active with HIR

HIR is the equivalent mode to HIT with the ring wire set to high impedance.

Active with Metering

Any allowed active mode can be used for metering either with Reverse Polarity or with TTX Signals.

Ground Start

The Tip wire is set to High-Impedance in Ground Start Mode. Any current drawn on the ring wire leads to a Signal on IT, indicating off-hook.

Ring Pause

The ring Burst is switched off in ring Pause, but the SLIC remains in the specified mode and the off-hook recognition behaves like in ringing Mode (Ring Trip).

3.2 Operating Modes for SLICOFI-2 and SLIC-E

Table 3-1 PEB 4265 Operating Modes

SLICOFI-2 mode	SLIC mode	SLIC internal supply voltages (+/-) [V_{HI} / V_{BI}]	System functionality	Active circuits	Tip/Ring output voltage
PDH	PDH	Open / V_{BATH}	None	None	High Impedance
Sleep	PDRH	Open / V_{BATH}	Off-hook detect via off-hook comparator	Off-hook, analog comparator	BGND / V_{BATH} (via 5kΩ)
Power Down resistive	PDRH	Open / V_{BATH}	Off-hook detect as in active mode (DSP)	Off-hook, DC-transmit path	BGND / V_{BATH} (via 5kΩ)
	PDRHL 1)	Open / V_{BATH}	Off-hook detect as in active mode (DSP)	Off-hook, DC-transmit path	BGND / V_{BATH} (via 5kΩ)
Active Low (ACTL)	ACTL	BGND / V_{BATL}	Voice and/or TTX transmission	Buffer, Sensor, DC+AC-Loop,TTX-generator (opt.)	Tip: $(V_{BATL}+V_{AC}+V_{DC}) / 2$ Ring: $(V_{BATL}-V_{AC}-V_{DC}) / 2$
Active High (ACTH)	ACTH	BGND / V_{BATH}	Voice and/or TTX transmission	Buffer, Sensor, DC+AC-Loop, TTX-generator (opt.)	Tip: $(V_{BATH}+V_{AC}+V_{DC}) / 2$ Ring: $(V_{BATH}-V_{AC}-V_{DC}) / 2$
Active Ring (ACTR)	ACTR	V_{HR} / V_{BATH}	Voice and/or TTX transmission	Buffer, Sensor, DC+AC-Loop, TTX-generator (opt.)	Tip: $(V_{BATH}+V_{HR}+V_{AC}+V_{DC}) / 2$ Ring: $(V_{BATH}+V_{HR}-V_{AC}-V_{DC}) / 2$
Ringing (Ring)	ACTR	V_{HR} / V_{BATH}	Balanced Ring signal feed (incl. DC-offset)	Buffer, Sensor, DC-Loop, ring generator	Tip: $(V_{BATH}+V_{HR}+V_{DC}+V_{AC}) / 2$ Ring: $(V_{BATH}+V_{HR}-V_{DC}-V_{AC}) / 2$
Ring Pause	ACTR	V_{HR} / V_{BATH}	DC-offset feed	Buffer, Sensor, DC-Loop, ramp generator	Tip: $(V_{BATH}+V_{HR}+V_{DC}+V_{AC}) / 2$ Ring: $(V_{BATH}+V_{HR}-V_{DC}-V_{AC}) / 2$

Table 3-1 PEB 4265 Operating Modes

SLICOFI-2 mode	SLIC mode	SLIC internal supply voltages (+/-) [V_{HI} / V_{BI}]	System functionality	Active circuits	Tip/Ring output voltage
HIRT	HIRT	V_{HR} / V_{BATH}	E.g. sensor offset calibration	Sensor, DC-transmit path	High Impedance
Active with HIR	HIR	V_{HR} / V_{BATH}	E.g. line test (Tip)	Tip-Buffer, Sensor, DC+AC-Loop	Tip: (V_{BATH}+V_{HR}+V_{AC} +V_{DC}) / 2 Ring: high impedance
Active with HIT	HIT	V_{HR} / V_{BATH}	E.g. line test (Ring)	Ring-Buffer, Sensor, DC+AC-Loop	Ring: (V_{BATH}+V_{HR}- V_{AC} -V_{DC}) / 2 Tip: high impedance

[1] load ext. C for switching from PDRH to ACTH in onhookmode

V_{AC}.....Tip / Ring AC Voltage

V_{DC}.....Tip / Ring DC Voltage

3.3 Operating Modes for SLICOFI-2 and SLIC-P

Table 3-2 PEB 4266 Operating Modes

SLICOFI-2 mode	SLIC mode	SLIC internal supply voltages (+/-) [V_{BI}]	System functionality	Active circuits	Tip/Ring output voltage
PDH	PDH	V_{BATR}	None	None	High Impedance
Sleep	PDRH	V_{BATH}	Off-hook detect via off-hook comparator	Off-hook, analog comparator	BGND / V_{BATH} (via 5kΩ)
Sleep	PDRR	V_{BATR}	Off-hook detect via off-hook comparator	Off-hook, analog comparator	BGND / V_{BATH} (via 5kΩ)
Power Down resistive	PDRH	V_{BATH}	Off-hook detect as in active mode (DSP)	Off-hook, DC-transmit path	BGND / V_{BATH} (via 5kΩ)
	PDRHL [1)]	V_{BATH}	Off-hook detect as in active mode (DSP)	Off-hook, DC-transmit path	BGND / V_{BATH} (via 5kΩ)
	PDRR	V_{BATR}	Off-hook detect as in active mode (DSP)	Off-hook, analog comparator	BGND / V_{BATR} (via 5kΩ)
	PDRRL [2)]	V_{BATR}	Off-hook detect as in active mode (DSP)	Off-hook, DC-transmit path	BGND / V_{BATR} (via 5kΩ)
Active Low (ACT)	ACTL	V_{BATL}	Voice and/or TTX transmission	Buffer, Sensor, DC+AC-Loop,TTX-generator (opt.)	Tip: $(V_{BATL}+V_{AC}+V_{DC}) / 2$ Ring: $(V_{BATL}-V_{AC}-V_{DC}) / 2$
Active High (ACT)	ACTH	V_{BATH}	Voice and/or TTX transmission	Buffer, Sensor, DC+AC-Loop, TTX-generator (opt.)	Tip: $(V_{BATH}+V_{AC}+V_{DC}) / 2$ Ring: $(V_{BATH}-V_{AC}-V_{DC}) / 2$
Active Ring (ACT)	ACTR	V_{BATR}	Voice and/or TTX transmission	Buffer, Sensor, DC+AC-Loop, TTX-generator (opt.)	Tip: $(+V_{BATR}+V_{AC}+V_{DC}) / 2$ Ring: $(+V_{BATR}-V_{AC}-V_{DC}) / 2$
Ringing (Ring)	ACTR	V_{BATR}	Balanced ring signal feed (incl. DC-offset)	Buffer, Sensor, DC-Loop, ring generator	Tip: $(V_{BATR}+V_{DC}+V_{AC}) / 2$ Ring: $(V_{BATR}-V_{DC}-V_{AC}) / 2$

Table 3-2 PEB 4266 Operating Modes

SLICOFI-2 mode	SLIC mode	SLIC internal supply voltages (+/-) [V_{BI}]	System functionality	Active circuits	Tip/Ring output voltage
Ringing (Ring)	ROR	V_{BATR}	Ring signal on ring, Tip on BGND	Buffer, Sensor, DC-Loop, ring generator	Ring: $(V_{BATR}-V_{DC}-V_{AC}) / 2$ Tip: 0V
Ringing (Ring)	ROT	V_{BATR}	Ring signal on ring, Tip on BGND	Buffer, Sensor, DC-Loop, ring generator	Ring: $(V_{BATR}+V_{DC}+V_{AC}) / 2$ Tip: 0V
Ring Pause	ACTR, ROR, ROT	V_{BATR}	DC-offset feed	Buffer, Sensor, DC-Loop, ramp generator	Tip: $(V_{BATR}+V_{DC}+V_{AC}) / 2$ Ring: $(V_{BATR}-V_{DC}-V_{AC}) / 2$
HIRT	HIRT	V_{BATR}	E.g. sensor offset calibration	Sensor, DC-transmit path	High Impedance
Active with HIR	HIR	V_{BATR}	E.g. line test (Tip)	Tip-Buffer, Sensor, DC+AC-Loop	Tip: $(V_{BATR}+V_{AC}+V_{DC}) / 2$ Ring: high impedance
Active with HIT	HIT	V_{BATR}	E.g. line test (Ring)	Ring-Buffer, Sensor, DC+AC-Loop	Ring: $(V_{BATR}-V_{AC}-V_{DC}) / 2$ Tip: high impedance

1) load ext. C for switching from PDRH to ACTH in onhookmode

2) load ext. C for switching from PDRR to ACTR in onhookmode

3.4 Operating Modes and Power Management

In many applications, the power dissipated on the line card is a critical parameter. In larger systems, the mean power value (taking into account traffic statistics and line length distribution) determines cooling requirements. Particularly in remotely fed systems, the maximum power for a line must not exceed a given limit.

3.4.1 Introduction

Generally, system power dissipation is determined mainly by the high-voltage part. The most effective power-saving method is to limit SLIC functionality and reduce supply voltage in line with requirements. This is achieved using different operating modes.
The three main modes - Power Down, Active and Ringing - correspond to the main system states: on-hook, signal transmission (voice and/or TTX) and Ring signal feed.

For power critical applications the SLEEP mode can be used for even lower power consumption than in Power Down Mode.

– Power Down

Off-hook detection is the only function available. It is realized by 5 kΩ resistors applied by the SLIC from Tip to V_{BGND} and Ring to V_{BAT}, respectively. A simple sensing circuit supervises the DC current through these resistors (zero in on-hook and non-zero in off-hook state). This scaled transversal line current is transferred to the IT pin and compared with a programmable current threshold in the SLICOFI-2. Only the DC loop in the SLICOFI-2 is active.

In **Sleep** mode, all functions of the SLICOFI-2 are switched off except for Off-hook detection which is still available via an analog comparator. Both AC and DC loops are inactive. To achieve the lowest power consumption of the DuSLIC chip set the clock cycles fed to the MCLK and PCLK pins have to be shut off (see **Table 3-3**).
For changing into another state the DuSLIC has to be waked up.

– Active

Both AC and DC loops are operative. The SLIC provides low-impedance voltage feed to the line. The SLIC senses, scales and separates transversal (metallic) and longitudinal line currents. The voltages at Tip and Ring are always symmetrical with reference to half the battery voltage (no ground reference!). An integrated switch makes it possible to choose between two (PEB 4265) or even three (PEB 4266) different battery voltages. With these voltages selected according to certain loop lengths, power optimized solutions can be achieved.

– Ringing

For SLIC-E, an auxiliary positive supply voltage V_{HR} is used to give a total supply range of up to 150 V. For SLIC-P the whole supply range is provided by V_{BATR}. Low impedance line feed (~ 61 Ω output impedance, R_{STAB} included) with a balanced sinusoidal Ring signal of up to 85 V_{RMS}, plus a DC offset of 20 V, is sufficient to supply very long lines at any kind of ringer load and to reliable detect Ring trip. Unbalanced ringing is supported by applying the Ring signal to only one line, while Ground is applied to the other line.

For an overview of all DuSLIC operating modes see **Table 3-1** for PEB 4265 and **Table 3-2** for PEB 4266.

3.4.2 Power Dissipation of the SLICOFI-2

For an optimized power consumption unused EDSP functions have to be switched off.

Table 3-3 shows typical power dissipation values for different operating modes of the SLICOFI-2. For more detailed characteristics, see the DuSLIC Data Sheet.

Table 3-3 SLICOFI-2 Power Dissipation (Typical Values)

Mode	Value	Condition
Sleep (both channels)	< 20 mW	with clock rate at pins MCLK, PCLK (f_{MCLK} = f_{PCLK} = 2 MHz)
Power Down both channels	< 70 mW	
Active one channel (non active channel in Sleep Mode)	115 mW 130 mW 145 mW	without EDSP (EDSP-EN = 0) with EDSP 8 MIPS (DTMF detection one channel) with EDSP 16 MIPS (DTMF detection two channels)
Active both channels	180 mW 250 mW	without EDSP (EDSP-EN = 0) with EDSP 32 MIPS

Table 3-4 SLICOFI-2S Power Dissipation (Typical Values)

Mode	Value	Condition
Sleep (both channels)	< 20 mW	with clock rate at pins MCLK, PCLK (f_{MCLK} = f_{PCLK} = 2 MHz)
Power Down both channels	< 70 mW	
Active one channel	115 mW	(non active channel in Sleep Mode)
Active both channels	180 mW	

3.4.3 Power Dissipation of the SLIC

The SLIC power dissipation mainly comes from internal bias currents and the buffers output stage (to a less extent from the sensor) where additional power is dissipated whenever current is fed to the line.

3.4.3.1 Power Down Modes

In Power Down modes, the internal bias currents are reduced to a minimum value and no current is fed to the line (see **Table 3-7**, **Table 3-9** and **Table 3-11**). Even with active off-hook detection the power dissipation of 5 mW (6 mW for SLIC-P) is negligible. Note that this is the dominant factor for low mean power value in large systems, as a large percentage of lines are always inactive.

3.4.3.2 Active Mode

In Active mode, the selected battery voltage V_{BAT} has the strongest influence on power dissipation. The power dissipation in the output stage PO is determined by the difference between V_{BAT} and the Tip-Ring voltage $V_{TIP/RING}$. At constant DC line current I_{Trans}, the shortest lines (lowest R_L) cause lowest $V_{TIP/RING}$, and accordingly exhibit the highest on-chip power dissipation. However, the minimum battery voltage required is determined by the longest line and therefore the maximum line resistance $R_{L,MAX}$ including R_{PROT} and R_{STAB}.

$$V_{BAT,min} = I_{Trans} \times (R_{L,MAX} + R_{PROT} + R_{STAB}) + V_{AC,P} + V_{DROP}$$

$V_{AC,P}$.....Peak value of AC signal

V_{DROP} .....Sum of voltage drop in the SLIC buffers (**Table 3-5**)

Table 3-5 Typical Buffer Voltage Drops (Sum) (for I_{TRANS} ($I_{T\ or\ R}$) in [mA])

Mode	Total voltage drop V_{DROP} [V]	
	SLIC-E/S	**SLIC-P**
ACTL	I_{TRANS} * 0.096	I_{TRANS} * 0.088
ACTH	I_{TRANS} * 0.1	I_{TRANS} * 0.1
ACTR	(I_{TRANS} * 0.1) + 1	I_{TRANS} * 0.092
ROR, ROT	-	I_{TRANS} * 0.092
HIR, HIT	($I_{T\ or\ R}$ * 0.048) + 1	$I_{T\ or\ R}$ * 0.052

The most efficient way to reduce short loop power dissipation is to use a second battery voltage of lower value (V_{BATL}), whenever line resistance is small enough. This method is

supported on the PEB 4265 by integrating a battery switch. With a standard battery voltage of -48 V, long lines up to 2 kΩ can be driven at 20 mA line current.

The SLIC-P PEB 4266 "low-power" version even allows three battery voltages (typically the most negative one, e.g. -48 V, is used in active mode (On Hook) and power down mode).

DuSLIC contains two mechanism which can be used as indication for the battery switching:

1. A threshold for the voltage at Tip/Ring can be set for generating an interrupt
2. The change between constant current and resistive feeding will generate an interrupt

3.4.3.3 SLIC Power Consumption Calculation in Active Mode

A scheme of a typical calulation is shown in **Figure 3-1**.

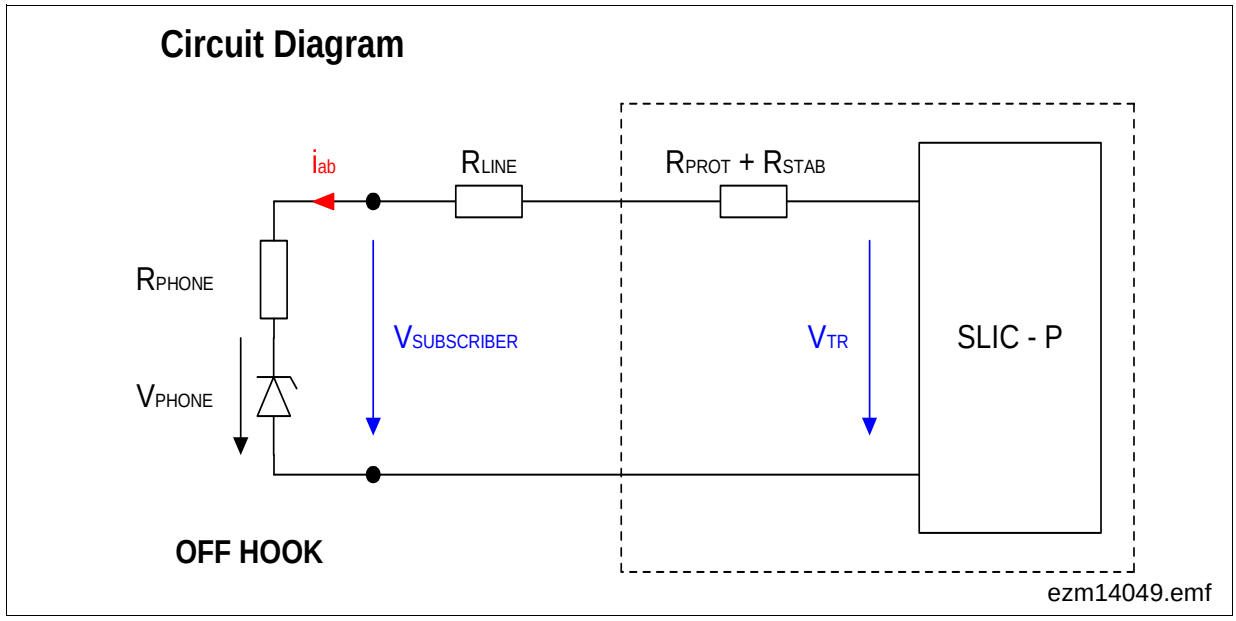


Figure 3-1 Circuit Diagram for Power Consumption

R_{Prot} = 40 Ω, R_{Stab} = 60 Ω, R_{Phone} = 150 Ω, V_{Phone} = 7 V, $i_{ab\ DC}$ = 20 mA, Conditions: $V_{Voice\ peak}$ = 2 V, $i_{Voice\ peak}$ = 2 mA, $V_{TTX,rms}$ (see example below)

Typical Power Consumption Calculation with SLIC-E

Assuming a typical application where the following battery voltages are used:

V_{DD} = 5 V, V_{BATL} = -43 V, V_{BATH} = -62 V, V_{HR} = 80 V and line feeding is guaranteed up to R_L = 1900 Ω. For longer lines (R_L > 1900 Ω) the extended battery feeding option can be used (Mode ACTR).
Requirement for TTX: V_{TTX} = 2.5 V_{rms} at a load of 200 Ω.

Table 3-6 shows line currents and output voltages for different operating modes.

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Table 3-6 Line Feed Conditions for Power Calculation for SLIC-E

Operating Mode	Line Currents	Output Voltages
PDRH, PDRHL	I_{TRANS} = 0 mA	-
ACTL	I_{TRANS} = 20 mA	$V_{TIP/RING}$ = 32 V
ACTH	I_{TRANS} = 20 mA	$V_{TIP/RING}$ = 50 V
ACTR extended battery feeding at higher loop length (R_L > 1900 Ω)	I_{TRANS} = 20 mA	$V_{TIP/RING}$ = 130 V

With the line feed conditions given in the above table the total power consumption PTOT and its shares at different operating modes are shown in **Table 3-7**. The output voltage at Tip and Ring is calculated for the longest line (R_L = 1900 Ω in ACTH, R_L = 996 Ω in ACTL).

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Table 3-7 SLIC-E PEB 4265 Typical Total Power Dissipation

	PQ[1)]	PI	PG	PO	PTOT
Operating Mode	[mW]	[mW]	[mW]	[mW]	[mW]
PDH	5.0	0	0	0	5.0
PDRH	6.0	0	0	0	6.0
ACTL	156	51.3	27.1	220	454
ACTH	239	72.2	32.8	240	584
ACTR	518	96.2	412	240	1266

1) The formulas for the calculation of the power shares PQ, PI, PG and PO can be found in the DuSLIC Data Sheet.

Figure 3-2 shows the total power dissipation PTOT of the SLIC-E in Active Mode (ACTH and ACTL) with switched Battery Voltage (V_{BATH}, V_{BATL}) as a function of R_{Line}. The power dissipation in the SLIC is strongly reduced for short lines.

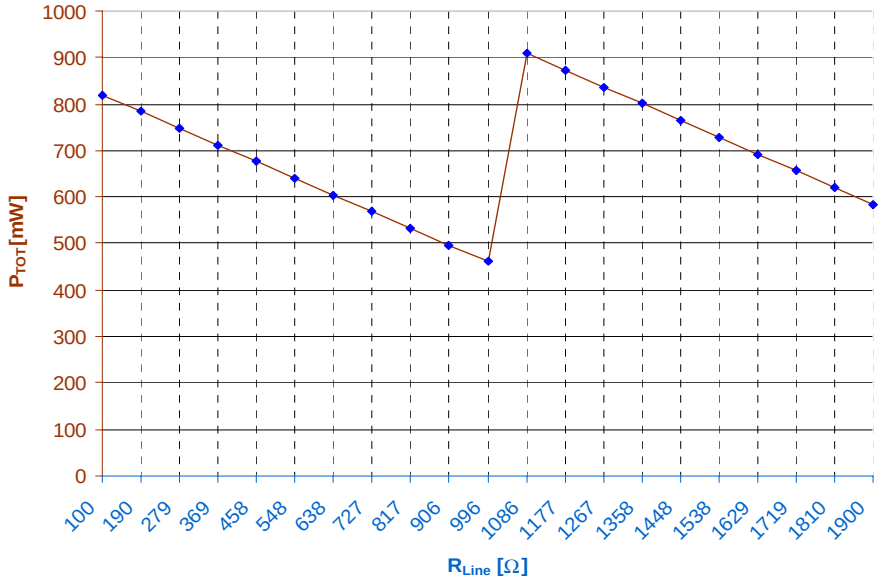

Figure 3-2 SLIC-E Power Dissipation with switched Battery Voltage

Typical Power Consumption Calculation with SLIC-P (Internal Ringing)

Assuming a typical application where the following battery voltages are used:

V_{DD} = 5 V, V_{BATL} = -36 V, V_{BATH} = -48 V, V_{BATR} = -108 V and line feeding is guaranteed up to R_L = 1200 Ω.

Requirement for TTX: V_{TTX} = 2.5 V_{rms} at a load of 200 Ω.

Table 3-8 shows line currents and output voltages for different operating modes.

Table 3-8 Line Feed Conditions for Power Calculation for SLIC-P

Operating Mode	Line Currents	Output Voltages
PDRH, PDRHL	I_{TRANS} = 0 mA	-
ACTL	I_{TRANS} = 20 mA	$V_{TIP/RING}$ = 25.2 V
ACTH	I_{TRANS} = 20 mA	$V_{TIP/RING}$ = 36.0 V
ACTR	I_{TRANS} = 20 mA	$V_{TIP/RING}$ = 96 V

With the line feed conditions given in the above table the total power consumption PTOT and its shares at different operating modes are shown in **Table 3-9**. The output voltage at Tip and Ring is calculated for the longest line (R_L = 1200 Ω in ACTH, R_L = 662 Ω in ACTL)

Table 3-9 SLIC-P PEB 4266 Power Dissipation

	PQ[1)]	PI	PG	PO	PTOT
Operating Mode	[mW]	[mW]	[mW]	[mW]	[mW]
PDH	9	0	0	0	9
PDRH	7	0	0	0	7
PDRR	10	0	0	0	10
ACTL	81.7	43.6	15.3	216	357
ACTH	135	56.8	0	240	432
ACTR (Boosted)	372	123	112	240	847
ROR, ROT (Ring Pause)	252	0	112	0	364

1) The formulas for the calculation of the power shares PQ, PI, PG and PO can be found in the DuSLIC Data Sheet

Figure 3-4 shows the total power dissipation PTOT of the SLIC-P in Active Mode (ACTH and ACTL) with switched Battery Voltage (V_{BATH}, V_{BATL}) as a function of R_{Line}.

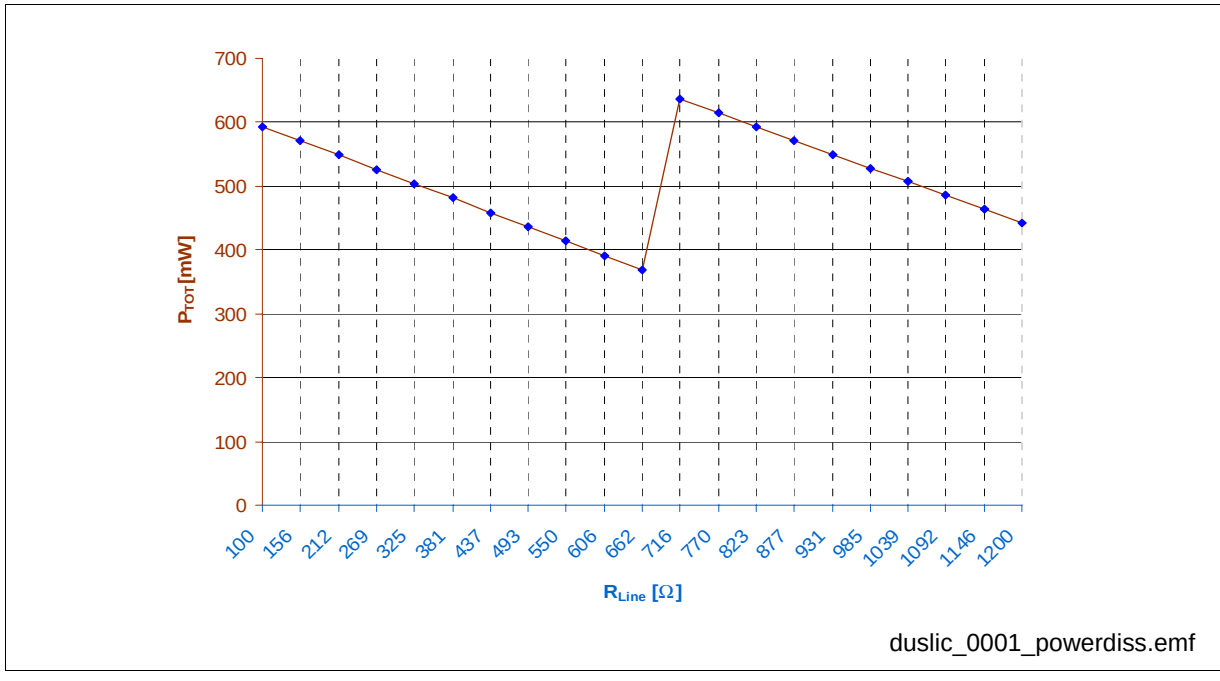

Figure 3-3 SLIC-P Power Dissipation (Switched Battery Voltage, Long loops)

Typical Power Consumption Calculation with SLIC-P (External Ringing)

Assuming a typical application where the following battery voltages are used:

V_{DD} = 5 V, V_{BATL} = -25 V, V_{BATH} = -31 V, V_{BATR} = -48 V and line feeding is guaranteed up to R_L = 600 Ω.

Requirement for TTX: $V_{TTX,rms}$ = 0.7 V.

This is a typical lowest power application, where V_{BATR} is used just in the On Hook state and V_{BATH} and V_{BATL} is used in the active modes with battery switching.

Table 3-10 shows line currents and output voltages for different operating modes.

Table 3-10 Line Feed Conditions for Power Calculation for SLIC-P

Operating Mode	Line Currents	Output Voltages
PDRH, PDRHL	I_{TRANS} = 0 mA	-
ACTL	I_{TRANS} = 20 mA	$V_{TIP/RING}$ = 19.2 V
ACTH	I_{TRANS} = 20 mA	$V_{TIP/RING}$ = 24 V
ACTR	I_{TRANS} = 20 mA	$V_{TIP/RING}$ = 41 V

With the line feed conditions given in the above table the total power consumption PTOT and its shares at different operating modes are shown in **Table 3-11**. The output voltage at Tip and Ring is calculated for the longest line (R_L = 600 Ω in ACTH, R_L = 358 Ω in ACTL)

Table 3-11 SLIC-P PEB 4266 Power Dissipation

	PQ[1)]	PI	PG	PO	PTOT
Operating Mode	[mW]	[mW]	[mW]	[mW]	[mW]
PDH	4.3	0	0	0	4.3
PDRH	3.9	0	0	0	3.9
PDRR	5.0	0	0	0	5.0
ACTL	57.7	31.5	1.0	116	206
ACTH	88.7	38.1	-28.6	140	238
ACTR	168	56.8	-87.2	140	277
ROR, ROT	153	0	-68.8	0	88.7

[1)] The formulas for the calculation of the power shares PQ, PI, PG and PO can be found in the DuSLIC Data Sheet

Figure 3-4 shows the total power dissipation PTOT of the SLIC-P in Active Mode (ACTH and ACTL) with switched Battery Voltage (V_{BATH}, V_{BATL}) as a function of R_{Line} (Lowest Power Applications).

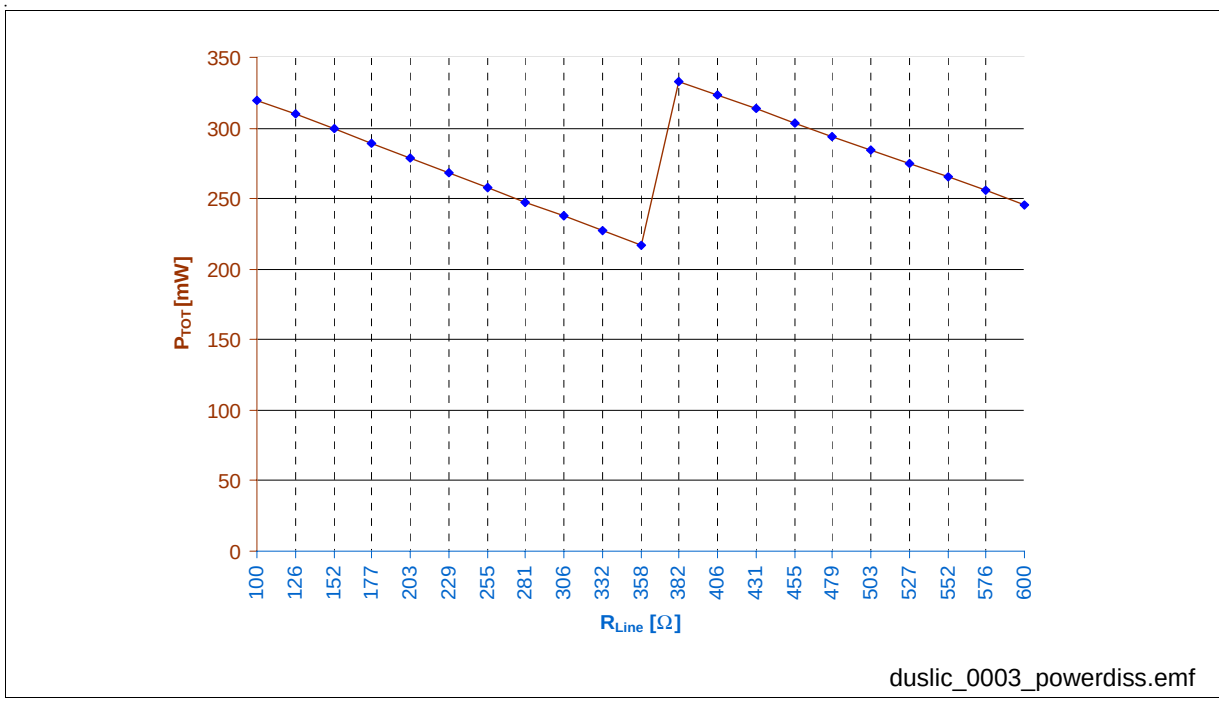

Figure 3-4 SLIC-P Power Dissipation (Switched Battery Voltage, Short Loops)

3.4.3.4 Ringing Modes

Internal Balanced Ringing (SLIC-E and SLIC-P)

The SLIC internal balanced ringing facility requires a higher supply voltage (auxiliary voltage V_{HR}). The highest share of the total power is dissipated in the output stage of the SLIC. The output stage power dissipation PO (see **Table 3-12**, **Table 3-13**) depends on the Ring amplitude ($V_{RNG,PEAK}$), the equivalent ringer load (R_{RNG} and C_{RNG}), the ring frequency (via cos ϕ_L) and the line length (R_L).

The minimum auxiliary voltage V_{HR} necessary for a required ring amplitude can be calculated using:

$$V_{HR} - V_{BATH} = V_{RNG,PEAK} + V_{RNG,DC} + V_{DROP} = V_{RNG,RMS} \times \text{crest factor} + V_{RNG,DC} + V_{DROP}$$

The crest factor is defined as peak value divided by RMS value (here always 1.41 because sinusoidal ringing is assumed).

$V_{RNG,DC}$ Superimposed DC voltage for Ring trip detection (10 to 20 V)

V_{DROP} Sum of voltage drops in SLIC buffers (**Table 3-5**)

$V_{RNG,PEAK}$ Peak ring voltage at Tip/Ring

The strong influence of the ringer load impedance Z_{LD} and the number of ringers is demonstrated by the formula for the current sensor power dissipation (PI + PO) in **Table 3-12** and **Table 3-13**.

The ringer load impedance Z_{LD} can be calculated as follows:

$Z_{LD} = |Z_{LD}| \, e^{j\phi LD} = R_L + R_{RNG} + 1 / j\omega C_{RNG}$ with

Z_{LD} Load impedance

R_{RNG} Ringer Resistance

C_{RNG} Ringer Capacitance

R_L Line Resistance

Internal Unbalanced Ringing with SLIC-P

The ring signal is present just on one line (modes ROR, ROT), while the other line is connected to a potential of GND.

The minimum battery voltage V_{BATR} necessary for a required ring amplitude can be calculated using:

$- V_{BATR} - V_{DROP} = 2 * V_{RNG,\,PEAK} = 2 * V_{RNG,RMS}$ x crest factor

External Ringing (SLIC-E and SLIC-P)

When an external ring generator and ring relays are used, the SLIC can be switched to Power Down mode.

The "low-power" SLIC-P is optimized for extremely power-sensitive applications (see **Table 3-11**). This SLIC has three different battery voltages. V_{BATR} can be used for on-hook, while V_{BATH} and V_{BATL} are normally used for the off-hook mode.

3.4.3.5 SLIC Power Consumption Calculation in Ringing Mode

The average power consumption for a ringing cadence of 1 sec. on and 4 seconds off is given by

$$PTOT_{average} = k * PTOT_{Ringing} + (1-k) * PTOT_{RingPause}$$

with k = 0.20

The typical circuit for ringing is shown in **Figure 3-5**.

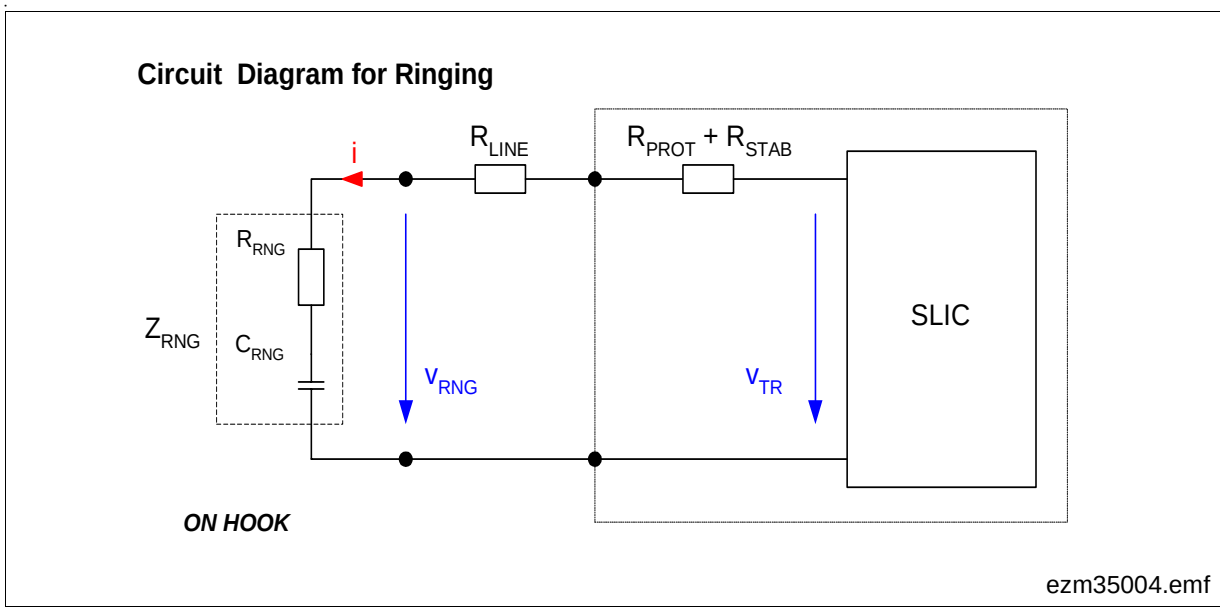

Figure 3-5 Circuit Diagram for Ringing

– Power Consumption Calculation for SLIC-E in Balanced Ringing Mode

With the example of the above calulation for SLIC-E (see **Chapter 3.4.3.3**) and a typical ringer load.

R_{RNG} = 450 Ω, C_{RNG} = 3.4 µF, required ringing voltage V_{RNG} = 58 V_{rms} and ringing frequency f_{RNG} = 20 Hz. DC Offset Voltage for ring trip detection V_{DC} = 20 V.

Table 3-12 shows the power calculation for the total power dissipation PTOT of the SLIC-E in balanced ringing mode consisting of the quiescent power dissipation PQ, the current sensor power dissipation PI, the gain stage power dissipation PG and the output stage power dissipation PO.

Table 3-12 SLIC-E Balanced Ringing Power Dissipation (typical)

$PTOT_{RingPause}$ = PQ + PI + PG +PO (I_{Trans}= 0 mA)	**710 mW**
$PTOT_{Ringing}$ = PQ + PI + PG +PO	**2481 mW[1)]**
$PQ = V_{DD}*I_{DD} + IV_{BATH}I*I_{BATH} + IV_{BATL}I*I_{BATL} + V_{HR}*I_{HR}$	390 mW
$PI = 0{,}015*I_{Trans,rms}*V_{HR} + 0{,}055*I_{Trans,rms}*\|V_{BATH}\| + 0{,}04*I_{Trans,rms}*V_{DD}$ with $I_{Trans,rms} = V_{TIP/RING,\ rms} / IZ_{LD}I$	118 mW
$PG = (V_{HR} + \|V_{BATH}\|)*(SQRT((V_{HR} + V_{BATH} + V_{DC\text{-}offset})^2 + (V_{TIP/RING}^2)/2) - IV_{HR} + V_{BATH}I)/60k + (V_{HR}^2 - 32^2 + V_{BATH}^2 - 48^2)*(1/60k + 1/216k)$	320 mW
$PO = (V_{HR} + IV_{BATH}I)*I_{Trans,rms}*2*SQRT(2)/\pi - V_{TIP/RING,\ rms}*I_{Trans,rms}*\cos(\phi_{Load})$	1653 mW

[1)] **Values for V_{DD} = 5 V, V_{BATL} = -43 V, V_{BATH} = -62 V, V_{HR} = 80 V, T_J = 25 °C**

– Power Consumption Calculation for SLIC-P in Balanced Ringing Mode

With the example of the above calulation with R_L = 1200 Ω line length for SLIC-P (see **Chapter 3.4.3.3**) when the internal ringing feature will be used.

Typical Ringer load: R_{RNG} = 1000 Ω, C_{RNG} = 3.7 µF. Required ringing voltage V_{RNG} = 45 Vrms and ringing frequency f_{RNG} = 20 Hz. DC Offset Voltage for ring trip detection V_{DC} = 20 V.

Table 3-13 shows the power calculation for the total power dissipation PTOT of the SLIC-P in balanced ringing mode consisting of the quiescent power dissipation PQ, the current sensor power dissipation PI, the gain stage power dissipation PG and the output stage power dissipation PO.

Table 3-13 SLIC-P Balanced Ringing Power Dissipation (typical)

$PTOT_{RingPause}$ = PQ + PI + PG +PO (I_{Trans}= 0 mA)	**482 mW**
$PTOT_{Ringing}$ = PQ + PI + PG +PO	**1618 mW[1)]**
PQ = V_{DD}*I_{DD} + IV_{BATR}I*I_{BATR} + IV_{BATH}I*I_{BATH} + IV_{BATL}I*I_{BATL}	370 mW
PI = 0,055*$I_{Trans,rms}$*IV_{BATR}I + 0,04*$I_{Trans,rms}$*V_{DD} with $I_{Trans,rms}$ = $V_{TIP/RING,\ rms}$ / IZ_{LD}I	117 mW
PG = (V_{BATR}^2 - 80^2)*(1/60k + 1/216k)	112 mW
PO = IV_{BATR}I*$I_{Trans,rms}$*2*SQRT(2)/π - $V_{TIP/RING,\ rms}$*$I_{Trans,rms}$*cos(ϕ_{Load})	1019 mW

1) Values for V_{DD} = 5 V, V_{BATL} = -36 V, V_{BATH} = -48 V, V_{BATR} = -108 V, T_J = 25 °C

– Power Consumption Calculation for SLIC-P in Unbalanced Ringing Mode

A similar power calculation is valid for internal unbalanced ringing mode, which is only available for the SLIC-P.

With the following example:

V_{DD} = 5 V, V_{BATL} = -30 V, V_{BATH} = -36 V, V_{BATR} = -150 V and line feeding is guaranteed up to 600 Ω.

Typical Ringer load R_{RNG} = 1000 Ω, C_{RNG} = 3.7 µF, required ringing voltage V_{RNG} = 45 V_{rms} and ringing frequency f_{RNG} = 20 Hz.

Table 3-14 shows the power calculation for the total power dissipation PTOT of the SLIC-P in unbalanced ringing mode.

Table 3-14 SLIC-P Unbalanced Ringing Power Dissipation (typical)

$PTOT_{RingPause}$ = PQ + PI + PG +PO (I_{Trans}= 0 mA)	**644 mW**
$PTOT_{Ringing}$ = PQ + PI + PG +PO	**2756 mW[1)]**
PQ = V_{DD}*I_{DD} + IV_{BATR}I*I_{BATR}+ IV_{BATH}I*I_{BATH} + IV_{BATL}I*I_{BATL}	349 mW
PI = 0,055*$I_{Trans,rms}$*IV_{BATR}I + 0,04*$I_{Trans,rms}$*V_{DD} with $I_{Trans,rms}$ = $V_{TIP/RING,\ rms}$ / IZ_{LD}I	160 mW
PG = (0,5*$V_{TIP/RING}^2$ - (V_{BATR}/2)^2)/60k + (V_{BATR}^2 - 80^2)*(1/60k + 1/216k)	295 mW
PO = IV_{BATR}I*$I_{Trans,rms}$*2*SQRT(2)/π - $V_{TIP/RING,\ rms}$*$I_{Trans,rms}$*cos(ϕ_{Load})	1952 mW

[1)] **Values for V_{DD} = 5 V, V_{BATL} = -30 V, V_{BATH} = -36 V, V_{BATR} = -150 V, T_J = 25 °C**

3.5 Test Modes

3.5.1 Introduction

Subscriber loops are subject to many types of failure and therefore have to be monitored. This requires easy access to the subscriber loop to perform regular measurements. The tests involve resistance, leakage and capacitance measurements and measurements of interfering currents and voltages.

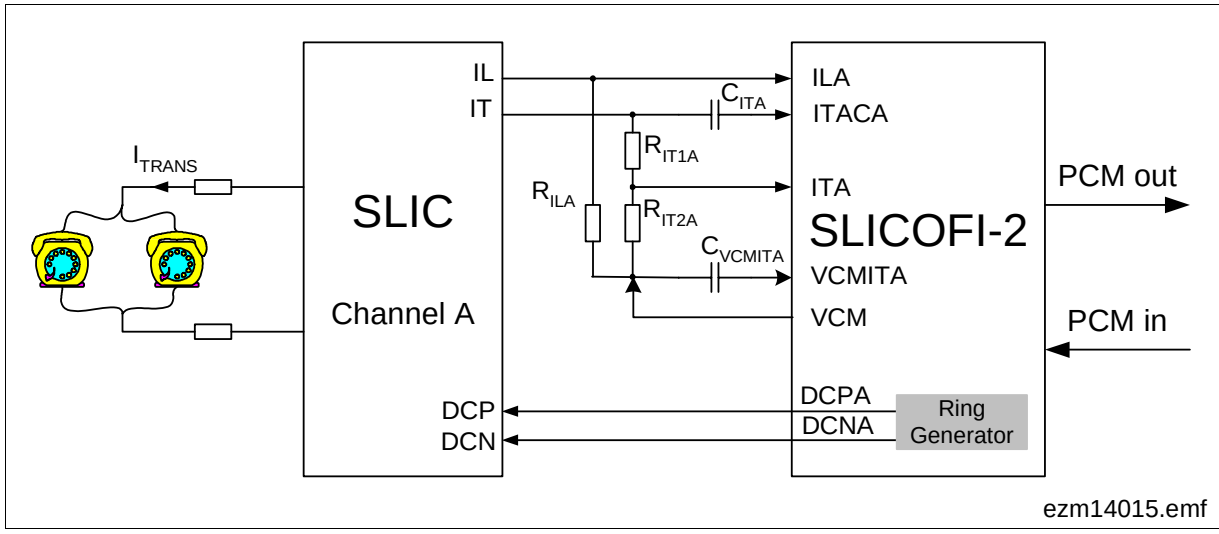

Figure 3-6 Capacitance Measurement

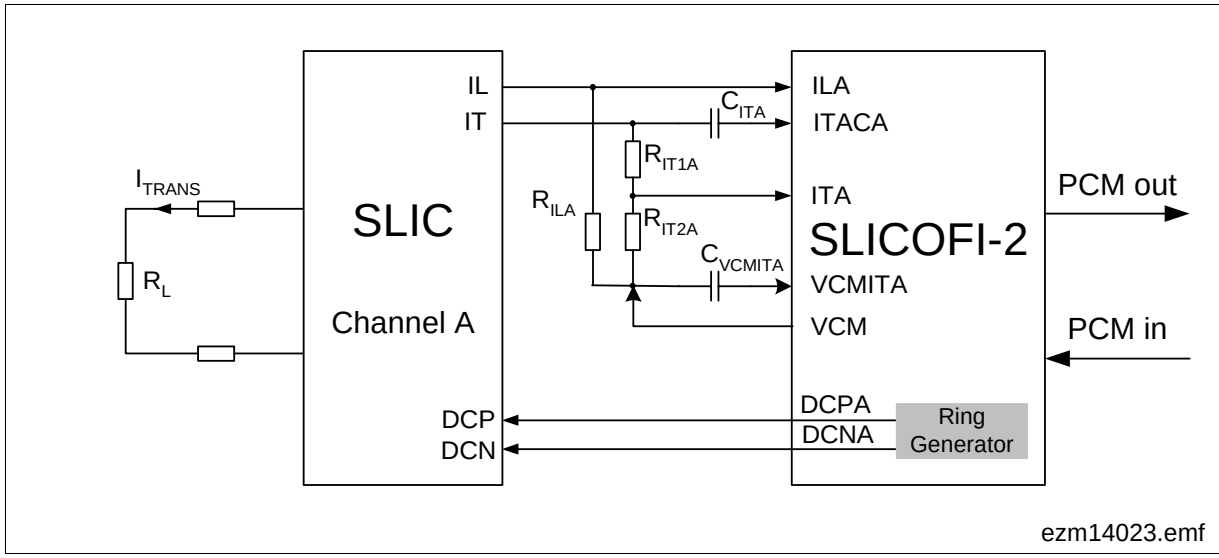

Figure 3-7 Resistance Measurement

3.5.2 Conventional Line Testing

Conventional analog line cards in Central Office applications usually include 3 to 4 relays per channel. One relay is normally required to switch an external ring generator to the line and some applications need an additional relay for polarity reversal. Two test relays are used to monitor the local loop (test-out relay) and to verify the line circuit itself (test-in relay).

The test-out relay switches an external test unit to the subscriber line. The external test unit performs capacitance, resistance and leakage measurements to detect any changes in the line condition or to detect line failures.

The test-in relay switches a test impedance to the SLIC and separates the subscriber line from the SLIC. With a test tone, it is possible to check the entire loop plus the CODEC including the SLIC.

With an external test unit, every line has to be connected separately to the test unit and the tests have to be performed one line at a time. Testing thousands of lines takes several hours. Because of the time factor, these tests are typically carried out once a week or once a month. The test cycle for a specific subscriber line is therefore very long and any failures are usually detected at a very late stage. This reduces the network quality.

3.5.3 DuSLIC Line Testing

With its Integrated Test and Diagnosis Functions (ITDF), DuSLIC can perform tests without an external test unit.

ITDF reduces testing time and manufacturing costs, accelerates the test flow in the field, and provides more flexibility. ITDF opens the way to a new dimension of test service for system manufacturers and their customers. All features are provided on silicon, eliminating the need for additional expensive test equipment. The external relay and the resistor is used to calibrate DuSLICs integrated Test and Diagnosis functions.

Whereas testing used to be carried out once a week or once a month, DuSLIC’s integrated test functions make it possible to test the subscriber lines every night.
The integrated test and diagnosis functions test the line and CODEC as described in the sections "Subscriber Line Testing" and "Board Testing ".

Subscriber Line Testing

The DuSLIC chipset offers a new approach for linetesting. Test capabilities are provided on a per line basis, allowing almost continuously to monitor the line. Therefore line problems can be detected before the customer gets notice of it and appropriate actions can be taken. Also no special hardware or test equipment is required to perform linetest functions. This results in cost savings for the linecard itself as well as improved system reliability as problems can be detected in a very early stage.

List of Line Test Functions:

- Loop resistance
- Leakage current Tip/Ring
- Leakage current Tip/GND
- Leakage current Ring/GND
- Ringer capacitance test
- Line capacitance
- Line capacitance Tip/Gnd
- Line capacitance Ring/GND
- Foreign voltage measurement Tip/GND
- Foreign voltage measurement Ring/GND
- Foreign voltage measurement Tip/Ring
- Measurement of ringing voltage
- Measurement of line feed current
- Measurement of transversal and longitudinal current

To perform the different linetest functions the DuSLIC includes several levelmeter blocks:

- DC levelmeter
- AC levelmeter
- TTX levelmeter

To do measurements means to stimulate the line, and to measure the response of the line. Following signal sources within the DuSLIC might be used as signal source:

- Constant DC voltage (ringing DC offset voltage)
- 2 Tone generators (voice frequency signals)
- TTX metering signal generator (12/16 kHz)
- Ramp generator (used for measuring capacitances)
- Ringing Generator (5Hz - 300Hz)

DC Level Meter:

- The DC levelmeter allows to measure:
- I_{Trans}: transversal current on the line $I_{Trans} = (I_T + I_R)/2$
- I_{Long}: longitudinal current on the line $I_{Long} = (I_T - I_R)/2$
- Voltage level at IO3 and IO4 (can be configured as analog inputs)
- Difference voltage level between IO4-IO3
- VDD voltage (internally connected to VDD/3)
- DC control voltage for DC loop

The input signal gets digitized and decimated to a +/- 17Bit value. The effective sampling rate would be 2kHz. Offset coming from the SLIC, the filter stage and the AD converter my be eliminated by adding the value of an offset register.

The AC levelmeter allows access to the voice signal path while active voice signals being transferred. After AD conversion and decimation the signal may be applied with a

programmable filter characteristic (bandpass, notch filter). Like the DC levelmeter signal the AC signal also may be rectified and integrated. The integration period is set either to 16ms or 256ms. Reading of the AC levelmeter result again is done via the result registers.

TTX Levelmeter:

The cancellation of the TTX signal in the transmit direction is done by an adaptive TTX filter. This adaptive filter offers two control signal which correlate with the real and imaginary part of the load connected to Tip/Ring wire of the SLIC. Therefore it can be used to measure the line impedance.

Board Testing

To perform a functional inspection of a complete analog line card at the end of the manufacturing process a variety of integrated analog and digital loops can be used. These Loops, together with an external relay and a reference resistor, allow the manufacturer a quick and easy inspection of the digital and analog interfaces. The integrated level metering function enables performance tests of different parameters without additional test and measurement equipment.

3.5.4 Test Loops

The main AC signal path of SLICOFI-2 and the integrated analog and digital loops are shown in **Figure 3-8**.

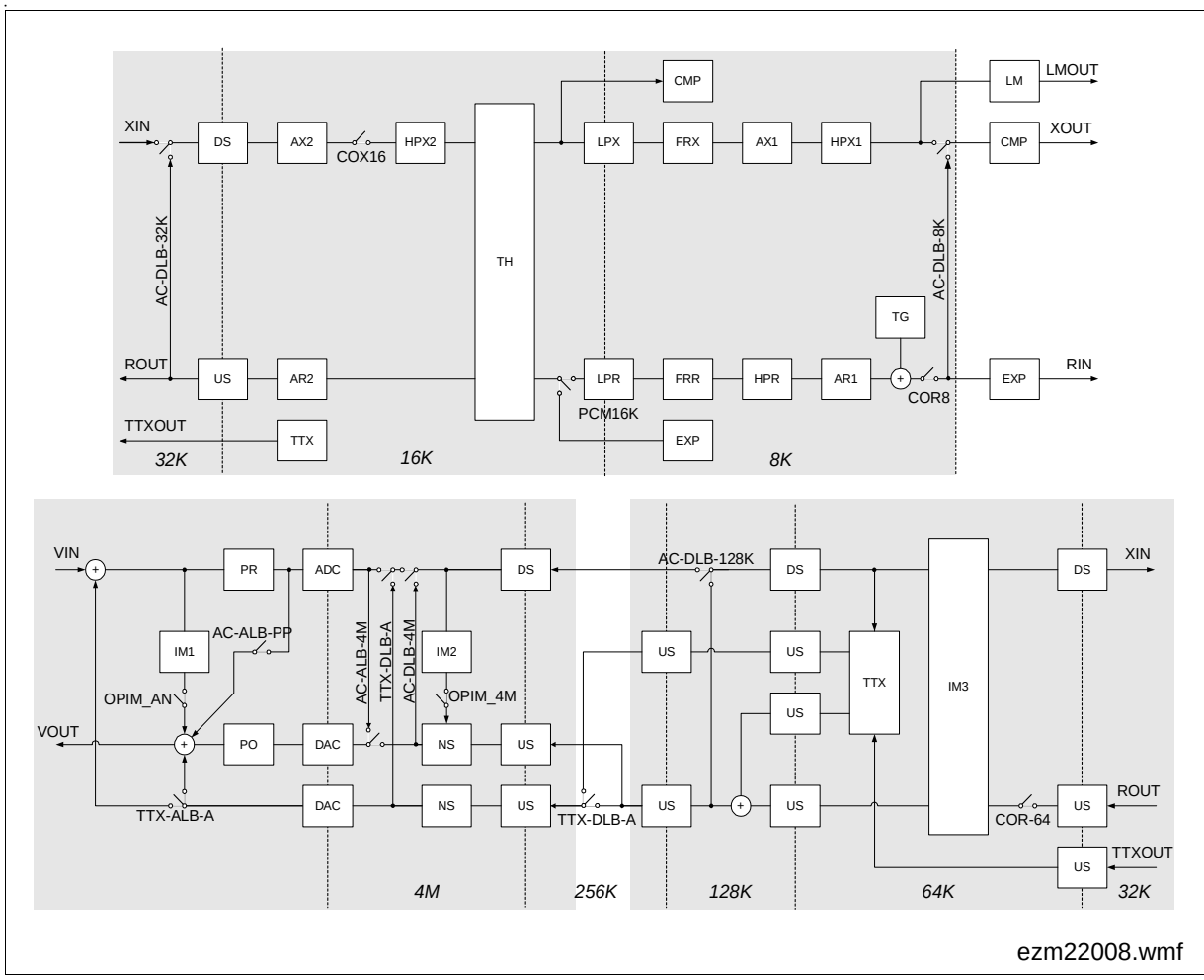

Figure 3-8 SLICOFI-2 Testloops

4 Interfaces

The DuSLIC connects the analog subscriber to the digital switching network by two different types of digital interfaces to allow highest flexibility in different applications:

- PCM interface combined with a serial microcontroller (µC) interface
- IOM-2 interface.

The PCM/$\overline{\text{IOM-2}}$ pin selects the interface mode.

PCM/$\overline{\text{IOM-2}}$ = 0: The IOM-2 interface is selected.
PCM/$\overline{\text{IOM-2}}$ = 1: The PCM/µC interface is selected.

The analog TIP/RING interface connects the DuSLIC to the subscriber.

4.1 PCM Interface with a Serial Microcontroller Interface

In PCM/µC interface mode voice and control data are seperated and handled by different pins of the SLICOFI-2. Voice data are transferred via the PCM highways while control data are using the microcontroller interface.

4.1.1 PCM Interface

The serial PCM interface is used to transfer A-law-or µ-law-compressed voice data. In test mode, the PCM interface can also transfer linear data. The eight pins of the PCM interface are used as follows (two PCM highways):

PCLK:	PCM Clock, 128 kHz to 8192 kHz
FSC:	Frame Synchronization Clock, 8 kHz
DRA:	Receive Data Input for PCM Highway A
DRB:	Receive Data Input for PCM Highway B
DXA:	Transmit Data Output for PCM Highway A
DXB:	Transmit Data Output for PCM Highway B
$\overline{\text{TCA}}$:	Transmit Control Output for PCM Highway A, Active low during transmission
$\overline{\text{TCB}}$:	Transmit Control Output for PCM Highway B, Active low during transmission

The FSC pulse identifies the beginning of a receive and transmit frame for both channels. The PCLK clock signal synchronizes the data transfer on the DXA (DXB) and DRA (DRB) lines. On all channels, bytes are serialized with MSB first. As a default setting, the rising edge indicates the start of the bit, while the falling edge is used to buffer the contents of the received data on DRA (DRB). If double clock rate is selected (PCLK

clock rate is twice the data rate), the first rising edge indicates the start of a bit, while, by default, the second falling edge is used to buffer the contents of the data line DRA (DRB).

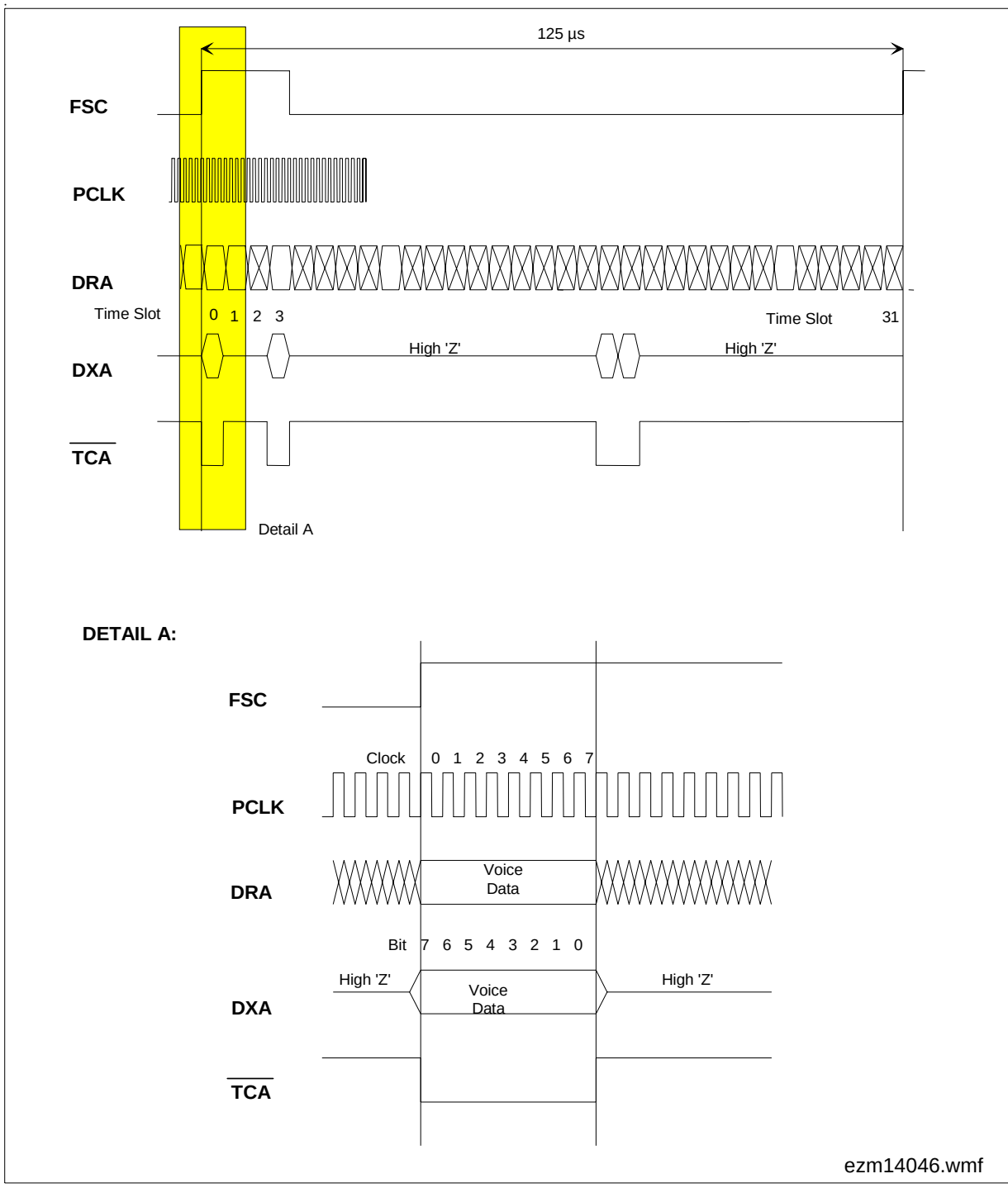

Figure 4-1 General PCM Interface Timing

The data rate of the interface can vary from 2*128 kb/s to 2*8192 kb/s (two highways). A frame may consist of up to 128 time slots of 8 bits each. The time slot and PCM

highway assignment for each DuSLIC channel can be programmed. Receive and transmit time slots can also be programmed individually. When DuSLIC is transmitting data on DXA (DXB), pin $\overline{\text{TCA}}$ ($\overline{\text{TCB}}$) is activated to control an external driving device.

The DRA/B and DXA/B pins may be connected to form a bidirectional data pin for special purposes. For example, for the Serial Interface Port (SIP) with the Subscriber Line Data (SLD) bus. The SLD approach provides a common interface for analog or digital per-line components. For more details, please see the User's Manual "ICs for Communications"[1)] available from Infineon Technologies on request.

Table 4-1 shows PCM interface examples; other frequencies (e.g. 1536 kHz) are also possible.

Table 4-1 SLICOFI-2 PCM Interface Configuration

Clock Rate PCLK [kHz]	**Single/Double Clock** [1/2]	**Time Slots** [per highway]	**Data Rate** [kbit/s per highway]
64	1	1	64
128	2	1	64
128	1	2	128
256	2	2	128
256	1	4	256
512	2	4	256
512	1	8	512
768	2	6	384
768	1	12	768
1024	2	8	512
1024	1	16	1024
2048	2	16	1024
2048	1	32	2048
4096	2	32	2048
4096	1	64	4096
8192	2	64	4096
8192	1	128	8192
f	1	f/64	f
f	2	f/128	f/2

1) Ordering No. B115-H6377-X-X-7600, published by Infineon Technologies.

4.1.2 Serial Microcontroller Interface

The microcontroller interface consists of four lines: $\overline{CS}$, DCLK, DIN and DOUT.

$\overline{CS}$: A synchronization signal starting a read or write access to SLICOFI-2.

DCLK: A clock signal (up to 8.192 MHz) supplied to SLICOFI-2.

DIN: Data input carries data from the master device to the SLICOFI-2.

DOUT: Data output carries data from SLICOFI-2 to a master device.

There are two different command types. Reset commands have just one byte. Read / write commands have two command bytes with the address offset information located in the second byte.

A write command consists of two command bytes and the following data bytes. The first command byte sets whether the command is read or write one, how the command field is to be used and the DuSLIC channel (A or B) is written. The second command byte contains the address offset.

A read command consists of the two above-mentioned command bytes written to DIN. After the second command byte is applied to DIN a dump-byte consisting of ’1’s is written to DOUT. Data transfer starts with the first byte following the ’dump-byte’.

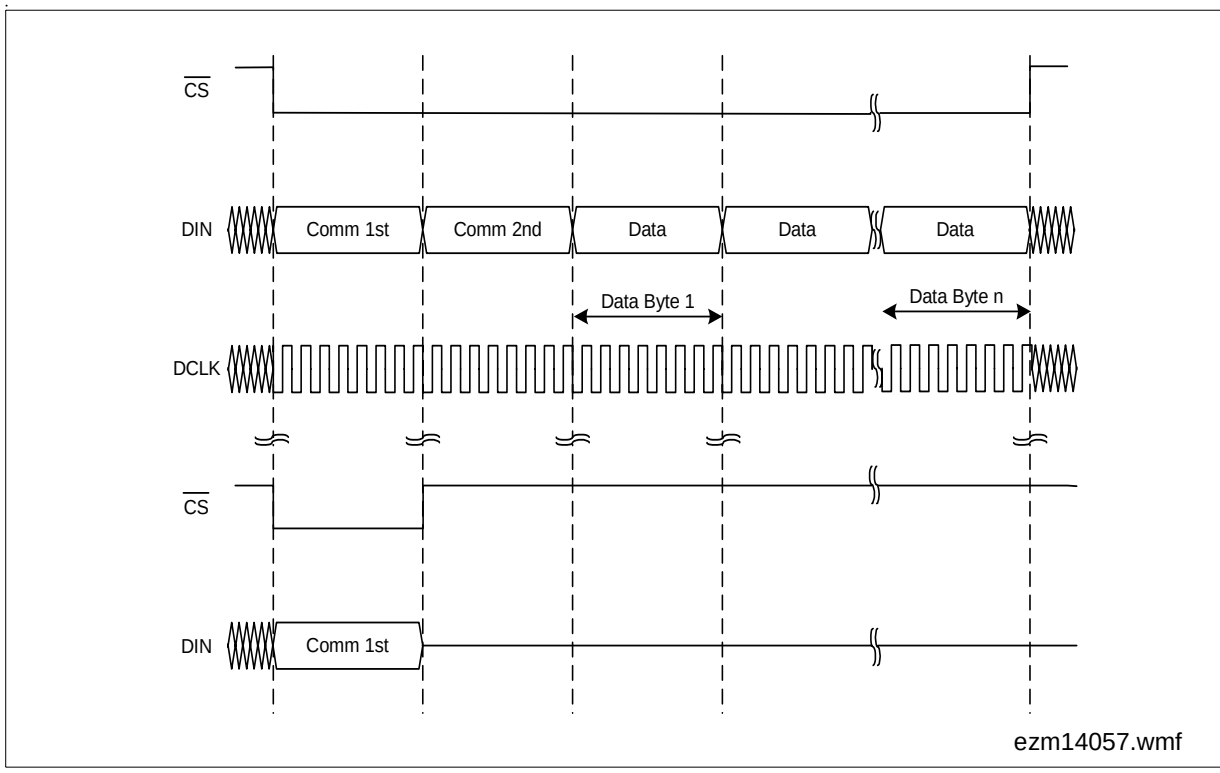

Figure 4-2 Serial µC Int. - Write Acc. (n Data Bytes and Single Byte Com.)

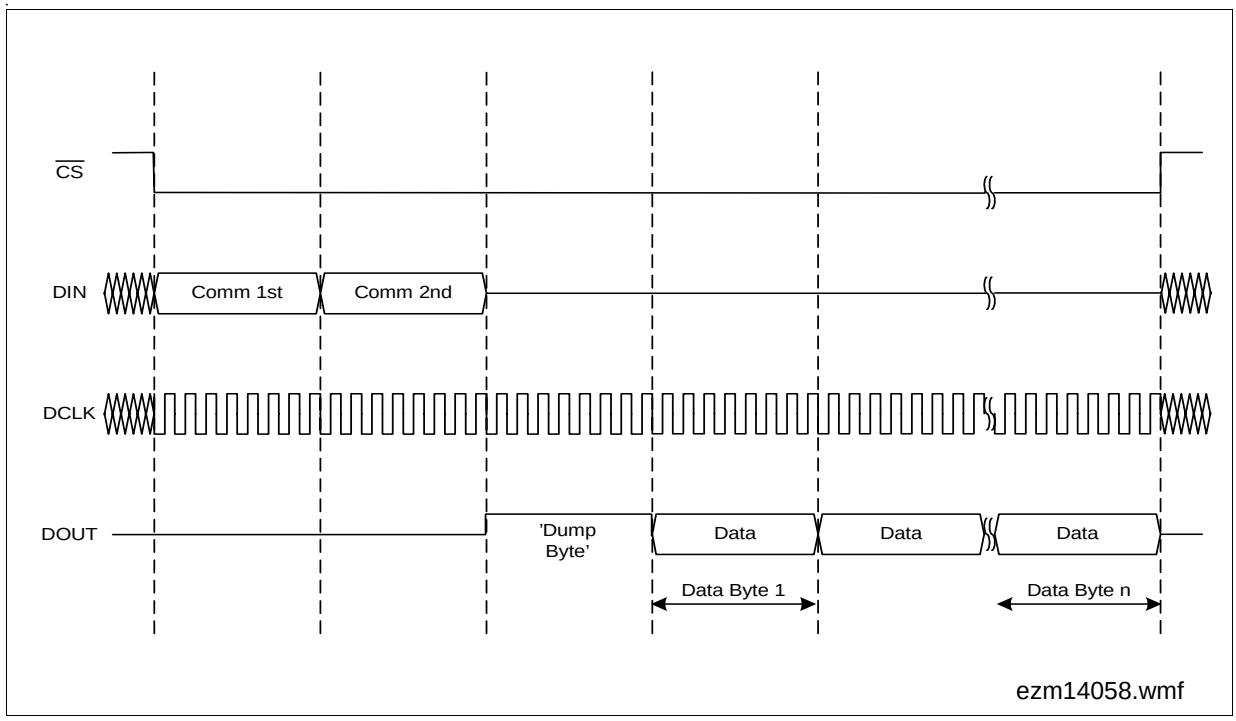

Figure 4-3 Serial µC Interface - Read Acc. (n Data Bytes Transfered)

4.2 The IOM-2 Interface

IOM-2 defines an industry standard serial bus for interconnecting telecommunication ICs for a broad range of applications - typically ISDN-based applications. The IOM-2 bus provides a symmetrical full-duplex communication link, containing data, control/ programming and status channels. Providing data, control and status information via a serial channel reduces pin count and cost by simplifying the line card layout. The IOM-2 Interface consists of two data lines and two clock lines as follows:

DU: Data upstream carries data from SLICOFI-2 to a master device.

DD: Data downstream carries data from the master device to the SLICOFI-2.

FSC: A frame synchronization signal (8 kHz) supplied to SLICOFI-2.

DCL: A data clock signal (2048 kHz or 4096 kHz) supplied to SLICOFI-2.

SLICOFI-2 handles data as described in the IOM-2 specification[1)] for analog devices.

1) Available on request from Infineon Technologies.

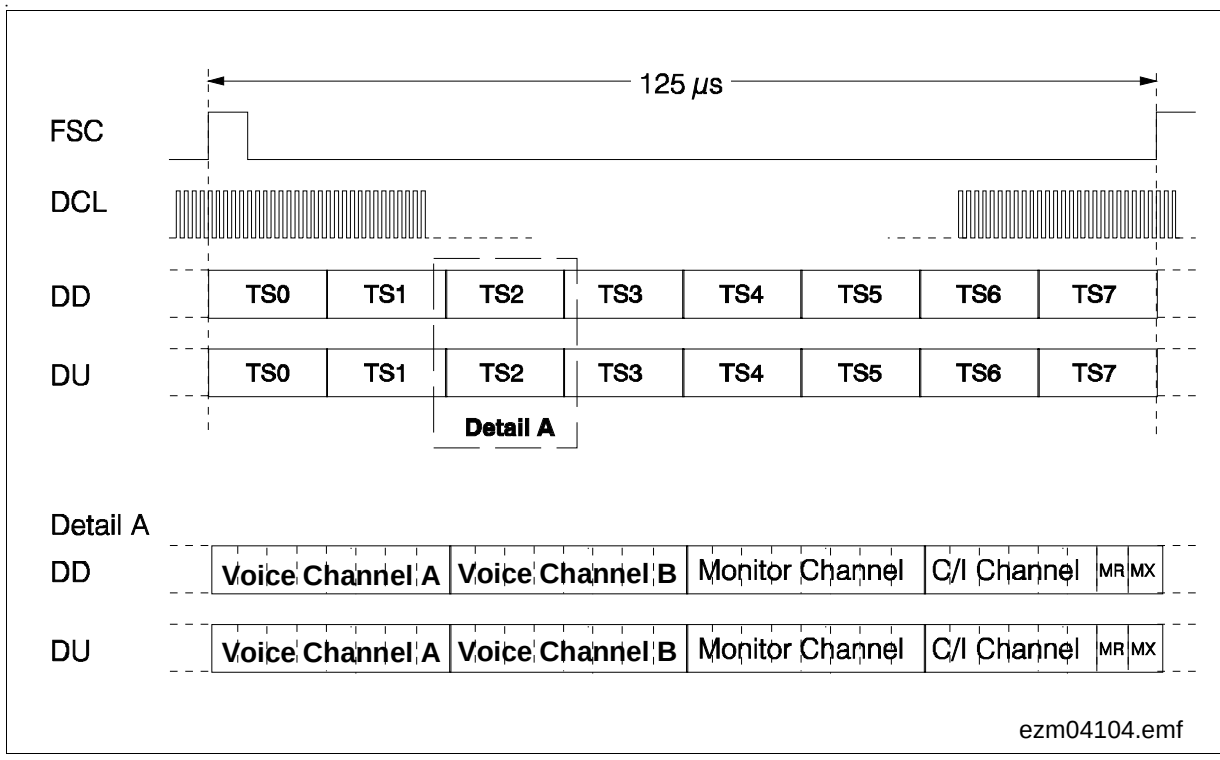

Figure 4-4 IOM-2 Int. Timing for up to 16 Voice Channels (Per 8 kHz Frame)

The information is multiplexed into frames, which are transmitted at an 8-kHz rate. The frames are subdivided into 8 sub-frames, with one sub-frame dedicated to each transceiver or pair of CODECs (in this case, two SLICOFI-2 channels). The sub-frames provide channels for data, programming and status information for a single transceiver or CODEC pair.

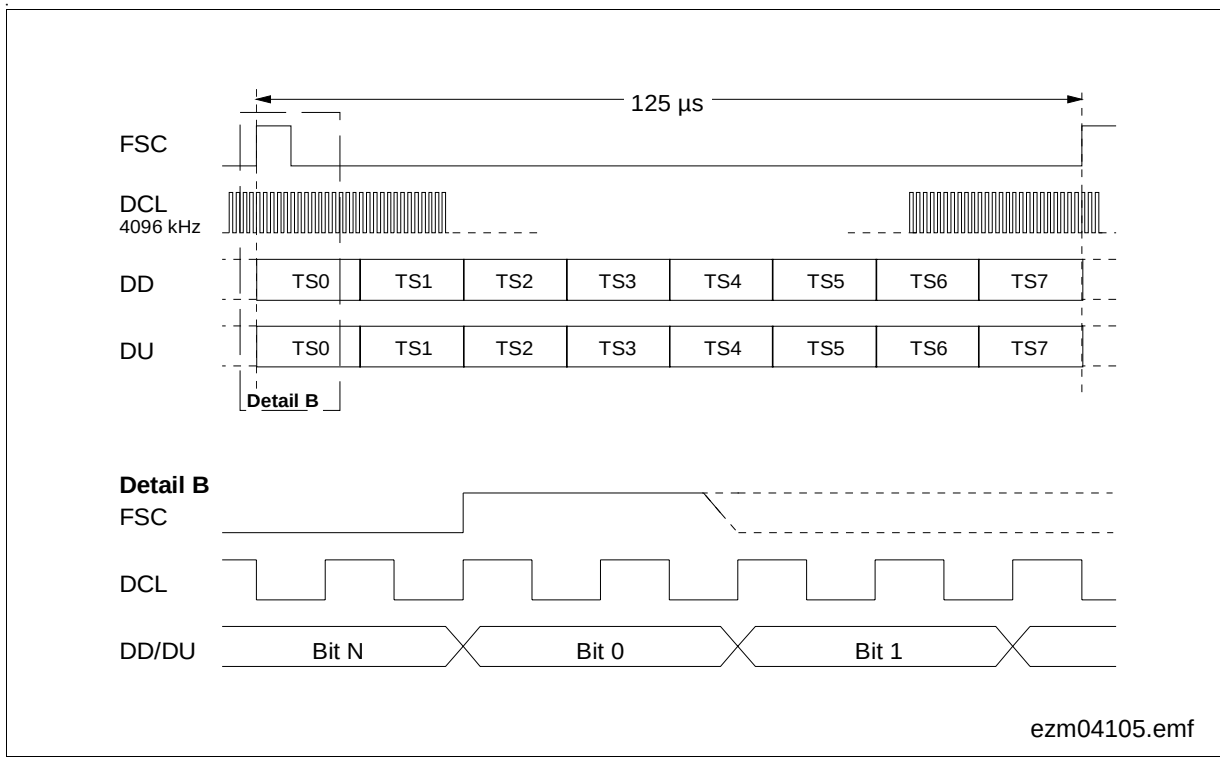

Figure 4-5 IOM-2 Interface Timing (DCL=4096 kHz, Per 8 kHz Frame)

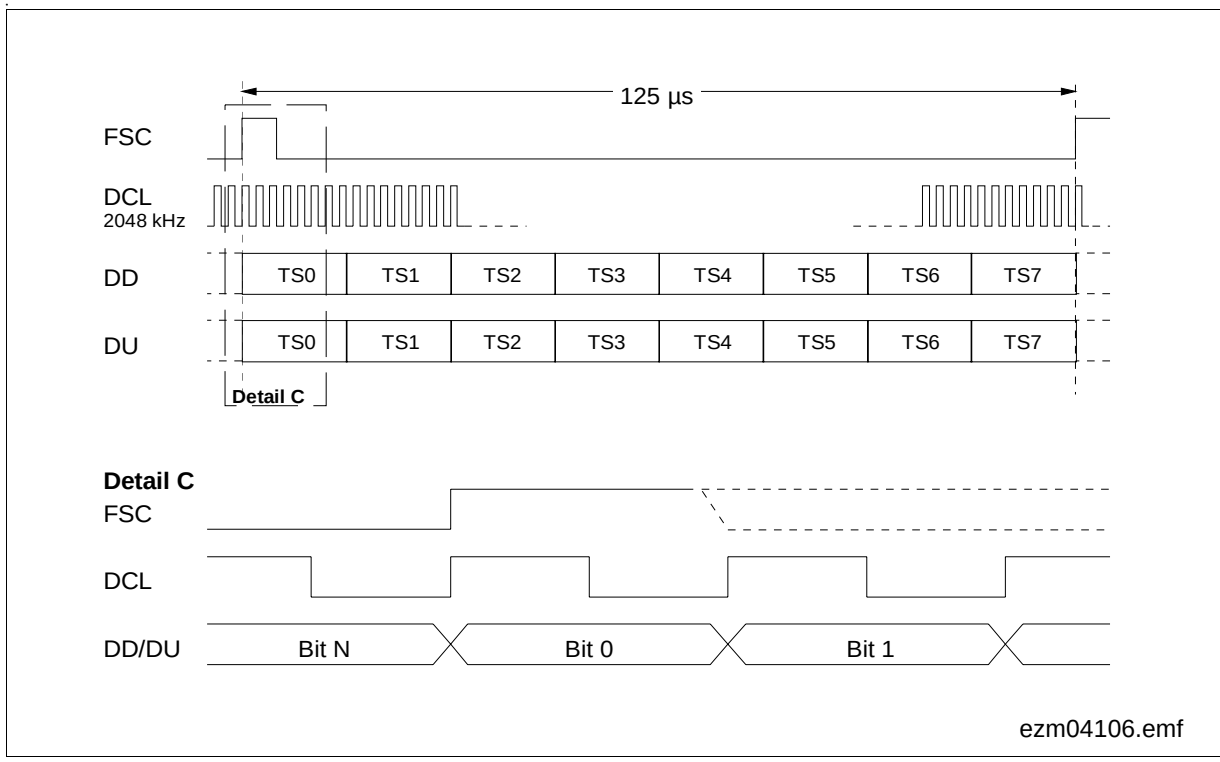

Figure 4-6 IOM-2 Interface Timing (DCL = 2048 kHz, Per 8 kHz Frame)

Both DuSLIC channels (see **Figure 4-4**) can be assigned to one of the eight time slots. Set the IOM-2 time slot selection as shown in **Table 4-2** below by pin-strapping. In this way, up to 16 channels can be handled with one IOM-2 interface on the line card.

Table 4-2 IOM-2 Time Slot Assignment

TS2	TS1	TS0	IOM-2 Operating Mode
0	0	0	Time slot 0; DCL = 2048, 4096 kHz
0	0	1	Time slot 1; DCL = 2048, 4096 kHz
0	1	0	Time slot 2; DCL = 2048, 4096 kHz
0	1	1	Time slot 3; DCL = 2048, 4096 kHz
1	0	0	Time slot 4; DCL = 2048, 4096 kHz
1	0	1	Time slot 5; DCL = 2048, 4096 kHz
1	1	0	Time slot 6; DCL = 2048, 4096 kHz
1	1	1	Time slot 7; DCL = 2048, 4096 kHz

2 MHz or 4 MHz DCL is selected by the SEL24 pin:

SEL24 = 0: DCL = 2048 kHz

SEL24 = 1: DCL = 4096 kHz

4.3 TIP/RING Interface

The TIP/RING interface is the interface that connects the subscriber to the DuSLIC. It meets the ITU-T recommendation Q.552 for a Z-interface and applicable LSSGR.

4.4 SLICOFI-2 and SLIC-E Interface

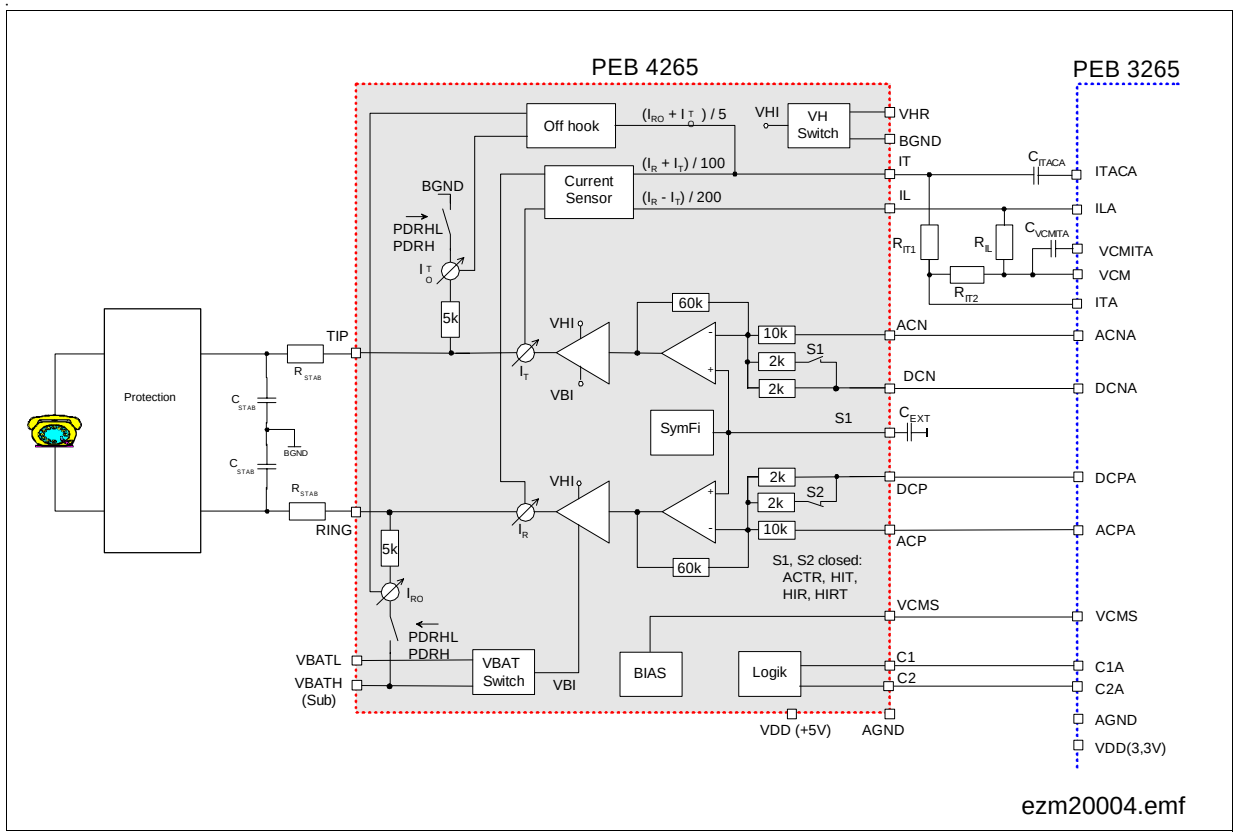

Figure 4-7 Minimal Application Circuit SLICOFI-2 and SLIC-E

The PEB 4265 operates in the following modes controlled by a ternary logic signal at the C1 and C2 input:

Table 1 SLIC-E Interface code

		C2		
		L	**M**	**H**
C1	**L**	PDH[1)]	PDRHL[1)]	PDRH [1)]
	M	ACTL	ACTH	ACTR
	H	HIRT	HIT	HIR

1) no "Overtemp" signaling possible via pin C1

4.5 SLICOFI-2 and SLIC-P Interface

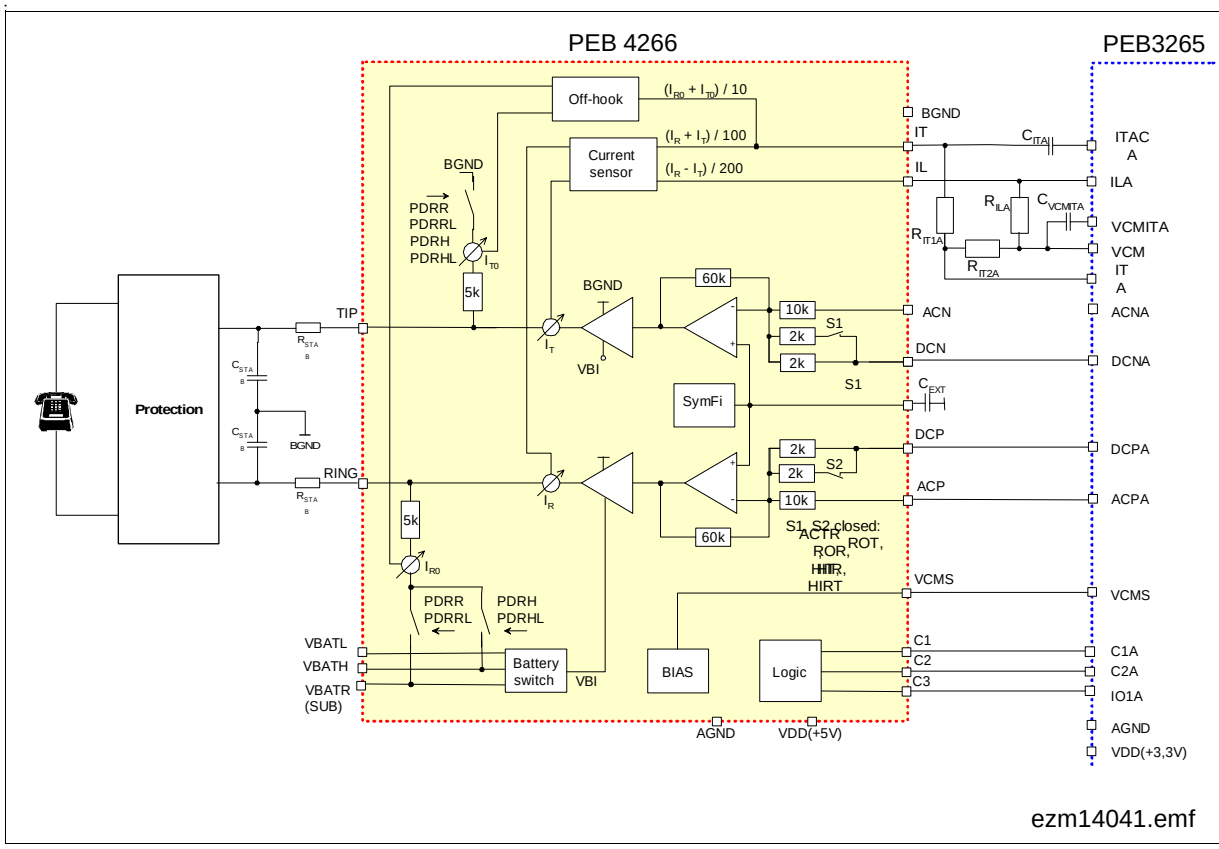

Figure 4-8 Minimal Application Circuit SLICOFI-2 and SLIC-P

The PEB 4266 operates in the following modes controlled by a ternary logic signal at the C1, C2 inputs and a binary logic signal at C3 input:

Table 4-3 SLIC-P Interface code

		C2		
		L	**M**	**H**
C1	**L**[1)]	PDH	PDRR	PDRRL
			PDRHL	PDRH
	M	ACTL	ACTH	ACTR
	H	HIRT	HIT	HIR
			ROT	ROR

C3 = L[2)]

C3 = H[3)]

1) No "Overtemp" signaling possible via pin C1

2) SLIC-P for extremely power sensitive applications without internal ringing

3) SLIC-P with two battery voltages (V_{BATH}, V_{BATL}) for voice and an additional voltage (V_{BATR}) for ringing

5 Electrical Characteristics

5.1 Electrical Characteristics PEB 4265 (SLIC-E)

5.1.1 Absolute Maximum Ratings PEB 4265

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Battery voltage L	V_{BATL} V_{BATL} - V_{BATH}	-85 -0.4	0.4		referred to V_{BGND}
Battery voltage H	V_{BATH}	-90	0.4	V	referred to V_{BGND}
Auxiliary supply voltage	V_{HR}	-0.4	90	V	referred to V_{BGND}
Total battery supply voltage, continuously	V_{HR}-V_{BATH}		160	V	
VDD supply voltage	V_{DD}	-0.4	7	V	referred to V_{AGND}
Ground voltage difference	V_{BGND}- V_{AGND}	 -0.4	 0.4	V	
Input voltages	V_{DCP},V_{DCN}, V_{ACP},V_{ACP}, V_{C1}, V_{C2}	-0.4	V_{DD}+0.4	V	referred to V_{AGND}
Voltages on current outputs	V_{IT}, V_{IL}	-0.4	V_{DD}+0.4	V	referred to V_{AGND}
RING, TIP voltages, continuously	V_R, V_T	V_{BATL}-0.4 V_{BATH}-0.4 V_{BATH}-0.4	0.4 0.4 V_{HR}+0.4	V V V	ACTL ACTH ACTR
RING,TIP voltages, pulse < 10 ms	V_R, V_T	t.b.d	t.b.d	V	ACTL, ACTH, ACTR
RING,TIP voltages, pulse < 1 ms	V_R, V_T	V_{BATH}-10	V_{HR}+10	V	ACTL, ACTH, ACTR
RING, TIP voltages, pulse < 1 µs	V_R, V_T	V_{BATH}-10	V_{HR}+30	V	ACTL, ACTH, ACTR
ESD-voltage, all pins			2	kV	HUMAN BODY MODEL[1)]

[1)] MIL STD 883D, method 3015.7 and ESD Assn. standard S5.1-1993.

Note: Stresses above those listed here may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

5.1.2 Operating Range PEB 4265

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Battery voltage L	V_{BATL}	-80	-15	V	referred to V_{BGND}
Battery voltage H	V_{BATH}	-85	-20	V	referred to V_{BGND}
Auxiliary supply voltage	V_{HR}	5	85	V	referred to V_{BGND}
Total battery supply voltage	V_{HR}-V_{BATH}		150	V	
VDD supply voltage	V_{DD}	4.75	5.25	V	referred to V_{AGND}
Ground voltage difference	V_{BGND}-V_{AGND}	-0.4	0.4	V	
Junction Temperature	T_j		125	°C	simulated for a lifetime of 15 years
Voltage compliance IT,IL	V_{IT}, V_{IL}	-0.4	3.5	V	
Input range VDCP, VDCN, VACP, VACN	V_{ACDC}	0	3.3	V	

Note: It is necessary that ground connections (AGND, BGND) are established first, and then the supply voltages may be applied in any sequence.

5.2 Electrical Characteristics PEB 4266 (SLIC-P)

5.2.1 Absolute Maximum Ratings PEB 4266

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Battery voltage L	V_{BATL} V_{BATL}- V_{BATH}	-145 -0.4	0.4	V	referred to V_{BGND}
Battery voltage H	V_{BATH}	-150	0.4	V	referred to V_{BGND}
Battery voltage R	V_{BATR} V_{BATH}- V_{BATR}	-155 -0.4	0.4	V	referred to V_{BGND}
Total battery supply voltage, continuously	V_{DD}-V_{BATR}		-160	V	
VDD supply voltage	V_{DD}	-0.4	7	V	referred to V_{AGND}
Ground voltage difference	V_{BGND}- V_{AGND}	-0.4	0.4	V	
Input voltages	V_{DCP},V_{DCN}, V_{ACP},V_{ACN}, V_{C1}, V_{C2}, V_{C3}	-0.4	V_{DD}+0.4	V	referred to V_{AGND}
Voltages on current outputs	V_{IT}, V_{IL}	-0.4	V_{DD}+0.4	V	referred to V_{AGND}
RING, TIP voltages, continuously	V_R, V_T	V_{BATL}-0.4 V_{BATH}-0.4 V_{BATR}-0.4	+0.4 +0.4 +0.4	V V V	ACTL ACTH ACTR
RING,TIP voltages, pulse < 10 ms	V_R, V_T	t.b.d	t.b.d	V	ACTL, ACTH, ACTR
RING,TIP voltages, pulse < 1 ms	V_R, V_T	V_{BATR}-10	+10	V	ACTL, ACTH, ACTR
RING, TIP voltages, pulse < 1 µs	V_R, V_T	V_{BATR}-10	+30	V	ACTL, ACTH, ACTR
ESD-voltage, all pins			2	kV	HUMAN BODY MODEL[1)]

[1)] MIL STD 883D, method 3015.7 and ESD Assn. standard S5.1-1993.

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

5.2.2 Operating Range PEB 4266

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Battery voltage L	V_{BATL}	-140	-15	V	referred to V_{BGND}
Battery voltage H	V_{BATH}	-145	-20	V	referred to V_{BGND}
Battery voltage R	V_{BATR}	-150	-25	V	referred to V_{BGND}
Total battery supply voltage	V_{DD}-V_{BATR}		155	V	
VDD supply voltage	V_{DD}	4.5	5.5	V	referred to V_{AGND}
Ground voltage difference	V_{BGND}-V_{AGND}	-0.4	0.4	V	
Junction Temperature	T_j		125	°C	calculated for a lifetime of 15 years
Voltage compliance IT,IL	V_{IT}, V_{IL}	-0.4	3.5	V	
Input range VDCP, VDCN, VACO, VACN	V_{ACDC}	0	3.3	V	

Note: It is necessary that ground connections (AGND, BGND) are established first, and then the supply voltages may be applied in any sequence.

5.3 AC Transmission DuSLIC

Table 5-1 AC Transmission

Parameter	Symbol	Conditions	Limit Values			Unit
			min.	typ.	max.	
Longitudinal current capability AC	I_{ll}	per line active	30			mA_{rms}
Overload level	V_{RT}	300 - 4000 Hz	2.3			V_{rms}
Transmission Performance (2-wire)						
Return Loss	RL	200 - 3600 Hz	26			dB
Insertion Loss (2-wire to 4-wire and 4-wire to 2-wire)						
Gain accuracy - Transmit	G_X	0 dBm0, 1014 Hz	-0.25		+0.25	dB
Gain accuracy - Receive	G_R	0 dBm0, 1014 Hz	-0.25		+0.25	dB
Frequency Response						
Transmit gain Frequency variation	G_{XAF}	Reference frequency 1014 Hz, Signal level 0 dBm0, H_{FRX}=1				
		f = 0 - 300 Hz	-0.25			dB
		f = 300 - 400 Hz	-0.25		0.9	dB
		f = 400 - 600 Hz	-0.25		0.65	dB
		f = 600 - 2400 Hz	-0.25		0.25	dB
		f = 2400 - 3000 Hz	-0.25		0.45	dB
		f = 3000 - 3400 Hz	-0.25		1.4	dB
		f = 3400 - 3600 Hz	-0.25			dB
Receive gain Frequency variation	G_{RAF}	Reference frequency 1014 Hz, Signal level 0 dBm0, H_{FRR}=1				
		f = 0 - 200 Hz	0			dB
		f = 200 - 300 Hz	-0.25			dB
		f = 300 - 400 Hz	-0.25		0.9	dB
		f = 400 - 600 Hz	-0.25		0.65	dB
		f = 600 - 2400 Hz	-0.25		0.25	dB
		f = 2400 - 3000 Hz	-0.25		0.45	dB
		f = 3000 - 3400 Hz	-0.25		1.4	dB
		f = 3400 - 3600 Hz	-0.25			dB

Table 5-1 AC Transmission (cont'd)

Parameter	Symbol	Conditions	Limit Values			Unit
			min.	typ.	max.	
Gain Tracking						
Transmit gain Signal level variation	G_{XAL}	Sinusoidal test method f = 1014 Hz, Reference level -10 dBm0				
		VF_XI = - 55 to - 50 dBm0	-1.4		1.4	dB
		VF_XI = - 50 to - 40 dBm0	-0.5		0.5	dB
		VF_XI = - 40 to + 3 dBm0	-0.25		0.25	dB
Receive gain Signal level variation	G_{RAL}	Sinusoidal test method f = 1014 Hz, Reference level -10 dBm0				
		D_R0 = - 55 to - 50 dBm0	-1.4		1.4	dB
		D_R0 = - 50 to - 40 dBm0	-0.5		0.5	dB
		D_R0 = - 40 to + 3 dBm0	-0.25		0.25	dB
Balance Return Loss		300 - 3400 Hz	26			dB
Group Delay						
Transmit delay, Absolute	D_{XA}	f = 500 - 2800 Hz	400	490	585	µs
Receive delay, Absolute	D_{RA}	f = 500 - 2800 Hz	290	380	475	µs
Group delay, Receive and Transmit, Relative to 1500 Hz	D_{XR}					
		f = 500 - 600 Hz			300	µs
		f = 600 - 1000 Hz			150	µs
		f = 1000 - 2600 Hz			100	µs
		f = 2600 - 2800 Hz			150	µs
		f = 2800 - 3000 Hz			300	µs
Overload Compression A/A	OC					

Table 5-1 AC Transmission (cont'd)

Parameter	Symbol	Conditions	Limit Values			Unit
			min.	typ.	max.	
Longitudinal Balance						
Longitudinal to transversal	L-T	300 - 3400 Hz	53			dB
Transversal to longitudinal	T-L	300 - 4000 Hz	46			dB
Longitudinal signal generation	4-L	300 - 4000 Hz	46			dB
TTX Signal Generation						
TTX signal	V_{TTX}	at 200 Ω			2.5	Vrms
Out-of-band Noise (Single frequency inband -25dBm0)						
Transversal	V_{RT}	12 kHz - 200 kHz		-55	-50	dBm
Longitudinal	V_{RT}	12 kHz - 200 kHz		-55	-50	dBm
Total Harmonic Distortion						
2-wire to 4-wire	THD4	-7 dBm0, 300 - 3400 Hz		-50	-44	dB
4-wire to 2-wire	THD2	-7 dBm0, 300 - 3400 Hz		-50	-44	dB
Idle Channel Noise						
2-wire port (receive) A-law	N_{RP}	Psophometric TTX disabled TTX enabled			 -74 -70	 dBmp dBmp
µ-law	N_{RC}	C message TTX disabled TTX enabled			 16 20	 dBrnC dBrnC
PCM side (transmit) A-Law	N_{TP}	Psophometric TTX disabled TTX enabled			 -69 -67	 dBmp dBmp
µ-Law	N_{TC}	C message TTX disabled TTX enabled			 18 20	 dBrnC dBrnC

Table 5-1 AC Transmission (cont'd)

Parameter	Symbol	Conditions	Limit Values			Unit
			min.	typ.	max.	
Distortion (Sinusoidal Test Method)						
Signal to Total Distortion Transmit	STD_X	Output connection: L_X = 0 dBr f = 1014 Hz (C-message weighted for µ-law, psophometrically weighted for A-law)				
		-45 dBm0	22			dB
		-40 dBm0	27			dB
		-30 dBm0	34			dB
		-20 dBm0	36			dB
		-10 dBm0 to +3 dBm0	36			dB
Signal to Total Distortion Receive	STD_R	Input connection: L_R = - 7 dBr f = 1014 Hz (C-message weighted for µ-law, psophometrically weighted for A-law)				
		-45 dBm0	17			dB
		-40 dBm0	22			dB
		-30 dBm0	31			dB
		-20 dBm0	35.5			dB
		-10 dBm0 to +3 dBm0	36			dB
Power Supply Rejection Ratio						
VDD referenced to AGND	PSRR	300 - 3400 Hz	33			dB
		4 - 128 kHz	tbd			
VBAT referenced to AGND	PSRR	300 - 3400 Hz	33			dB
		4 - 128 kHz	tbd			

5.4 DC Characteristics

Table 5-2 DC Characteristics

Parameter	Symbol	Conditions	Limit Values			Unit
			min.	typ.	max.	
Line Termination Tip, Ring						
Sinusoidal Ringing						
Max. ringing voltage	V_{RNG0}	V_H-V_{BAT} = 150V, V_{DC} = 20 V for ring trip	85			V_{rms}
Output impedance	R_{OUT}	SLIC output buffer and R_{STAB}		61		Ω
Harmonic distortion	THD				5	%
Output current limit	$\lvert I_{R, max} \rvert$, $\lvert I_{T, max} \rvert$	Modes: Active SLIC-E: SLIC-P:	 85 70		 120 100	 mA mA
Loop current accuracy				tbd	4	%
Loop open resistance TIP to V_{BGND}	R_{TG}	Modes: Power Down I_{TIP} = 2mA		5		kΩ
Loop open resistance RING to V_{BAT}	R_{BG}	Modes: Power Down I_R = 2mA		5		kΩ
Ring trip function						
Ring trip DC voltage		SLIC-E: SLIC-P: balanced SLIC-P: unbalanced	0 0	 $V_{BATR}/2$	30 30	Vdc Vdc Vdc
Ring trip detection time delay					2	periods
Ring off time delay					2	periods

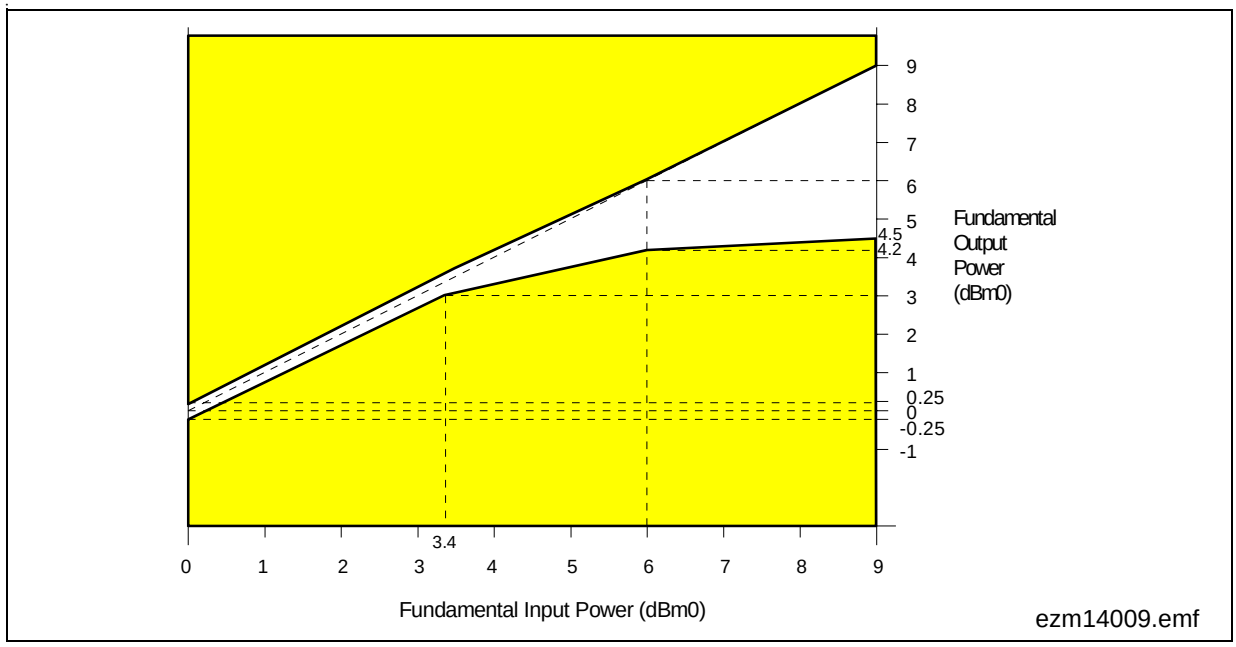

Figure 5-1 Overload Compression

6 Application Circuits

Application circuits are shown for balanced ringing with DuSLIC-E/S, for unbalanced ringing with DuSLIC-P and for external unbalanced ringing with DuSLIC-E/S for two lines. Channel A and the SLIC have to be duplicated in the circuit diagrams to show all components.

6.1 Balanced Ringing

Internal balanced ringing is supported up to 85 Vrms for DuSLIC-E/E2 and up to 45 Vrms for DuSLIC-S. With the DuSLIC-E/P versions line testing and board testing are fully integrated, test relays are not necessary.

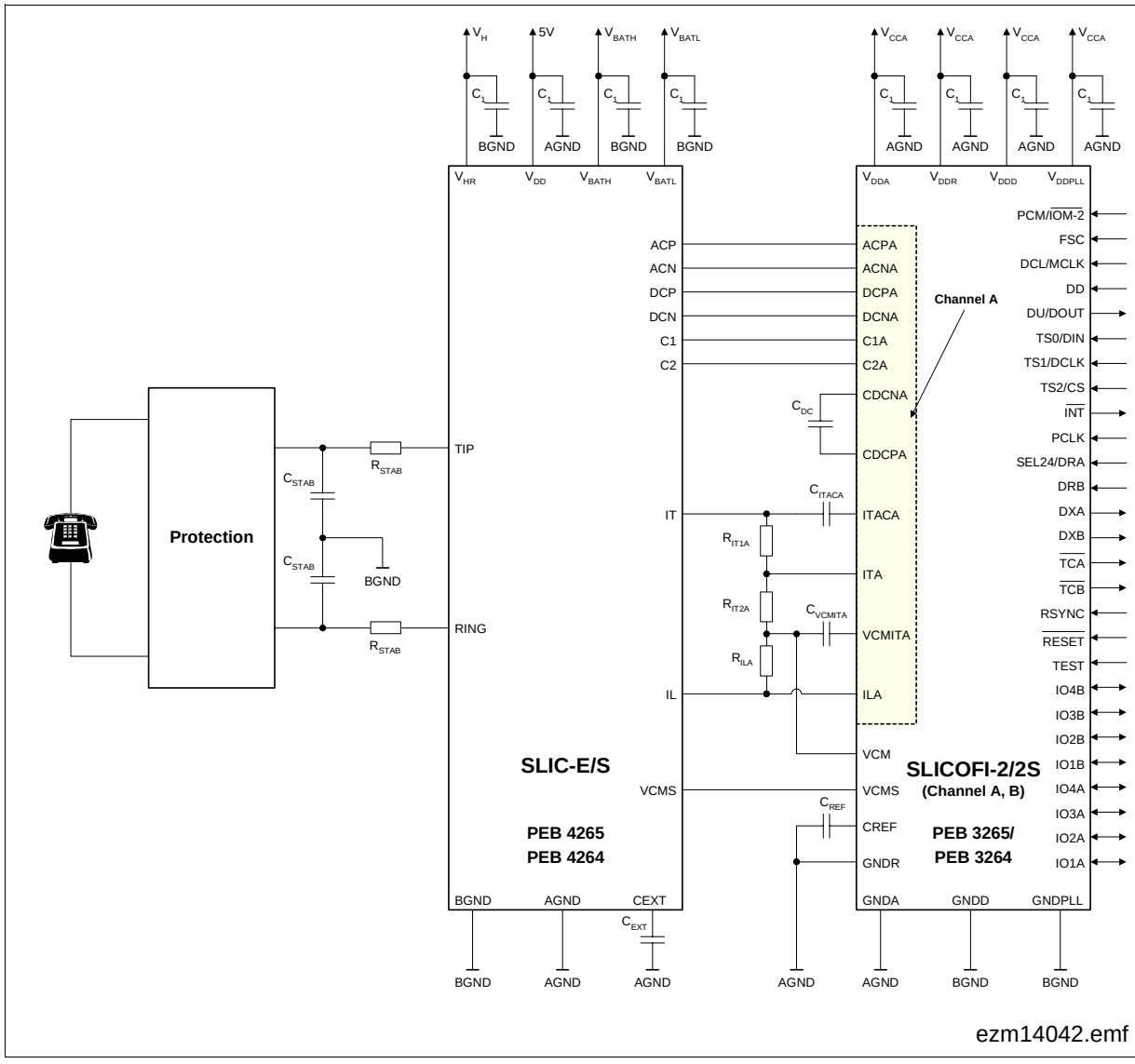

Figure 6-1 Application Circuit, Internal Balanced Ringing

6.1.1 Protection Circuit for SLIC-E and SLIC-S

A typical overvoltage protection circuit for SLIC-E/S is shown in **Figure 6-2**. Other proved application schemes are available on request.

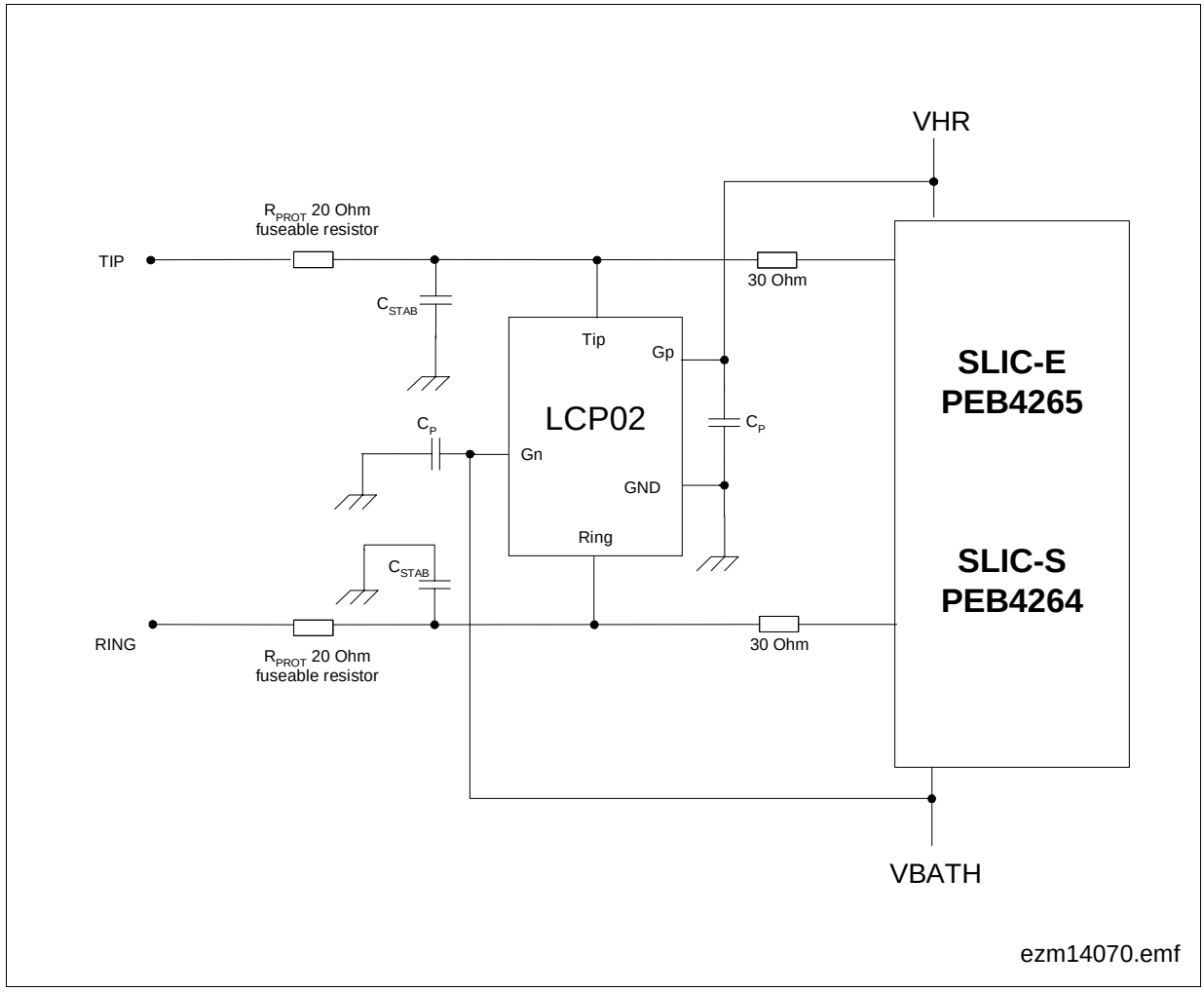

Figure 6-2 Typical Overvoltage Protection for SLIC-E and SLIC-S

The LCP02 (from STM) protects against overvoltage strikes exceeding V_{HR} and V_{BATH}. Protection resistors must be rated for lightning pulses. In case of power contact, protection resistors must go open or additional fuses are needed.

Table 6-1 List of Passive Components in Application Circuits for DuSLIC-E/S

(calculated for a dual channel solution consisting of one SLICOFI-2 and two SLICs)

No.	Symbol	Value	Unit	Tolerance	Rating
2	R_{IT1}	470	Ω	1%	
2	R_{IT2}	680	Ω	1%	
2	R_{IL}	1.6	kΩ	1%	
4	R_{STAB}	30	Ω	0.1%	
4	R_{PROT}	20	Ω	0.1%	
4	C_{STAB}	15	nF	10%	according to V_{BATH} or V_{HR}
2	C_{DC}	120	nF	10%	10 V
2	C_{ITAC}	680	nF	10%	10 V
2	C_{VCMIT}	680	nF	10%	10 V
1	C_{REF}	68	nF	20%	10 V
2	C_{EXT}	470	nF	20%	10 V
12	C_1	100	nF	10%	according to supply voltages
2	STM	LCP02	–	–	
4	C_P	220	nF	10%	according to V_{BATH} or V_{HR}

For handling higher electromagnetic compatibility (EMC) requirements, additional effort in the circuit design may be necessary, e.g., a current-compensated choke of 470 µH in the Ring/Tip lines.

Additionally to the capacitors C_1 a 22 µF capacitor per 8 Ring/Tip lines is recommended for buffering the supply voltages.

6.2 Unbalanced Ringing

In applications with the SLIC-P, unbalanced ringing is fully supported up to 50 Vrms ringing voltage without any additional external components (see **Figure 6-3**).

For unbalanced ringing with more than 50 Vrms ringing voltage (e.g. 75 Vrms), an external ring generator and a relay for one line (Ring or Tip) have to be used (see circuit proposals in **Figure 6-5** and **Figure 6-6**).

On the other line, a DC voltage for ring trip detection can be fed to the subscriber by the DuSLIC.

Off-hook detection and ring trip detection are fully integrated in the DuSLIC chip set (there is no need for external components).

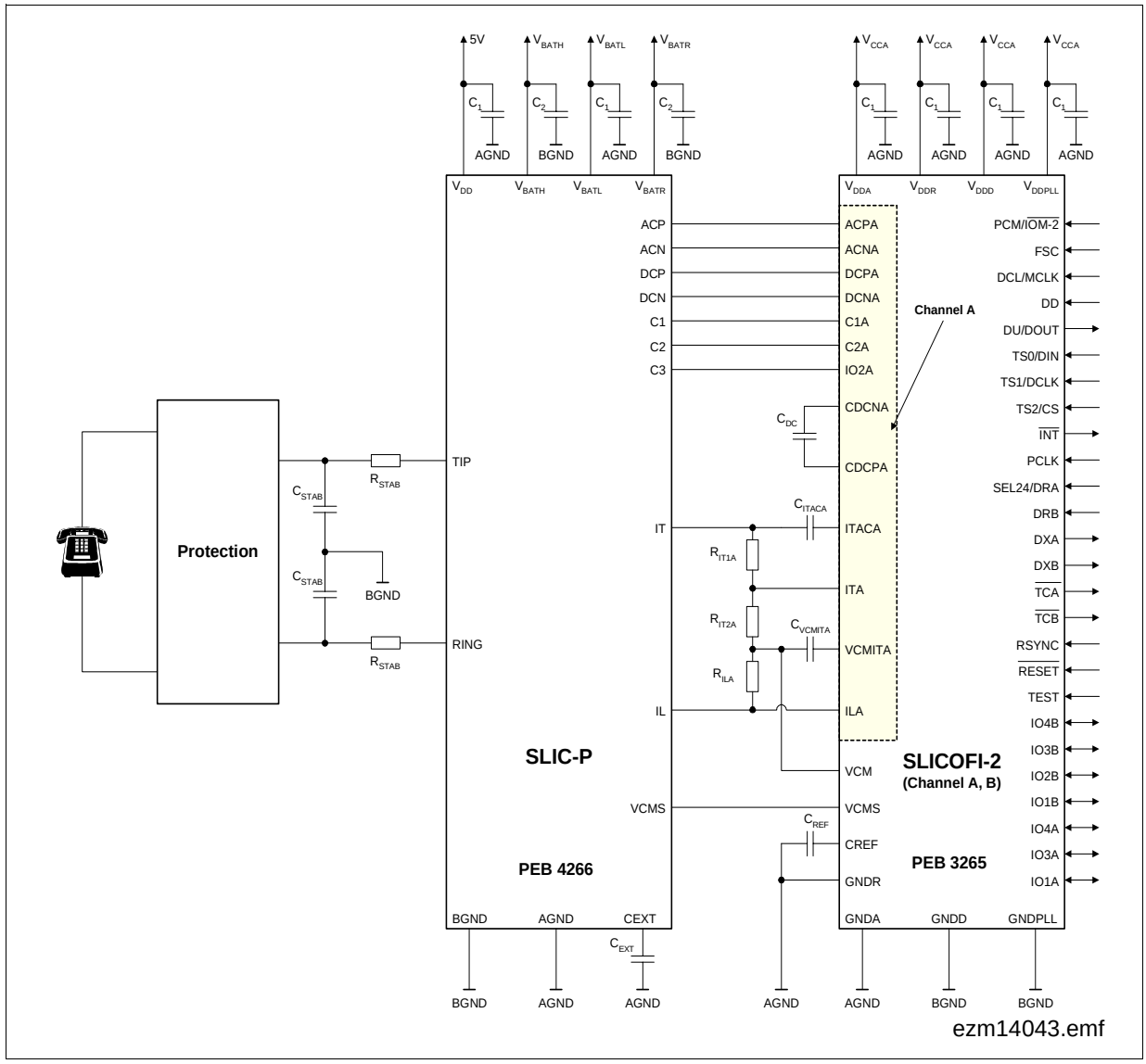

Figure 6-3 Application Circuit, Unbalanced Ringing with SLIC-P (PEB 4266)

6.2.1 Protection Circuit for SLIC-P

A typical protection circuit for SLIC-P is shown in **Figure 6-4**. Other proved application schemes are available on request.

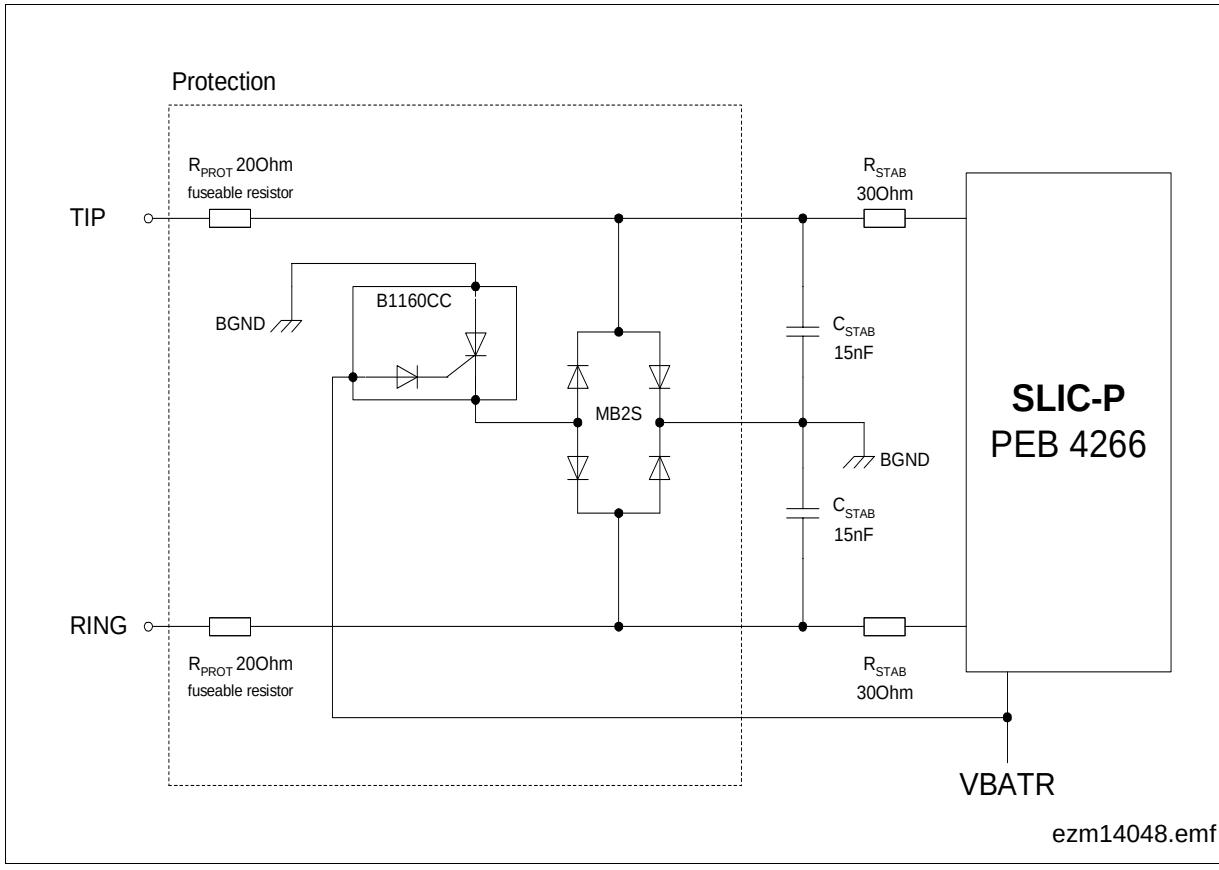

Figure 6-4 Typical Overvoltage Protection for SLIC-P

The gate trigger voltage of the Battrax B1160CC (Teccor) can be set down to the battery voltage of V_{BATR} (– 150 V).

Protection resistors must be rated for lightning pulses. In case of power contact, protection resistors must go open circuit or additional fuses are needed.

Table 6-2 List of Passive Components in Application Circuits for DuSLIC-P

(calculated for a dual channel solution consisting of one SLICOFI-2 and two SLICs)

No.	Symbol	Value	Unit	Tolerance	Rating
2	R_{IT1}	470	Ω	1%	
2	R_{IT2}	680	Ω	1%	
2	R_{IL}	1.6	kΩ	1%	
4	R_{STAB}	30	Ω	0.1%	
4	R_{PROT}	20	Ω	0.1%	
4	C_{STAB}	15	nF	10%	according to V_{BATR}
2	C_{DC}	120	nF	10%	10 V
2	C_{ITAC}	680	nF	10%	10 V
2	C_{VCMIT}	680	nF	10%	10 V
1	C_{REF}	68	nF	20%	10 V
2	C_{EXT}	470	nF	20%	10 V
12	C_1	100	nF	10%	
2	Battrax	B1160CC	–	–	according to supply voltage
2	Diodebridge	MB2S			

For handling higher electromagnetic compatibility (EMC) requirements, additional effort in the circuit design may be necessary, e.g., a current-compensated choke of 470 µH in the Ring/Tip lines.

Additionally to the capacitors C_1 a 22 µF capacitor per 8 Ring/Tip lines is recommended for buffering the supply voltages.

6.3 External Unbalanced Ringing with DuSLIC-S/E/P

External unbalanced ringing applications are shown for a standard solution (see **Figure 6-5**) and for a solution dedicated to higher loop lenghts (see **Figure 6-6**).

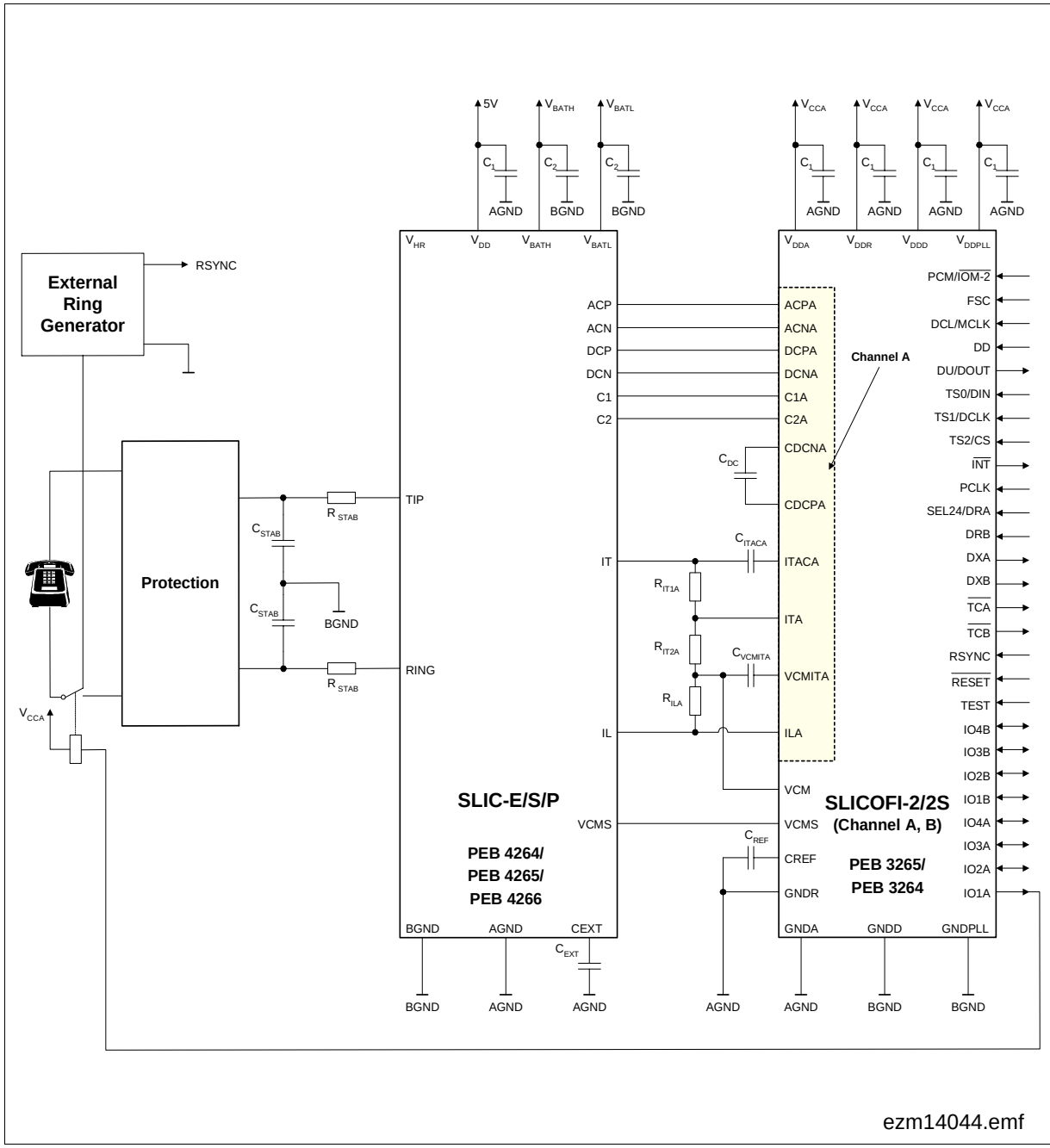

Figure 6-5 Application Circuit, External Unbalanced Ringing

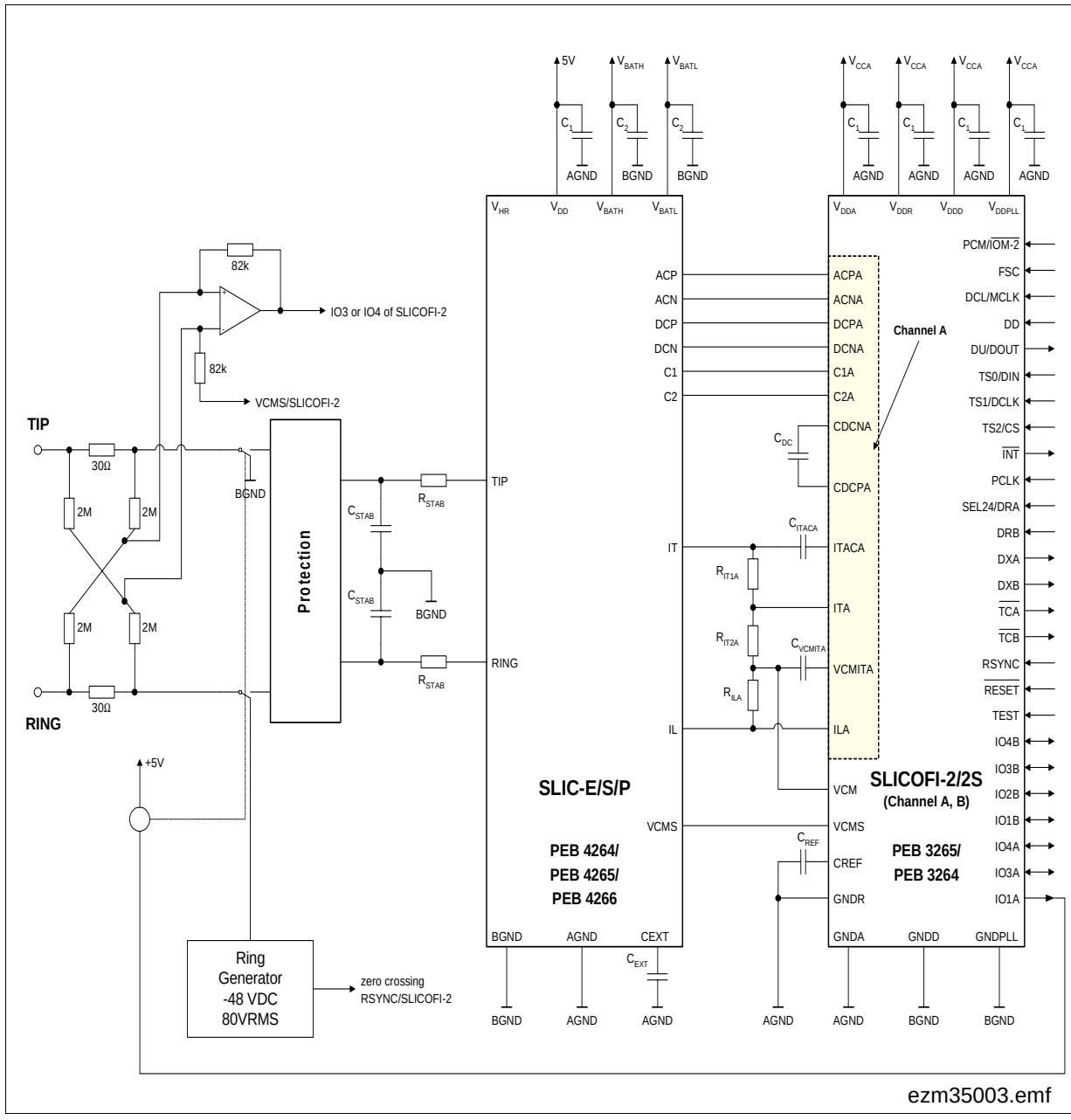

Figure 6-6 Application Circuit, External Unbalanced Ringing for Long Loops

For handling higher electromagnetic compatibility (EMC) requirements, additional effort in the circuit design may be necessary, e.g., a current-compensated choke of 470 µH in the Ring/Tip lines.