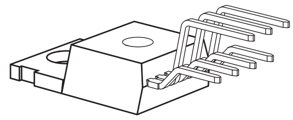
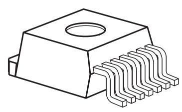
5-V Low Drop Voltage Regulator TLE 4267

Features

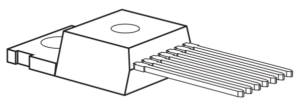
- Output voltage tolerance ≤ ±2%
- 400 mA output current capability
- Low-drop voltage
- Very low standby current consumption
- Input voltage up to 40 V
- Overvoltage protection up to 60 V (≤ 400 ms)
- Reset function down to 1 V output voltage
- ESD protection up to 2000 V
- Adjustable reset time
- On/off logic
- Overtemperature protection
- Reverse polarity protection
- Short-circuit proof
- Wide temperature range
- Suitable for use in automotive electronics



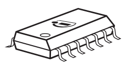
P-TO220-7-3



P-TO 220-7-180
(TO-220 AB/7, Option E3180)



P-TO220-7-230



P-DSO-14-3, -8, -9, -11, 14

Functional Description

TLE 4267 is a 5-V low drop voltage regulator for automotive applications in the P-TO220-7 or P-DSO-14-8 package. It supplies an output current of > 400 mA. The IC is shortcircuit-proof and has an overtemperature protection circuit.

Application

The IC regulates an input voltage V_I in the range of 5.5 V < V_I < 40 V to a nominal output voltage of

Type	Ordering Code	Package
TLE 4267	Q67000-A9153	P-TO220-7-3, P-TO220-7-11
TLE 4267 G	Q67006-A9169	P-TO220-7-180, P-TO220-7-4
TLE 4267 S	Q67000-A9246	P-TO220-7-230, P-TO220-7-12
TLE 4267 GM	Q67006-A9398	P-DSO-14-8

V_Q = 5.0 V. A reset signal is generated for an output voltage of $V_Q < V_{RT}$ (typ. 4.5 V). The reset delay can be set with an external capacitor. The device has two logic inputs. A voltage of V_{E2} > 4.0 V given to the E2-pin (e.g. by ignition) turns the device on. Depending on the voltage on pin E6 the IC may be hold in active-state even if V_{E2} goes to low level. This makes it simple to implement a self-holding circuit without external components. When the device is turned off, the output voltage drops to 0 V and current consumption tends towards 0 µA.

Design Notes for External Components

The input capacitor C_I is necessary for compensation of line influences. The resonant circuit consisting of lead inductance and input capacitance can be damped by a resistor of approx. 1 Ω in series with C_I. The output capacitor is necessary for the stability of the regulating circuit. Stability is guaranteed at values of ≥ 22 µF and an ESR of ≤ 3 Ω within the operating temperature range.

Circuit Description

The control amplifier compares a reference voltage, which is kept highly accurate by resistance adjustment, to a voltage that is proportional to the output voltage and drives the base of the series transistor via a buffer. Saturation control as a function of the load current prevents any over-saturating of the power element.

The reset output RO is in high-state if the voltage on the delay capacitor C_D is greater or equal V_{UD}. The delay capacitance C_D is charged with the current I_D for output voltages greater than the reset threshold V_{RT}. If the output voltage gets lower than V_{RT} a fast discharge of the delay capacitor C_D sets in and as soon as V_{CD} gets lower than V_{LD} the reset output RO is set to low-level (see **Figure 6**). The reset delay can be set within wide range by dimensioning the capacitance of the external capacitor.

Table 1 Truth Table for Turn-ON/Turn-OFF Logic

E2, Inhibit	E6, Hold	V_Q	Remarks
L	X	OFF	Initial state, Inhibit internally pulled-up
H	X	ON	Regulator switched on via Inhibit, by ignition for example
H	L	ON	Hold clamped active to ground by controller while Inhibit is still high
X	L	ON	Previous state remains, even ignition is shut off: self-holding state
L	L	ON	Ignition shut off while regulator is in self-holding state
L	H	OFF	Regulator shut down by releasing of Hold while Inhibit remains Low, final state. No active clamping required by external self-holding circuit (μC) to keep regulator in off-state.

Inhibit: E2 Enable function, active High
Hold: E6 Hold and release function, active Low

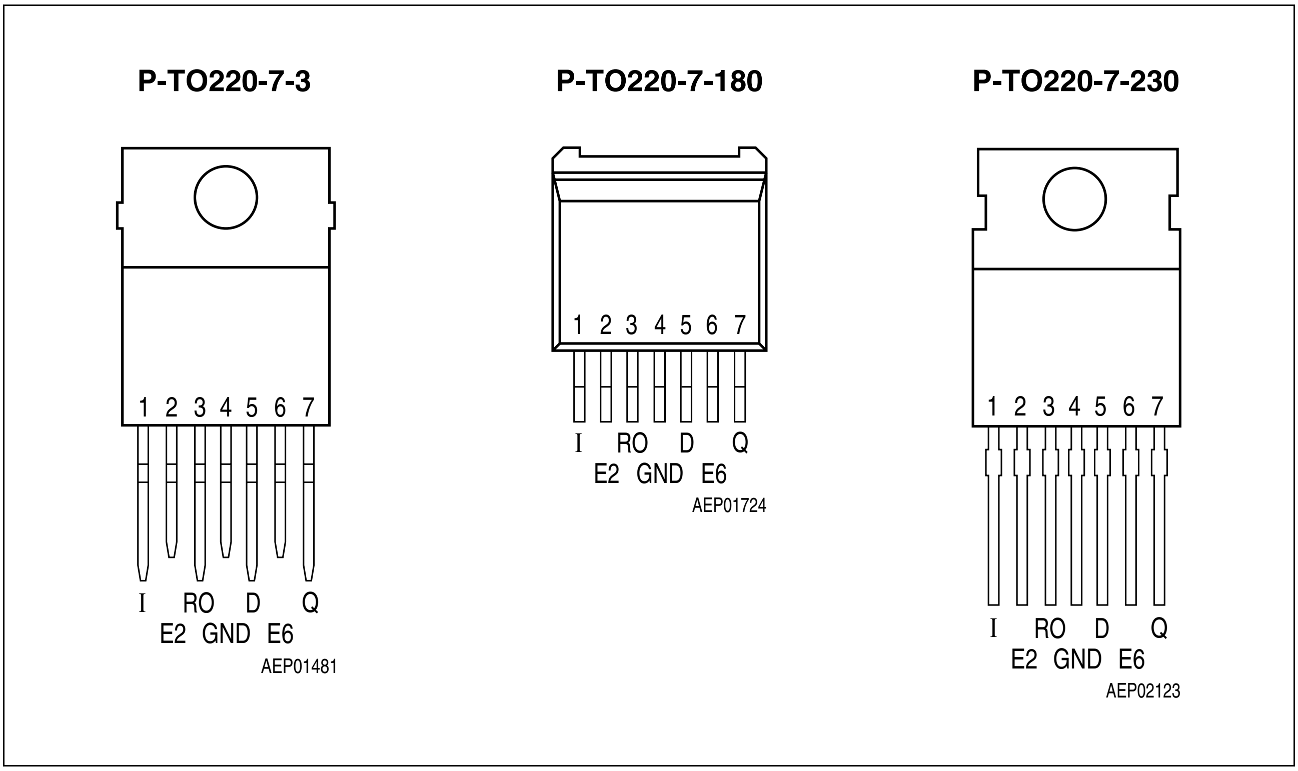


Figure 1 Pin Configuration (top view)

Table 2 Pin Definitions and Functions

Pin	Symbol	Function
1	I	**Input;** block to ground directly at the IC by a ceramic capacitor
2	E2	**Inhibit;** device is turned on by High signal on this pin; internal pull-down resistor of 100 kΩ
3	RO	**Reset Output;** open-collector output internally connected to the output via a resistor of 30 kΩ
4	GND	**Ground;** connected to rear of chip
5	D	**Reset Delay;** connect via capacitor to GND
6	E6	**Hold;** see **Table 1** for function; this input is connected to output voltage via a pull-up resistor of 50 kΩ
7	Q	**5-V Output;** block to GND with 22-µF capacitor, ESR < 3 Ω

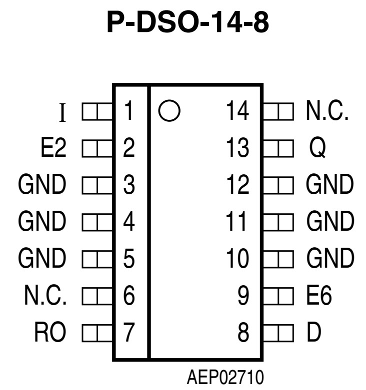


Figure 2 **Pin Configuration** (top view)

Table 3 **Pin Definitions and Functions**

Pin	Symbol	Function
1	I	**Input;** block to ground directly at the IC by a ceramic capacitor
2	E2	**Inhibit;** device is turned on by High signal on this pin; internal pull-down resistor of 100 kΩ
7	RO	**Reset Output;** open-collector output internally connected to the output via a resistor of 30 kΩ
3, 4, 5, 10, 11, 12	GND	**Ground;** connected to rear of chip
8	D	**Reset Delay;** connect with capacitor to GND for setting delay
9	E6	**Hold;** see **Table 1** for function; this input is connected to output voltage via a pull-up resistor of 50 kΩ
13	Q	**5-V Output;** block to GND with 22-µF capacitor, ESR ≤ 3 Ω
6, 14	N.C.	Not Connected

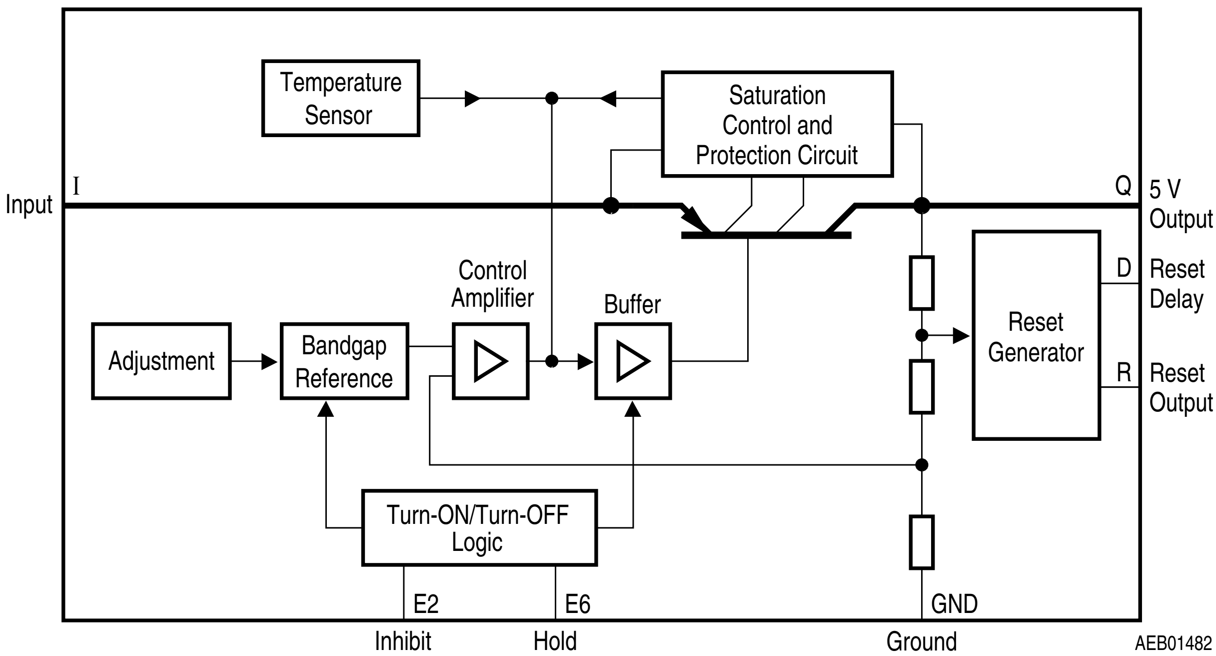


Figure 3 Block Diagram

Table 4 Absolute Maximum Ratings

T_J = -40 to 150 °C

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Input					
Voltage	V_I	-42	42	V	–
Voltage	V_I	–	60	V	$t \leq$ 400 ms
Current	I_I	–	–	–	internally limited
Reset Output					
Voltage	V_{RO}	-0.3	7	V	–
Current	I_{RO}	–	–	–	internally limited
Reset Delay					
Voltage	V_D	-0.3	42	V	–
Current	I_D	–	–	–	–
Output					
Voltage	V_Q	-0.3	7	V	–
Current	I_Q	–	–	–	internally limited
Inhibit					
Voltage	V_{E2}	-42	42	V	–
Current	I_{E2}	-5	5	mA	$t \leq$ 400 ms
Hold					
Voltage	V_{E6}	-0.3	7	V	–
Current	I_{E6}	–	–	mA	internally limited
GND					
Current	I_{GND}	-0.5	–	A	–
Temperatures					
Junction temperature	T_J	–	150	°C	–
Storage temperature	T_{stg}	-50	150	°C	–

Table 5 Operating Range

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Input voltage	V_I	5.5	40	V	see diagram
Junction temperature	T_J	-40	150	°C	–
Thermal Resistance					
Junction ambient	R_{thja}	–	65	K/W	P-TO220-7-3 package
Junction-case	R_{thjc}	–	6	K/W	P-TO220-7-3 package
Junction-case	Z_{thjc}	–	2	K/W	T < 1 ms P-TO220-7-3 package
Junction ambient	R_{thja}	–	70	K/W	P-TO220-7-180 (SMD) package
Junction-case	R_{thjc}	–	6	K/W	P-TO220-7-180 (SMD) package
Junction-case	Z_{thjc}	–	2	K/W	T < 1 ms P-TO220-7-180 (SMD) package
Junction ambient	R_{thja}	–	65	K/W	P-TO220-7-230 package
Junction-case	R_{thjc}	–	6	K/W	P-TO220-7-230 package
Junction-case	Z_{thjc}	–	2	K/W	T < 1 ms P-TO220-7-230 package
Junction ambient	R_{thja}	–	70	K/W	P-DSO-14-8 package
Junction-pin	R_{thjp}	–	30	K/W	P-DSO-14-8 package

Table 6 Characteristics

V_I = 13.5 V; -40 °C < T_J < 125 °C; V_{E2} > 4 V (unless specified otherwise)

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Output voltage	V_Q	4.9	5	5.1	V	5 mA ≤ I_Q ≤ 400 mA 6 V ≤ V_I ≤ 26 V
Output voltage	V_Q	4.9	5	5.1	V	5 mA ≤ I_Q ≤ 150 mA 6 V ≤ V_I ≤ 40 V
Output current limiting	I_Q	500	–	–	mA	T_J = 25 °C
Current consumption $I_q = I_I - I_Q$	I_q	–	–	50	µA	IC turned off
Current consumption $I_q = I_I - I_Q$	I_q	–	1.0	10	µA	T_J = 25 °C IC turned off
Current consumption $I_q = I_I - I_Q$	I_q	–	1.3	4	mA	I_Q = 5 mA IC turned on
Current consumption $I_q = I_I - I_Q$	I_q	–	–	60	mA	I_Q = 400 mA
Current consumption $I_q = I_I - I_Q$	I_q	–	–	80	mA	I_Q = 400 mA V_I = 5 V
Drop voltage	V_{Dr}	–	0.3	0.6	V	I_Q = 400 mA[1)]
Load regulation	ΔV_Q	–	–	50	mV	5 mA ≤ I_Q ≤ 400 mA
Supply-voltage regulation	ΔV_Q	–	15	25	mV	V_I = 6 to 36 V; I_Q = 5 mA
Supply-voltage rejection	SVR	–	54	–	dB	f_r = 100 Hz; V_r = 0.5 Vpp
Longterm stability	ΔV_Q	–	0	–	mV	1000 h
Reset Generator						
Switching threshold	V_{RT}	4.2	4.5	4.8	V	–
Reset High level	–	4.5	–	–	V	$R_{ext} = \infty$
Saturation voltage	$V_{RO,SAT}$	–	0.1	0.4	V	R_R = 4.7 kΩ [2)]
Internal Pull-up resistor	R_{RO}	–	30	–	kΩ	–
Saturation voltage	$V_{D,SAT}$	–	50	100	mV	$V_Q < V_{RT}$
Charge current	I_D	8	15	25	µA	V_D = 1.5 V
Upper delay switching threshold	V_{UD}	2.6	3	3.3	V	–

Table 6 Characteristics (cont'd)

V_I = 13.5 V; -40 °C < T_J < 125 °C; V_{E2} > 4 V (unless specified otherwise)

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Delay time	t_D	–	20	–	ms	C_d = 100 nF
Lower delay switching threshold	V_{LD}	–	0.43	–	V	–
Reset reaction time	t_{RR}	–	2	–	µs	C_d = 100 nF
Inhibit						
Turn on voltage	$V_{U,INH}$	–	3	4	V	IC turned on
Turn off voltage	$V_{L,INH}$	2	–	–	V	IC turned off
Pull-down resistor	R_{INH}	50	100	200	kΩ	–
Hysteresis	ΔV_{INH}	0.2	0.5	0.8	V	–
Input current	I_{INH}	–	35	100	µA	V_{INH} = 4 V
Hold voltage	$V_{U,HOLD}$	30	35	40	%	Referred to V_Q
Turn off voltage	$V_{L,HOLD}$	60	70	80	%	Referred to V_Q
Pull-up resistor	R_{HOLD}	20	50	100	kΩ	–
Overvoltage Protection						
Turn off voltage	$V_{I,OV}$	42	44	46	V	V_I increasing
Turn on voltage	$V_{I,turn\ on}$	36	–	–	V	V_I decreasing after turn off

1) Drop voltage = V_I - V_Q (measured when the output voltage V_Q has dropped 100 mV from the nominal value obtained at V_I = 13.5 V)

2) The reset output is Low for 1 V < V_Q < V_{RT}

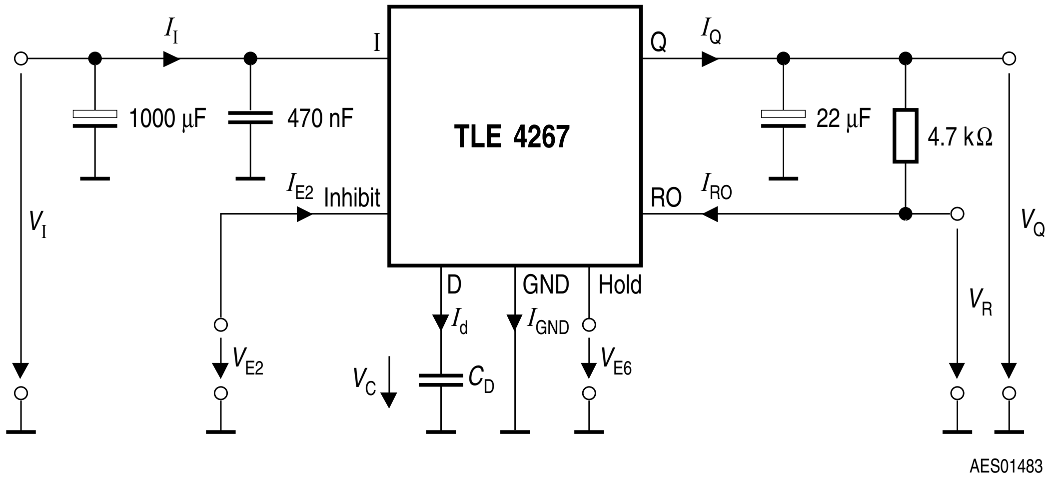


Figure 4 Test Circuit

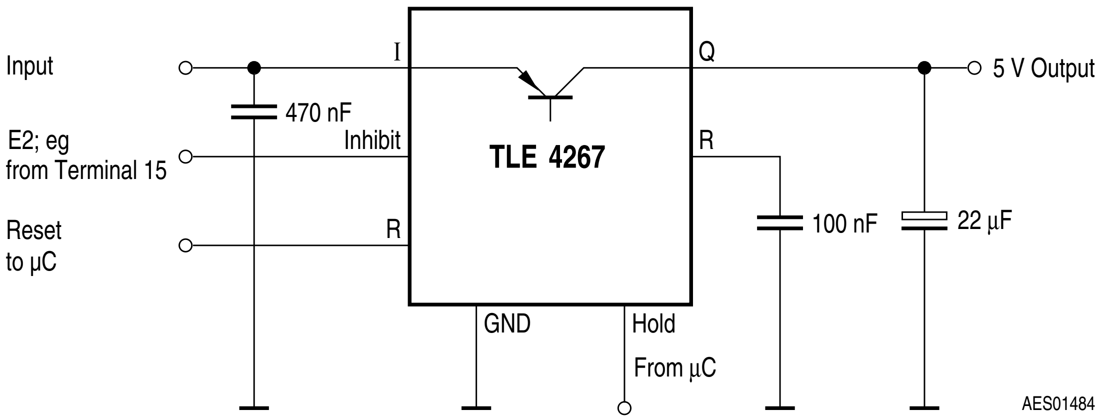


Figure 5 Application Circuit

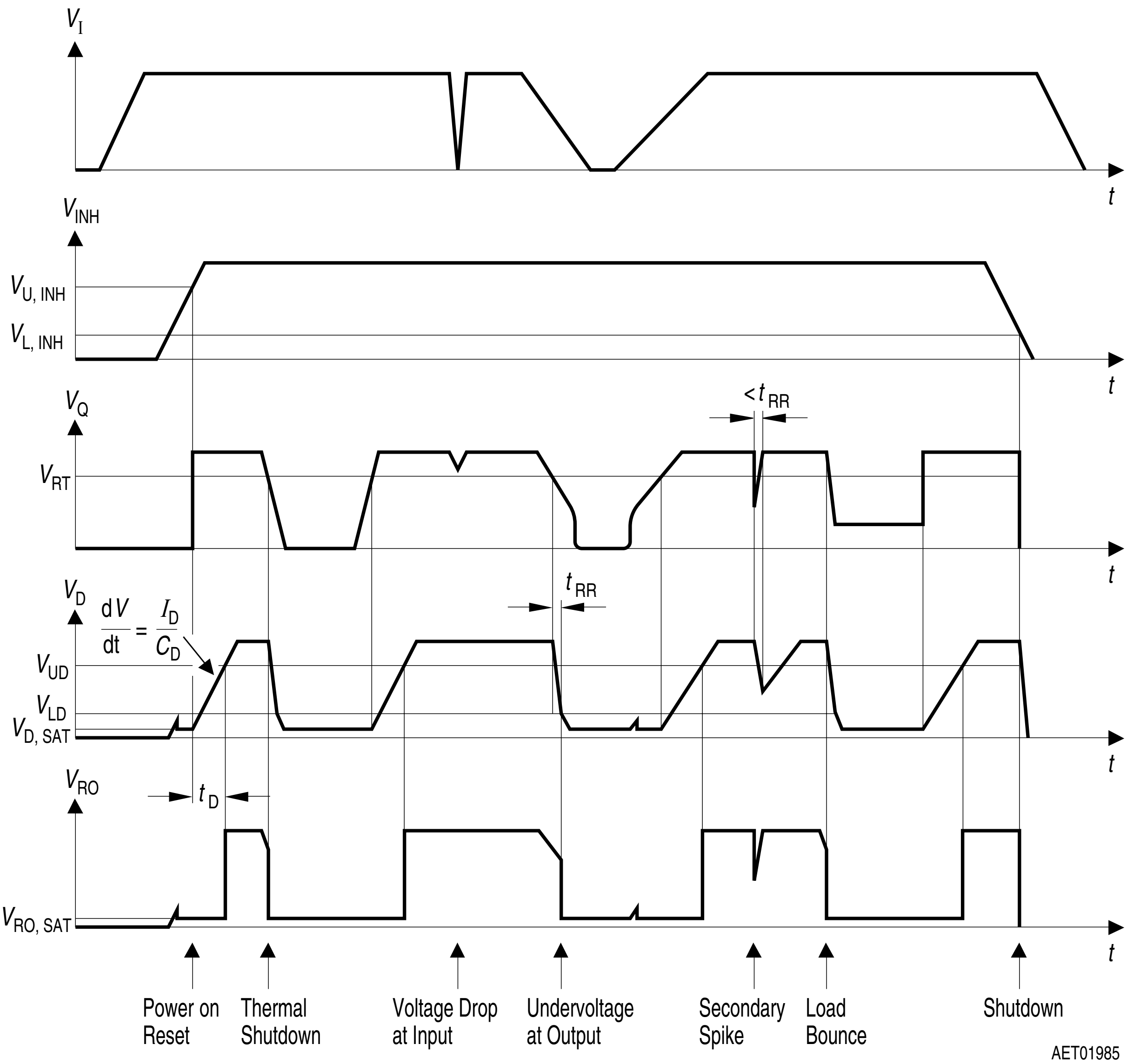
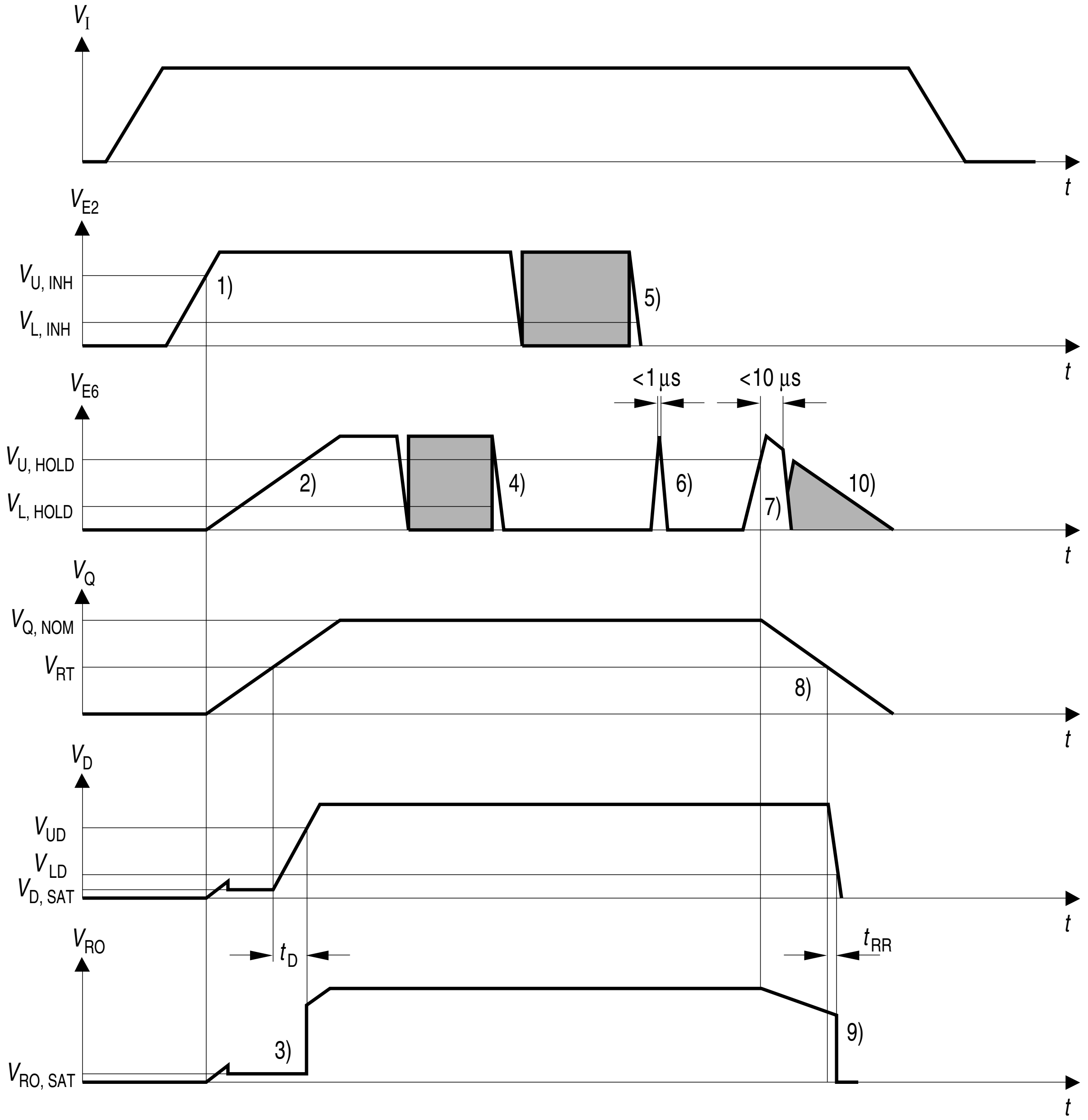


Figure 6 Time Response



1) Enable active
2) Hold inactive, pulled up by V_Q
3) Power-ON reset
4) Hold active, clamped to GND by external µC
5) Enable inactive, clamped by int. pull-down resistor
6) Pulse width smaller than 1 µs
7) Hold inactive, released by µC
8) Voltage controller shutdown
9) Output-low reset
10) No switch on via V_{E6} possible after E6 was released to $V_{E6} > V_{E6, rel}$ for more than 4 µs

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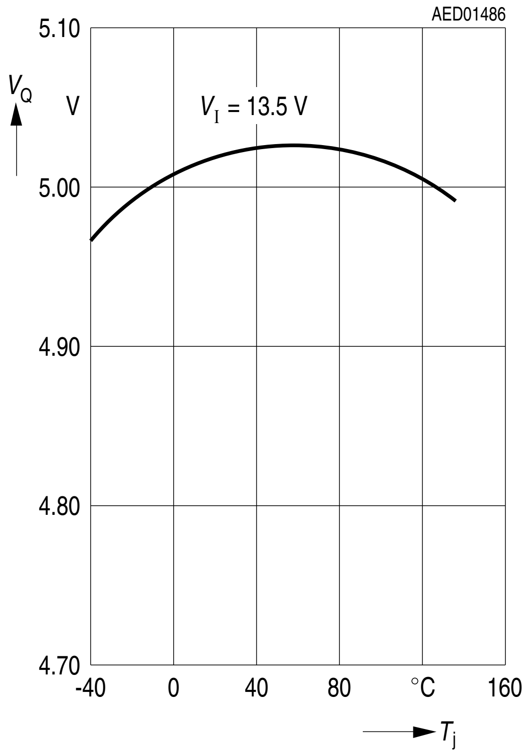
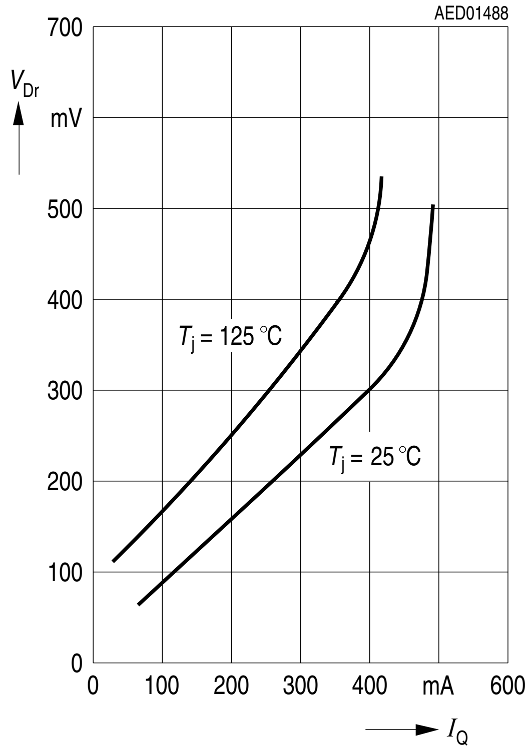
Figure 7 Enable and Hold Behavior

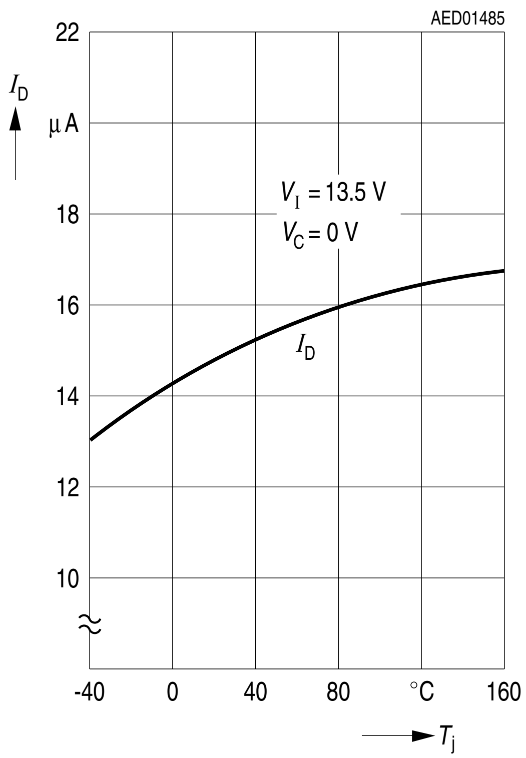
Output Voltage V_Q versus Temperature T_j



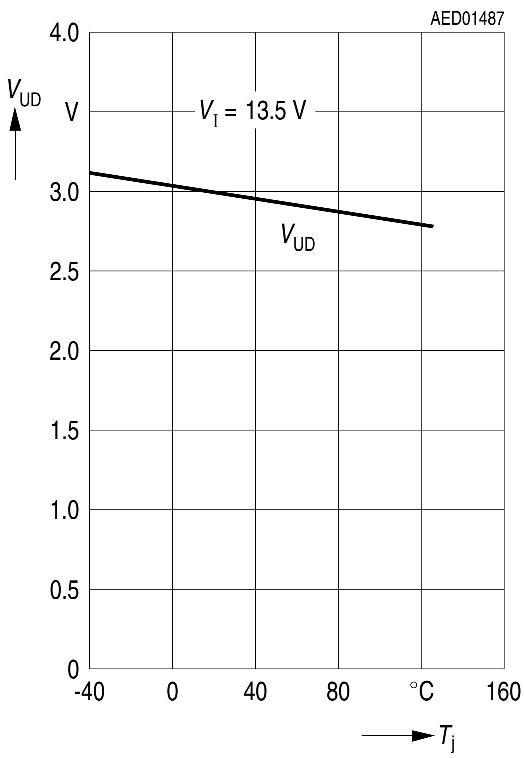
Drop Voltage V_{Dr} versus Output Current I_Q



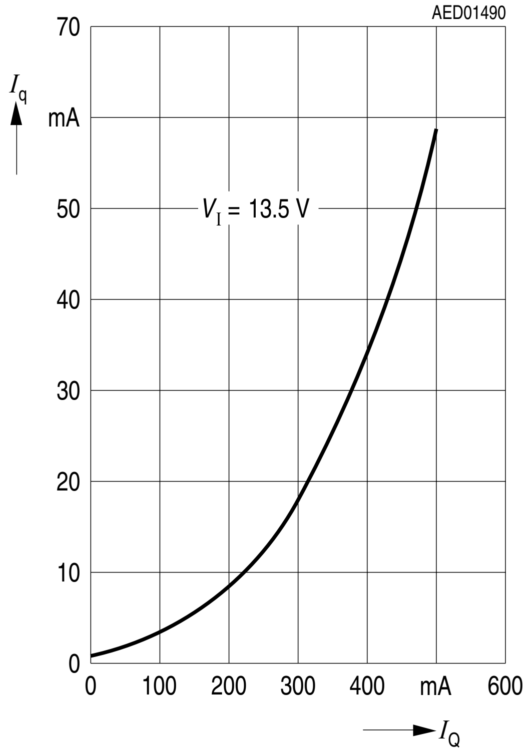
Charge Current I_D versus Temperature T_j



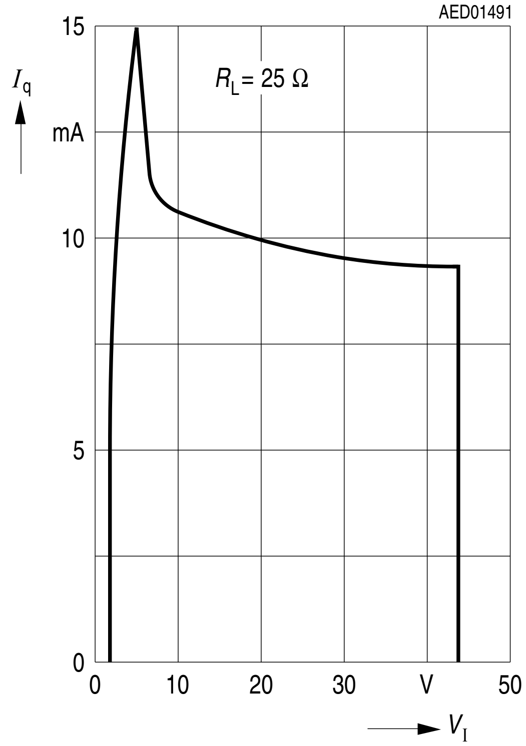
Delay Switching Threshold V_{UD} versus Temperature T_j



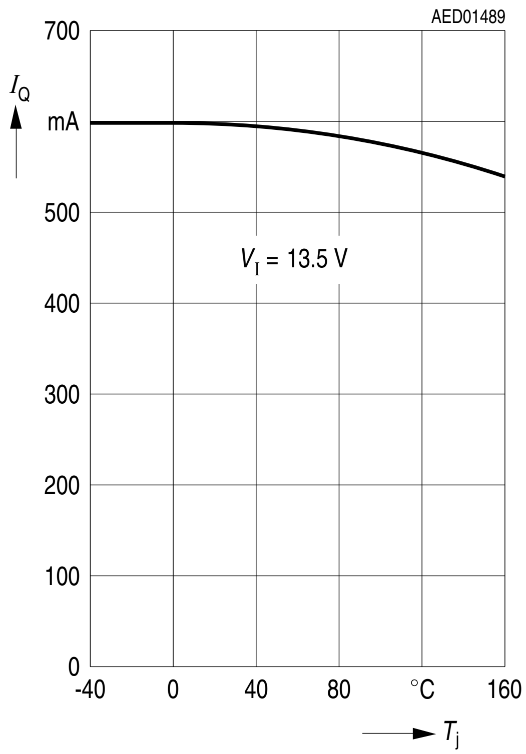
Current Consumption I_q versus Output Current I_Q



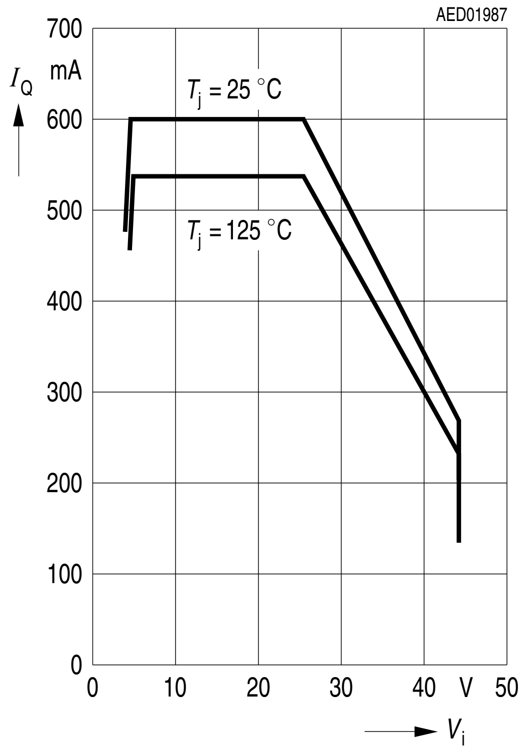
Current Consumption I_q versus Input Voltage V_I



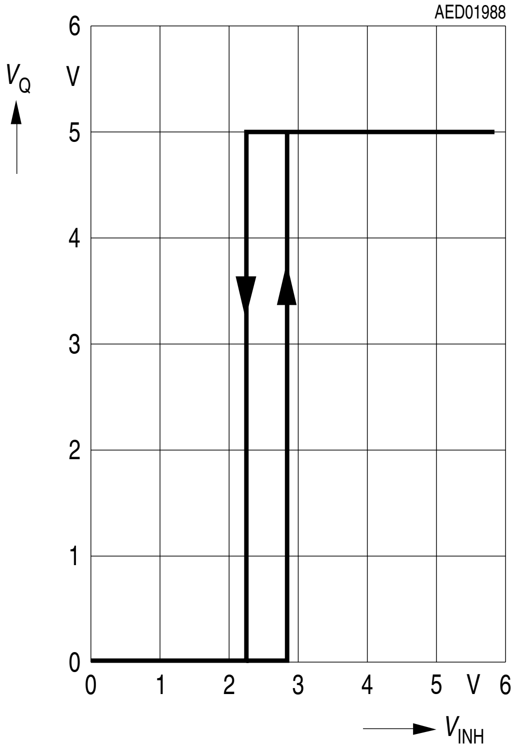
Output Current Limiting I_Q versus Temperature T_j



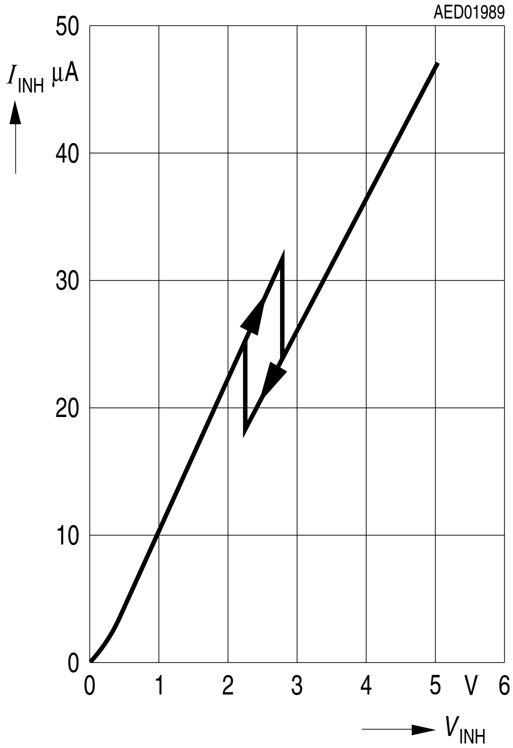
Output Current Limiting I_Q versus Input Voltage V_I



Output Voltage V_Q versus Inhibit Voltage V_{INH}



Inhibit Current I_{INH} versus Inhibit Voltage V_{INH}



Package Outlines

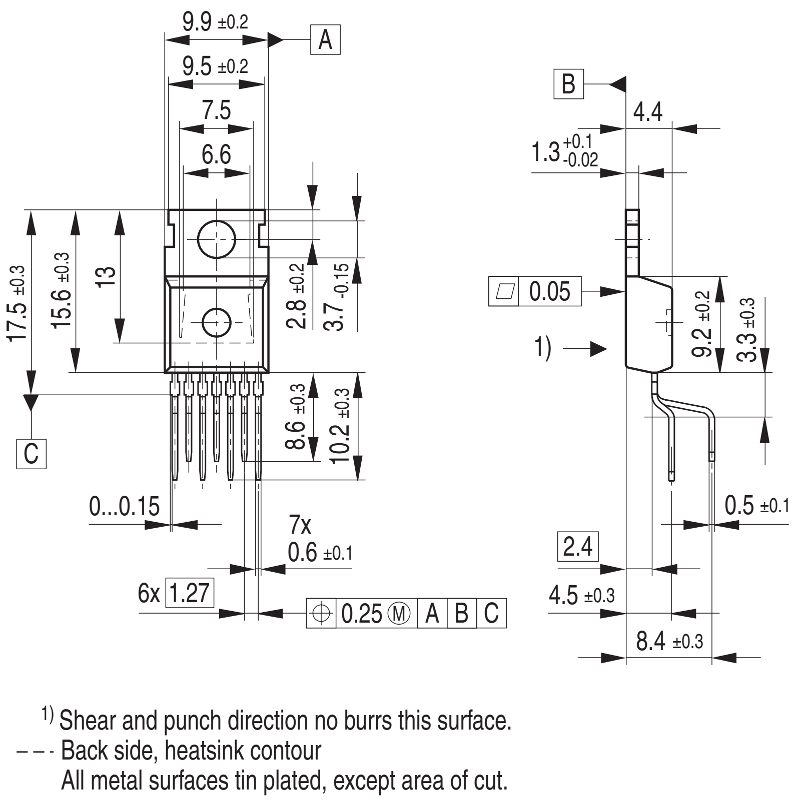


Figure 8 **P-TO220-7-3** (Plastic Transistor Single Outline)

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SMD = Surface Mounted Device

Dimensions in mm

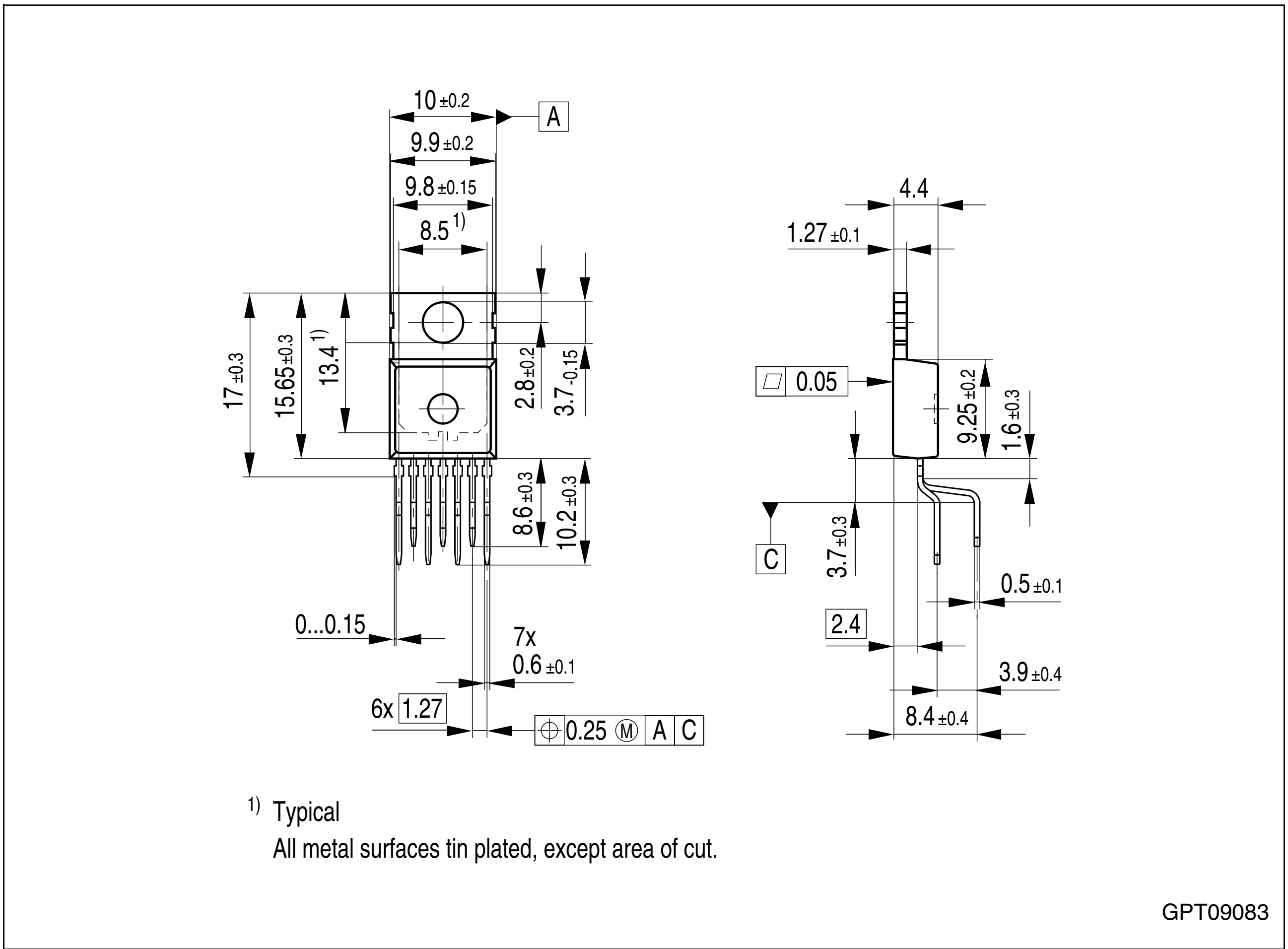

Figure 9 **P-TO220-7-11** (Plastic Transistor Single Outline)

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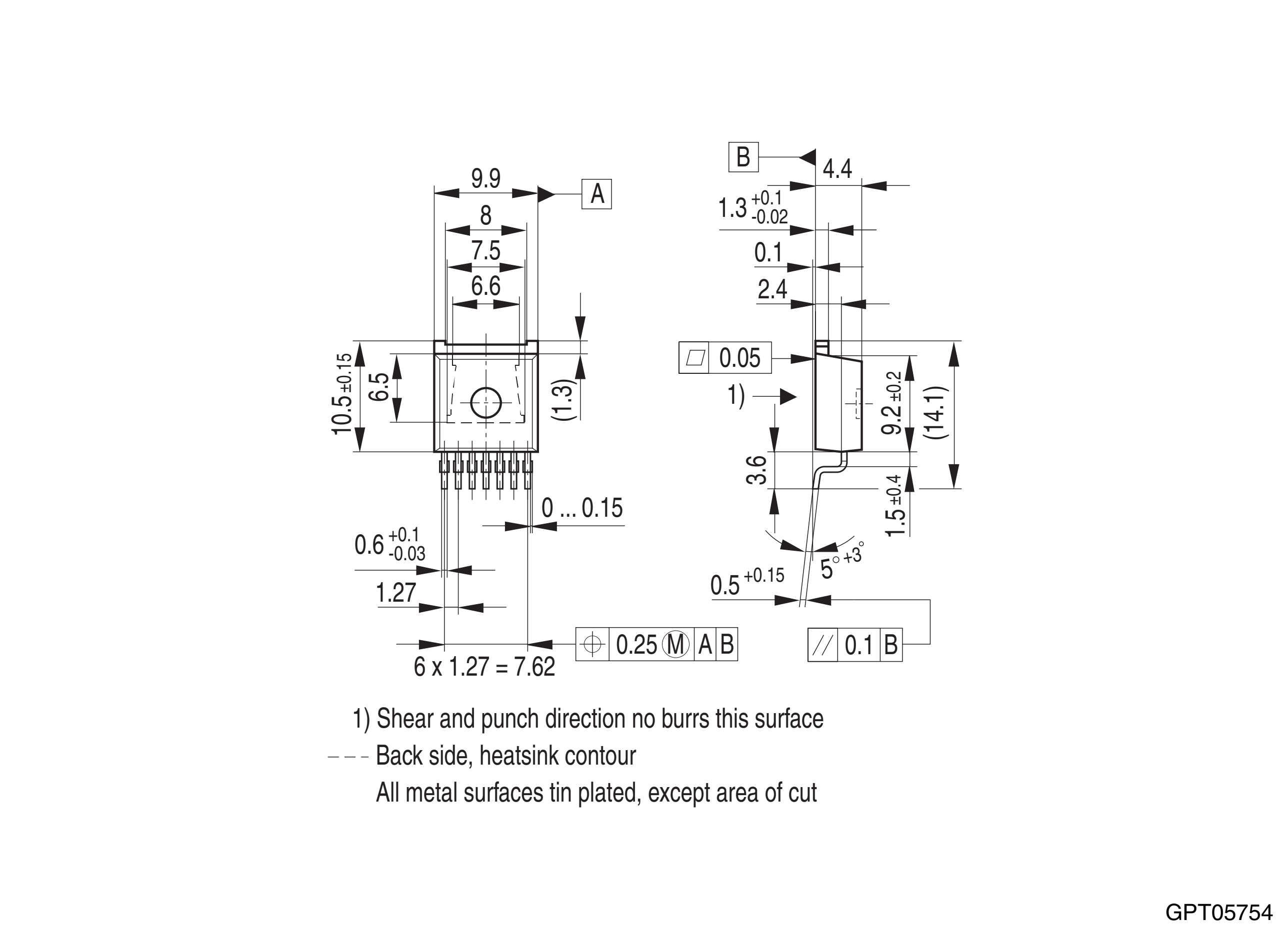

Figure 10 **P-TO220-7-180** (Plastic Transistor Single Outline)

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Dimensions in mm

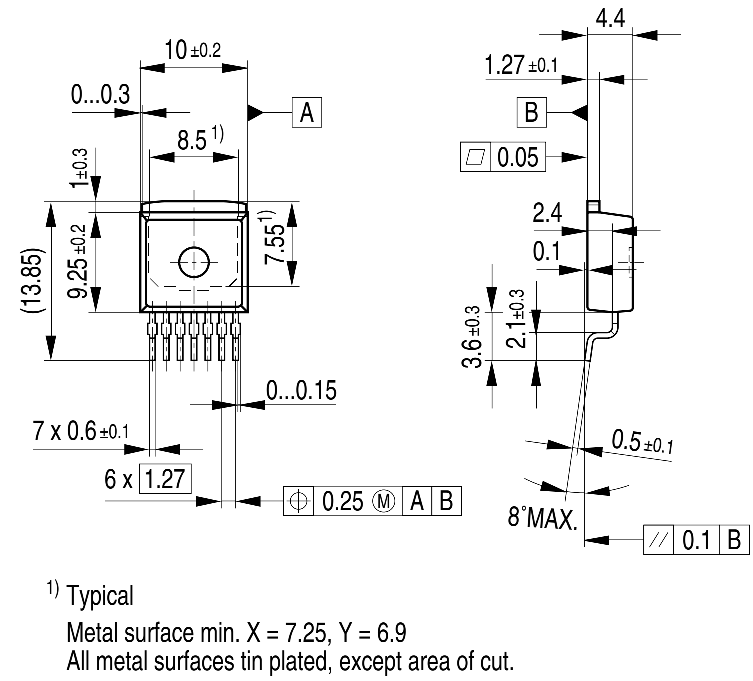

Figure 11 **P-TO220-7-4** (Plastic Transistor Single Outline)

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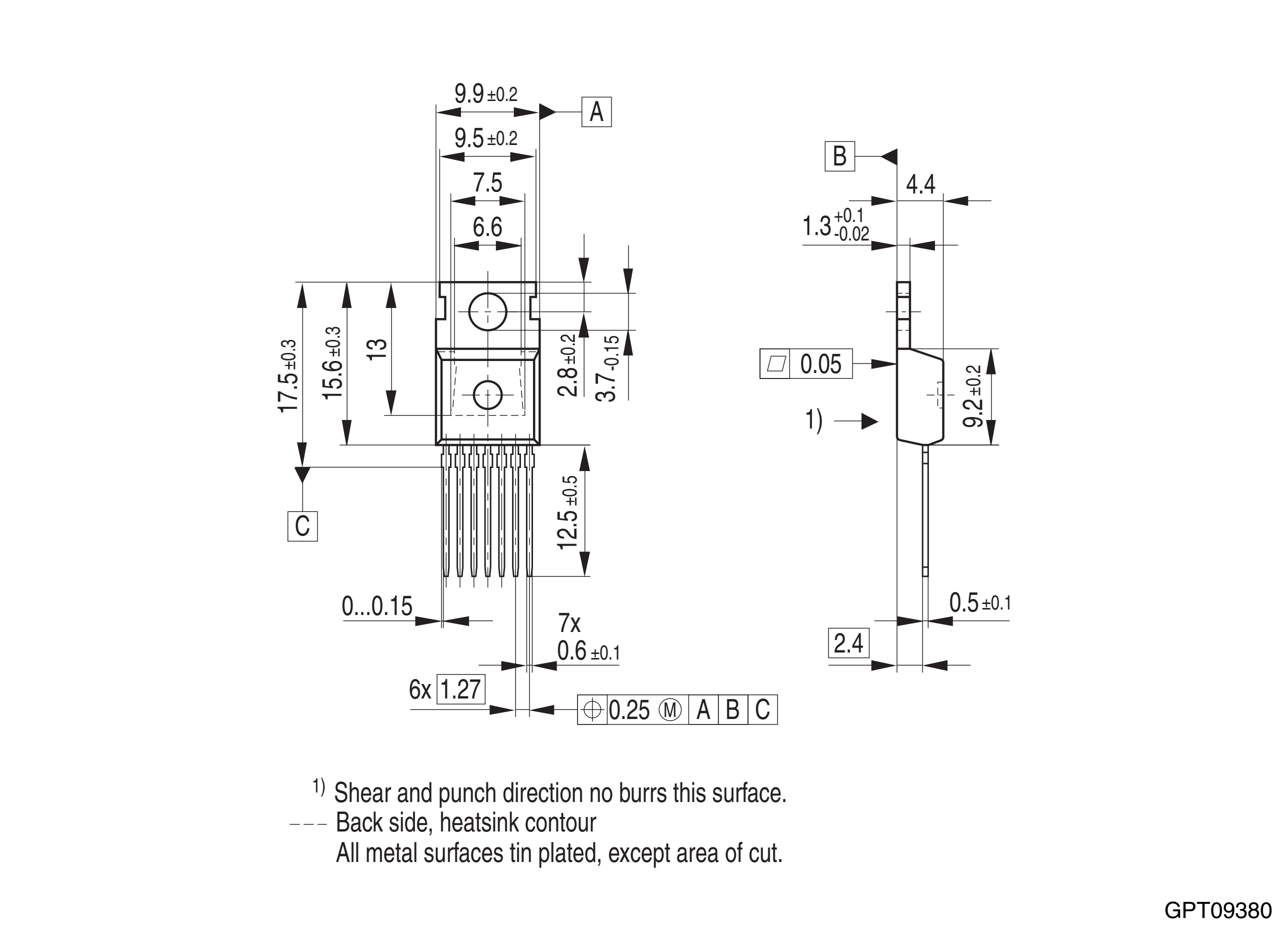

Figure 12 **P-TO220-7-230** (Plastic Transistor Single Outline)

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Dimensions in mm

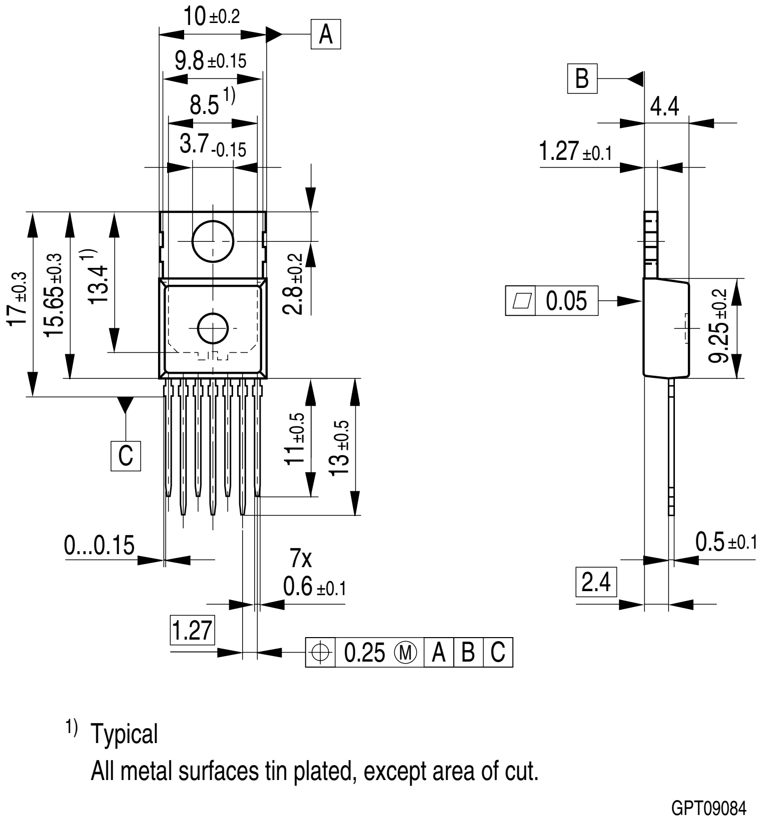

Figure 13 **P-TO220-7-12** (Plastic Transistor Single Outline)

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Dimensions in mm

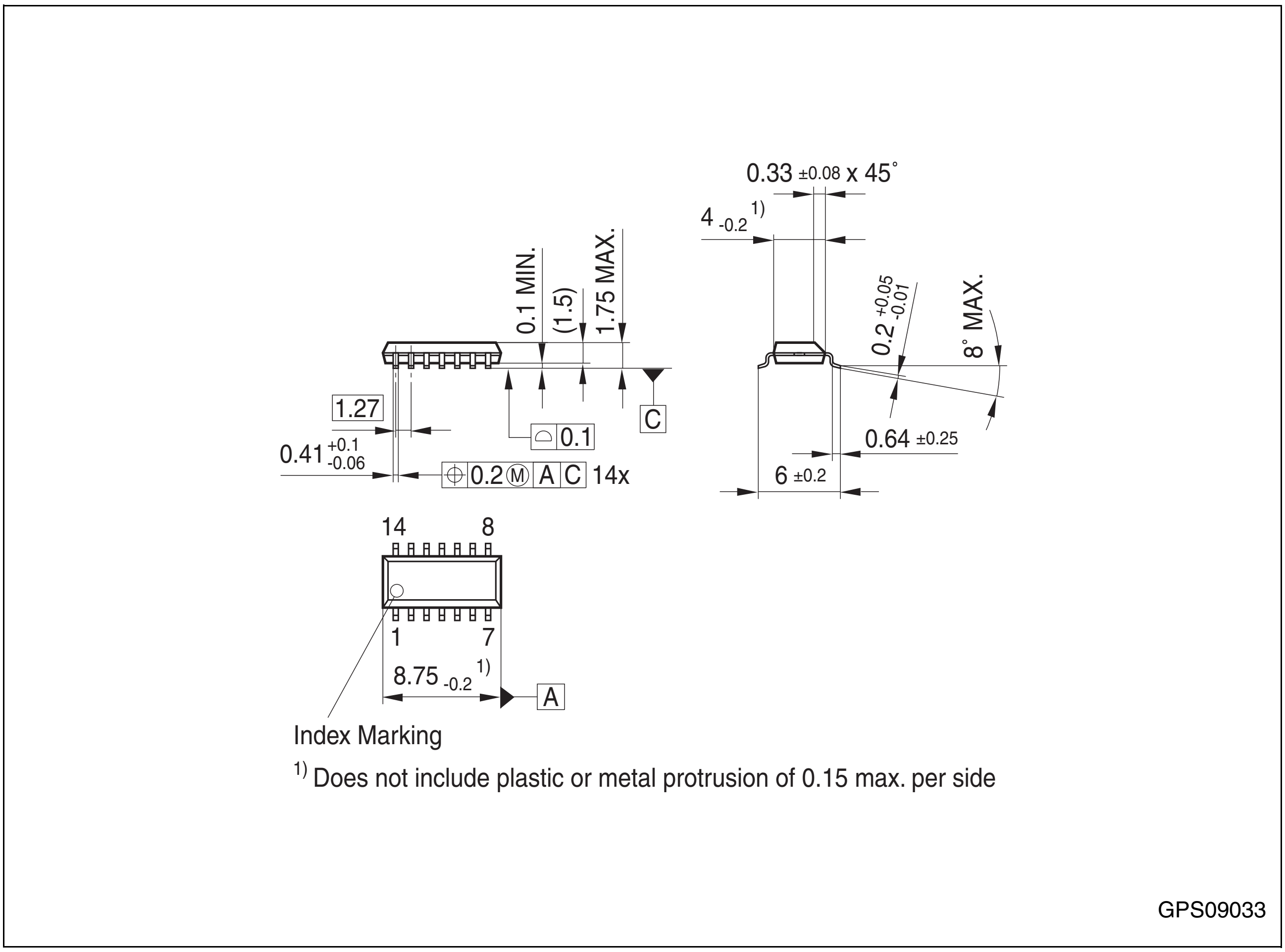

Figure 14 **P-DSO-14-8** (Plastic Dual Small Outline)

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SMD = Surface Mounted Device

Dimensions in mm

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