DUAL PROCESSOR SUPERVISORS

FEATURES

- **Dual Supervisory Circuits for DSP- and Processor-Based Systems**
- **Power-On Reset Generator with Fixed Delay Time of 200ms; no External Capacitor Needed**
- **Watchdog Timer Retriggers the $\overline{\text{RESET}}$ Output at SENSEn ≥ V_{IT+}**
- **Temperature-Compensated Voltage Reference**
- **Maximum Supply Current of 40μA**
- **Supply Voltage Range: 2.7V to 6V**
- **Defined $\overline{\text{RESET}}$ Output From V_{DD} ≥ 1.1V**
- **MSOP-8 and SO-8 Packages**
- **Temperature Range: –40°C to +85°C**

APPLICATIONS

- **Processor Supply Monitoring**
- **Industrial Equipment**
- **Automotive Systems**
- **Portable/Battery-Powered Equipment**
- **Wireless Communication Systems**
- **Notebook/Desktop Computers**

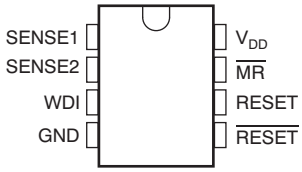
DESCRIPTION

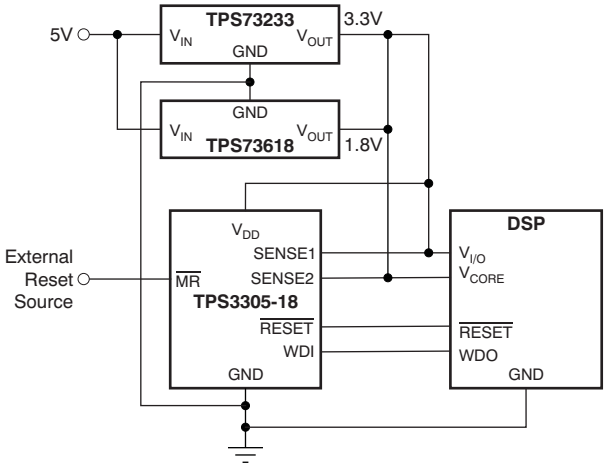
The TPS3305 family is a series of micropower supply voltage supervisors designed for circuit initialization. Its dual monitor topology is well-suited to use in DSP and processor-based systems, which often require two supply voltages, core and I/O.

$\overline{\text{RESET}}$ is asserted when the voltage at either SENSEn pin falls below its threshold voltage, V_{IT}. When both SENSEn pins are again above their respective threshold voltages, $\overline{\text{RESET}}$ is held low for the factory-programmed delay time (200ms typ). $\overline{\text{RESET}}$ is also asserted if the watchdog input (WDI) is not toggled for more than 1.6s typ.

The TPS3305-xx devices are available in either 8-pin MSOP or SO packages, and are specified for operation over a temperature range of –40°C to +85°C.

D OR DGN PACKAGE
(TOP VIEW)





This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

DEVICE	NOMINAL SUPERVISED VOLTAGE		THRESHOLD VOLTAGE (TYP)	
	SENSE1	SENSE2	SENSE1	SENSE2
TPS3305-18	3.3 V	1.8 V	2.93 V	1.68 V
TPS3305-25	3.3 V	2.5 V	2.93 V	2.25 V
TPS3305-33	5.0 V	3.3 V	4.55 V	2.93 V

(1) For the most current specifications and package information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Over operating junction temperature range (unless otherwise noted).

	UNIT
Supply voltage range, V_{DD}	–0.3V to +7V
$V_{\overline{MR}}$, V_{WDI}	–0.3V to V_{DD} + 0.3V
Input voltage at SENSE1 and SENSE2, V_I	(V_{DD} + 0.3)V_{IT} / 1.25V
V_{RESET}, $V_{\overline{RESET}}$	–0.3V to +7V
Maximum low output current, I_{OL}	5mA
Maximum high output current, I_{OH}	–5mA
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD})	±20mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD})	±20mA
Continuous total power dissipation	See Dissipation Ratings Table
Operating junction temperature range, T_J	–40°C to +85°C
Storage temperature range, T_{stg}	–65°C to +150°C
Soldering temperature	+260°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.

DISSIPATION RATINGS TABLE

PACKAGE	T_A ≤ +25°C POWER RATING	DERATING FACTOR ABOVE T_A = +25°C	T_A = +70°C POWER RATING	T_A = +85°C POWER RATING
DGN	2.14W	17.1mW/°C	1.37W	1.11W
D	725mW	5.8mW/°C	464mW	377mW

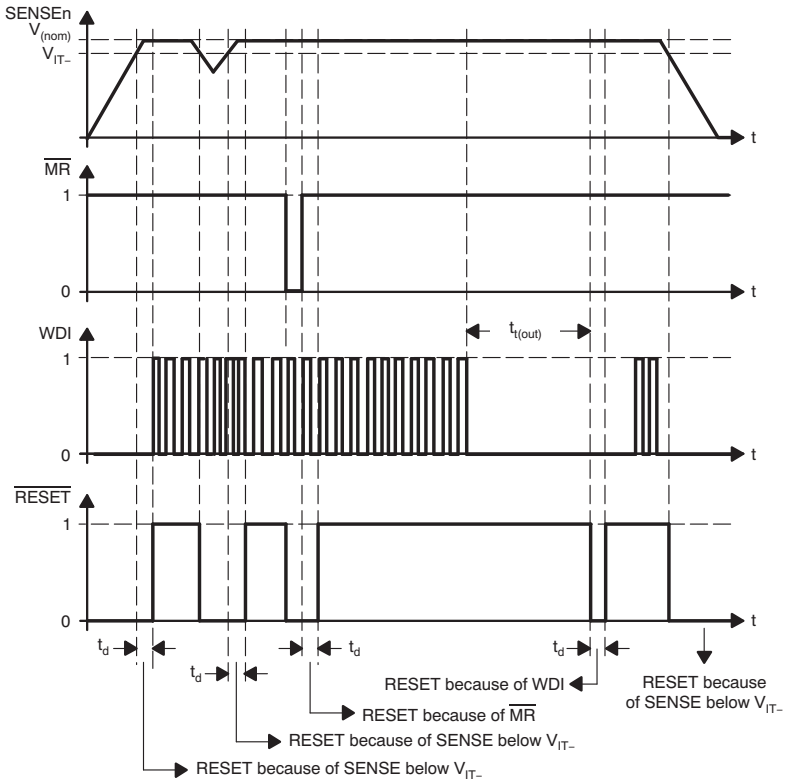
ELECTRICAL CHARACTERISTICS

Over operating junction temperature range (unless otherwise noted).

PARAMETER			TEST CONDITIONS	TPS3305-xx MIN	TPS3305-xx TYP	TPS3305-xx MAX	UNIT
V_{DD}	Input supply range			2.7		6.0	V
T_J	Operating junction temperature range			–40		+85	°C
V_{OH}	High-level output voltage		V_{DD} = 2.7V to 6V, I_{OH} = –20µA	V_{DD} – 0.2V			V
			V_{DD} = 3.3V, I_{OH} = –2mA	V_{DD} – 0.4V			V
			V_{DD} = 6V, I_{OH} = –3mA	V_{DD} – 0.4V			V
V_{OL}	Low-level output voltage		V_{DD} = 2.7V to 6V, I_{OL} = 20µA			0.2	V
			V_{DD} = 3.3V, I_{OL} = 2mA			0.4	V
			V_{DD} = 6V, I_{OL} = 3mA			0.4	V
	Power-up reset voltage(1)		V_{DD} ≥ 1.1V, I_{OL} = 20µA			0.4	V
$V_{IT–}$	Negative-going input threshold voltage(2)	VSENSE1, VSENSE2	V_{DD} = 2.7V to 6V, T_A = 0°C to +85°C	1.64	1.68	1.72	V
				2.20	2.25	2.30	V
				2.86	2.93	3.0	V
				4.46	4.55	4.64	V
		VSENSE1, VSENSE2	V_{DD} = 2.7V to 6V, T_A = –40°C to +85°C	1.64	1.68	1.73	V
				2.20	2.25	2.32	V
				2.86	2.93	3.02	V
				4.46	4.55	4.67	V
V_{hys}	Hysteresis at VSENSEn input		$V_{IT–}$= 1.68V		15		mV
			$V_{IT–}$ = 2.25V		20		mV
			$V_{IT–}$ = 2.93V		30		mV
			$V_{IT–}$ = 4.55V		40		mV
$I_{H(AV)}$	Average high-level input current	WDI	WDI = V_{DD} = 6V Time average (dc = 88%)		100	150	µA
$I_{L(AV)}$	Average low-level input current	WDI	WDI = 0V, V_{DD} = 6V Time average (dc = 12%)		–15	–20	µA
V_{IH}	High-level input voltage at $\overline{MR}$ and WDI			0.7 x V_{DD}			V
V_{IL}	Low-level input voltage at $\overline{MR}$ and WDI					0.3 x V_{DD}	V
Δt / ΔV	Input transition rise and fall rate at $\overline{MR}$					50	ns/V
I_H	High-level input current	WDI	WDI = V_{DD} = 6V		120	170	µA
		$\overline{MR}$	$\overline{MR}$ = 0.7 × V_{DD}, V_{DD} = 6V		–130	–180	µA
		SENSE1	VSENSE1 = V_{DD} = 6V		5	8	µA
		SENSE2	VSENSE2 = V_{DD} = 6V		6	9	µA
I_L	Low-level input current	WDI	WDI = 0V, V_{DD} = 6V		–120	–170	µA
		$\overline{MR}$	$\overline{MR}$ = 0V, V_{DD} = 6V		–430	–600	µA
		SENSEn	VSENSE1,2 = 0V	–1		1	µA
I_{DD}	Supply current					40	µA
C_I	Input capacitance		V_I = 0V to V_{DD}		10	pF	

(1) The lowest supply voltage at which $\overline{RESET}$ becomes active. t_r, V_{DD} ≥15 µs/V.
(2) To ensure best stability of the threshold voltage, a bypass capacitor (0.1 µF ceramic) should be placed close to the supply terminals.

TIMING DIAGRAM



TIMING REQUIREMENTS

At V_{DD} = 2.7V to 6V, R_L = 1MΩ, C_L = 50pF, and T_J = +25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_w	Pulse width	SENSEn	$V_{SENSEnL} = V_{IT-} - 0.2V$, $V_{SENSEnH} = V_{IT+} + 0.2V$	6			µs
		$\overline{MR}$	$V_{IH} = 0.7 \times V_{DD}$, $V_{IL} = 0.3 \times V_{DD}$	100			ns
		WDI		100			ns

SWITCHING CHARACTERISTICS

At V_{DD} = 2.7V to 6V, R_L = 1MΩ, C_L = 50pF, and T_J = +25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{t(out)}$	Watchdog time-out		$V_{I(SENSEn)} \geq V_{IT+} + 0.2V$, $\overline{MR} \geq 0.7 \times V_{DD}$ See Timing Diagram	1.1	1.6	2.3	s
t_d	Delay time		$V_{I(SENSEn)} \geq V_{IT+} + 0.2V$, $\overline{MR} \geq 0.7 \times V_{DD}$ See Timing Diagram	140	200	280	ms
t_{PHL}	Propagation (delay) time, high-to-low level output	$\overline{MR}$ to $\overline{RESET}$, $\overline{MR}$ to RESET	$V_{I(SENSEn)} \geq V_{IT+} + 0.2V$, $V_{IH} = 0.7 \times V_{DD}$, $V_{IL} = 0.3 \times V_{DD}$		200	500	ns
t_{PLH}	Propagation (delay) time, low-to-high level output	$\overline{MR}$ to $\overline{RESET}$, $\overline{MR}$ to RESET	$V_{I(SENSEn)} \geq V_{IT+} + 0.2V$, $V_{IH} = 0.7 \times V_{DD}$, $V_{IL} = 0.3 \times V_{DD}$		200	500	ns
t_{PHL}	Propagation (delay) time, high-to-low level output	SENSEn to $\overline{RESET}$, SENSEn to RESET	$V_{IH} = V_{IT+} + 0.2V$, $V_{IL} = V_{IT-} - 0.2V$, $\overline{MR} \geq 0.7 \times V_{DD}$		1	5	µs
t_{PLH}	Propagation (delay) time, low-to-high level output	SENSEn to $\overline{RESET}$, SENSEn to RESET	$V_{IH} = V_{IT+} + 0.2V$, $V_{IL} = V_{IT-} - 0.2V$, $\overline{MR} \geq 0.7 \times V_{DD}$		1	5	µs

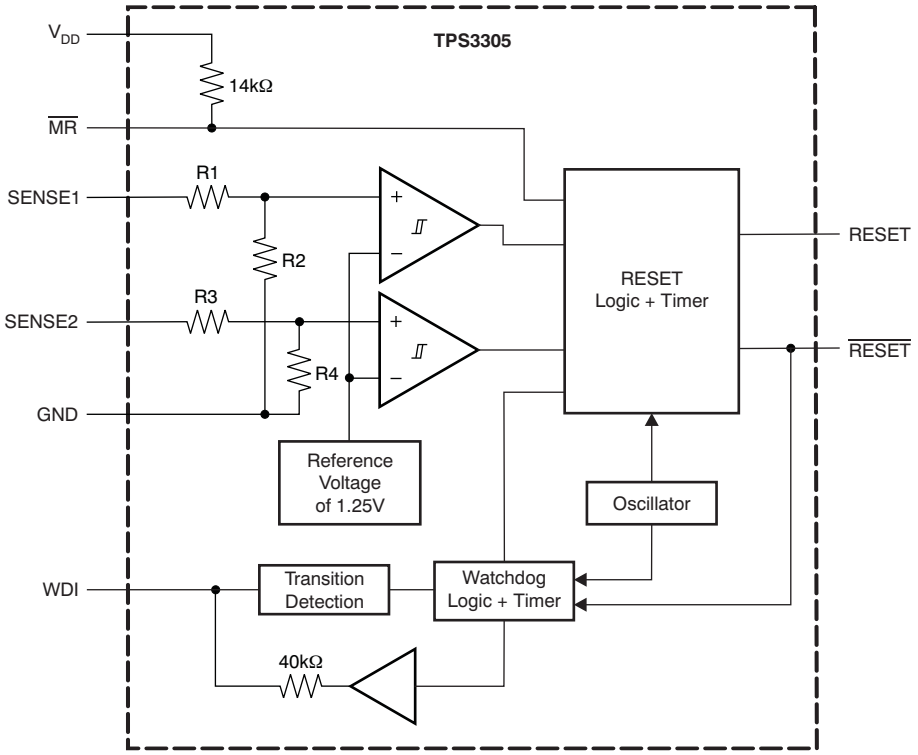
DEVICE INFORMATION

FUNCTION/TRUTH TABLE(1)

$\overline{MR}$	SENSE1 > V_{IT1}	SENSE2 > V_{IT2}	$\overline{RESET}$	RESET
L	X	X	L	H
H	0	0	L	H
H	0	1	L	H
H	1	0	L	H
H	1	1	H	L

(1) **X** = Don't care

FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
GND	4	Ground
$\overline{MR}$	7	Manual reset
$\overline{RESET}$	5	Active-low reset output
RESET	6	Active-high reset output
SENSE1	1	Sense voltage input 1
SENSE2	2	Sense voltage input 2
WDI	3	Watchdog timer input
V_{DD}	8	Supply voltage

TYPICAL CHARACTERISTICS

NORMALIZED SENSE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE AT V_{DD}

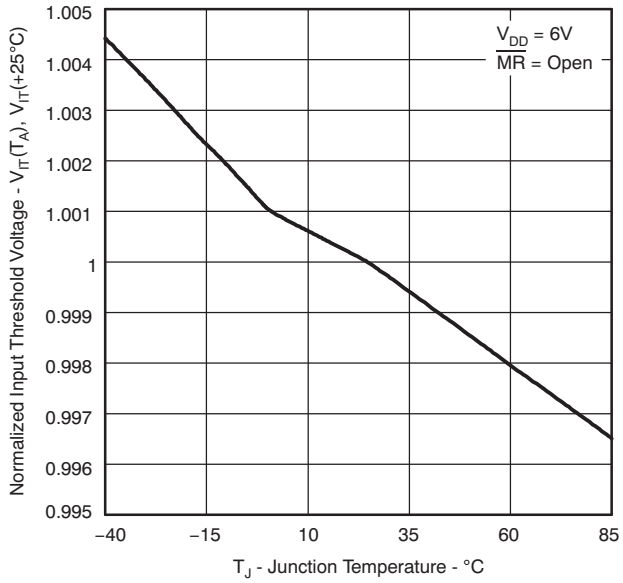


Figure 1.

SUPPLY CURRENT vs SUPPLY VOLTAGE

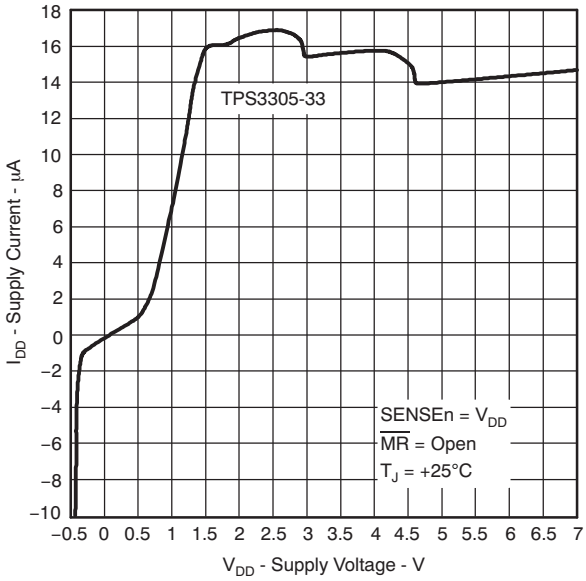


Figure 2.

INPUT CURRENT vs INPUT VOLTAGE AT $\overline{MR}$

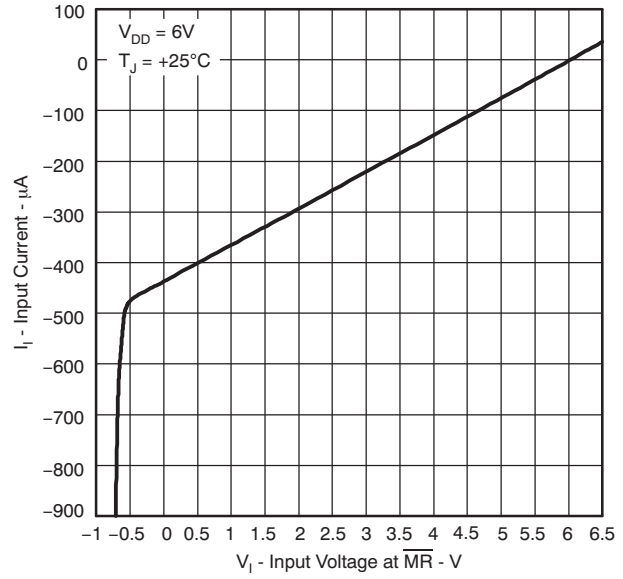


Figure 3.

MINIMUM PULSE DURATION AT SENSE vs THRESHOLD OVERDRIVE

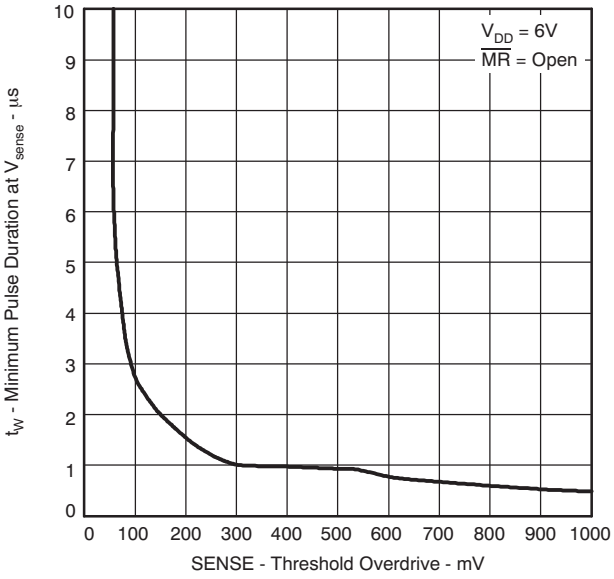


Figure 4.

TYPICAL CHARACTERISTICS (continued)

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

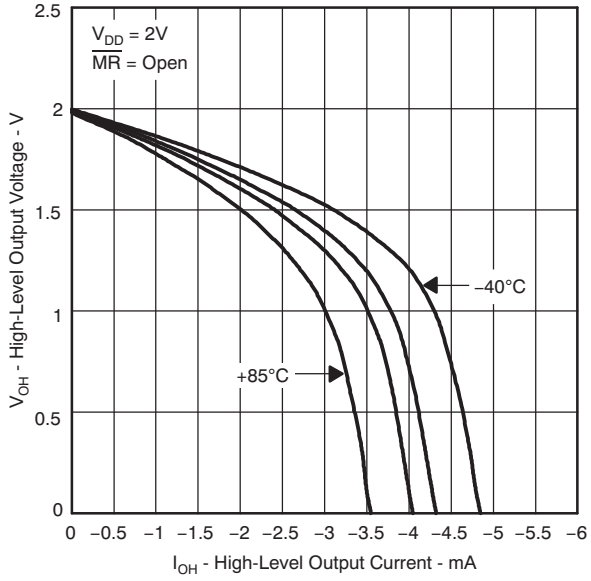


Figure 5.

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

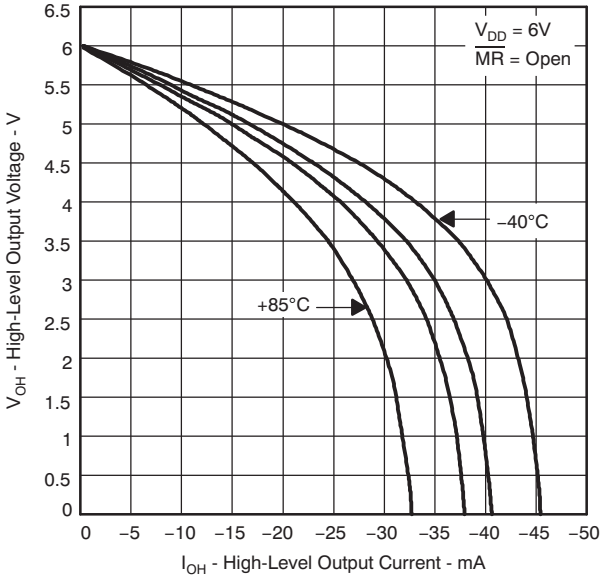


Figure 6.

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

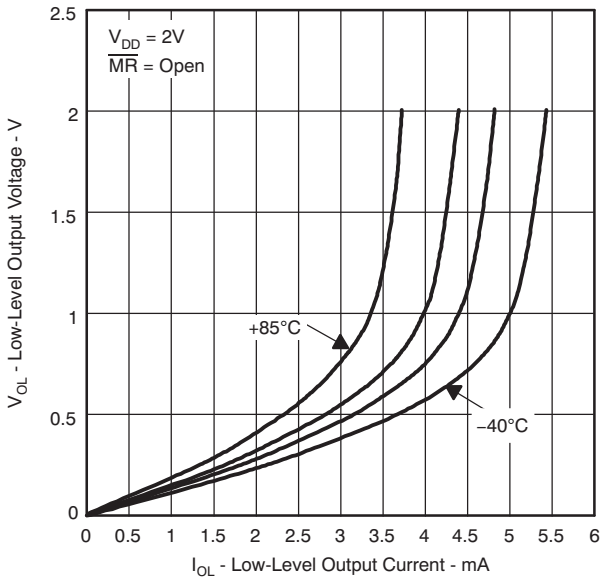


Figure 7.

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

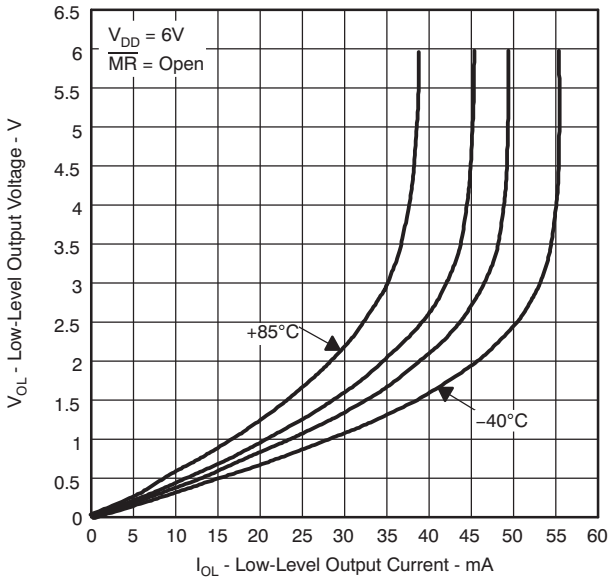


Figure 8.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS3305-18D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3305-18DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3305-18DGN	ACTIVE	MSOP-Power PAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3305-18DGNG4	ACTIVE	MSOP-Power PAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3305-18DGNR	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3305-18DGNRG4	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3305-18DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3305-18DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3305-25D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3305-25DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3305-25DGN	ACTIVE	MSOP-Power PAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3305-25DGNG4	ACTIVE	MSOP-Power PAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3305-25DGNR	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3305-25DGNRG4	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3305-25DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3305-25DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3305-33D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3305-33DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3305-33DGN	ACTIVE	MSOP-Power PAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3305-33DGNG4	ACTIVE	MSOP-Power PAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3305-33DGNR	ACTIVE	MSOP-	DGN	8	2500	Green (RoHS &	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
		Power PAD				no Sb/Br)		
TPS3305-33DGNRG4	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3305-33DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3305-33DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

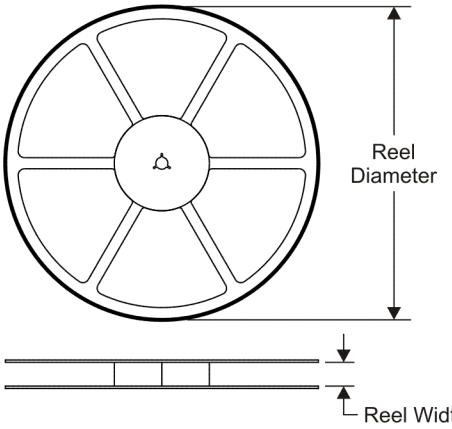
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

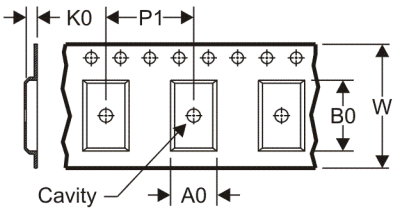
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

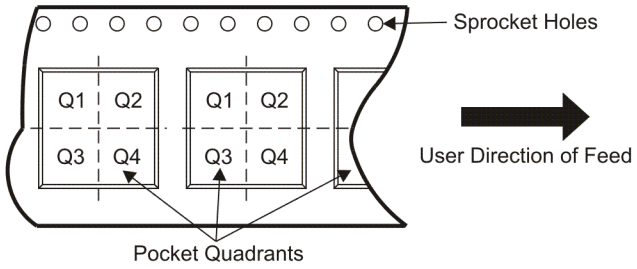


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

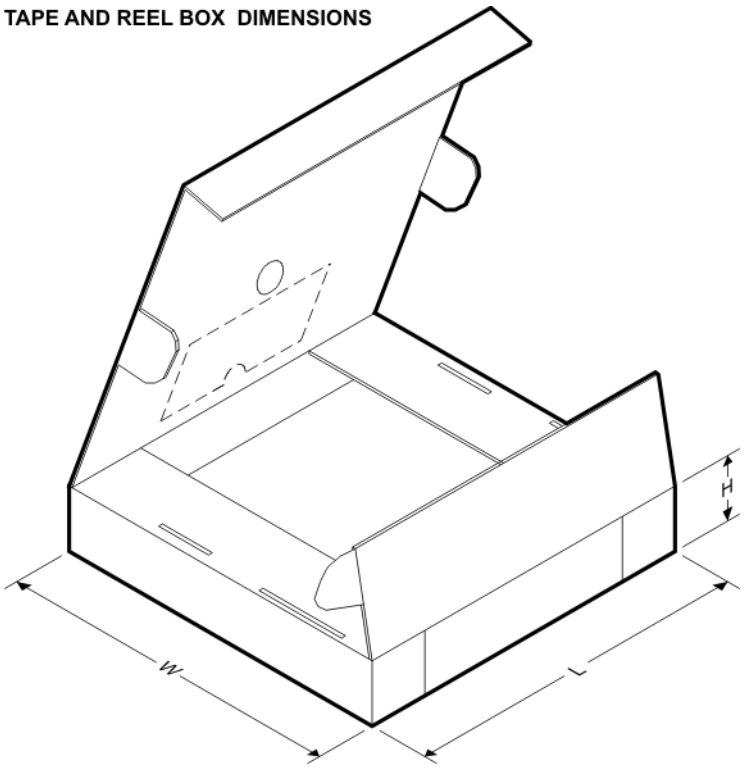
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3305-18DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS3305-18DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS3305-25DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS3305-25DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS3305-33DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS3305-33DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

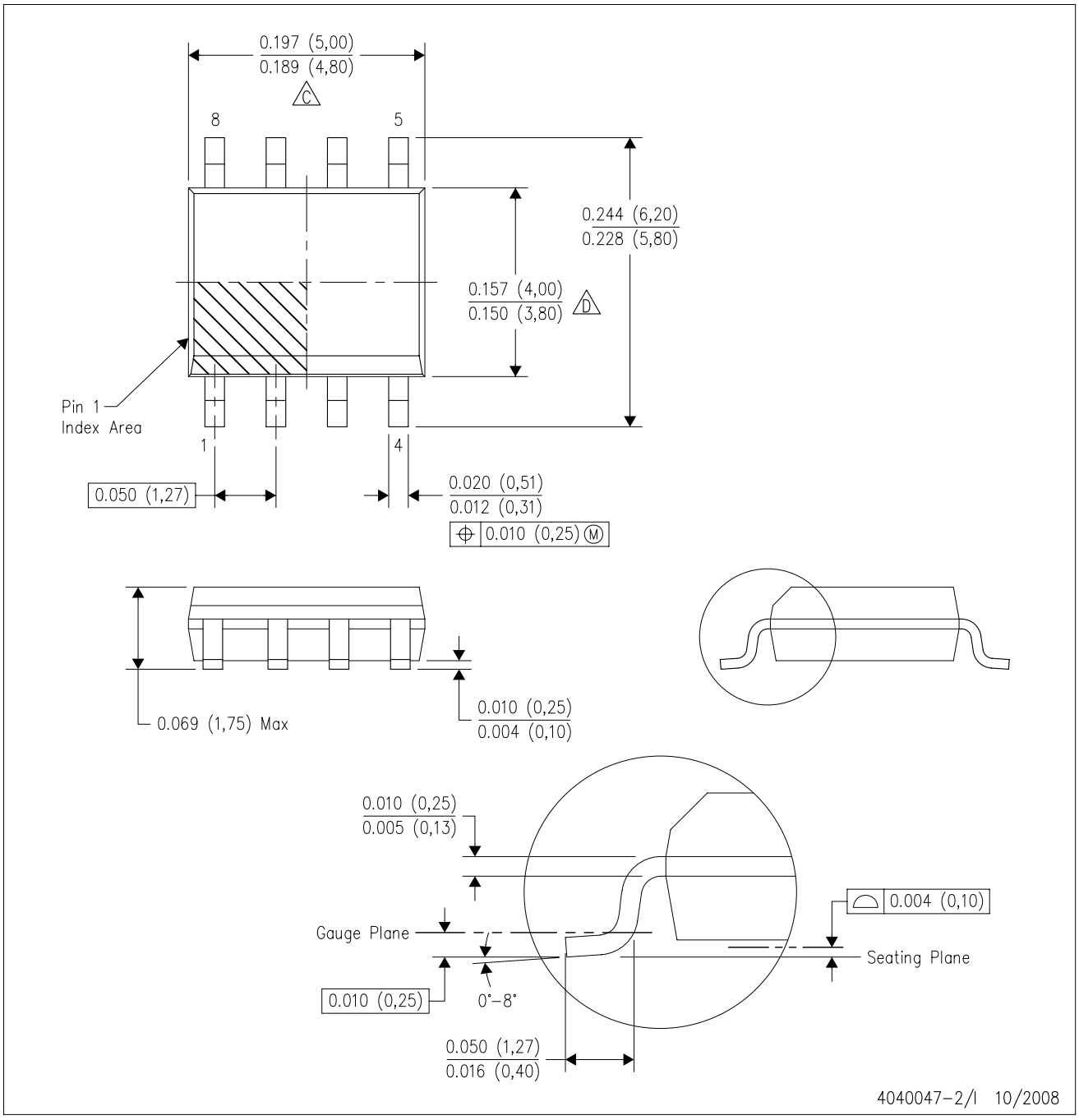
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

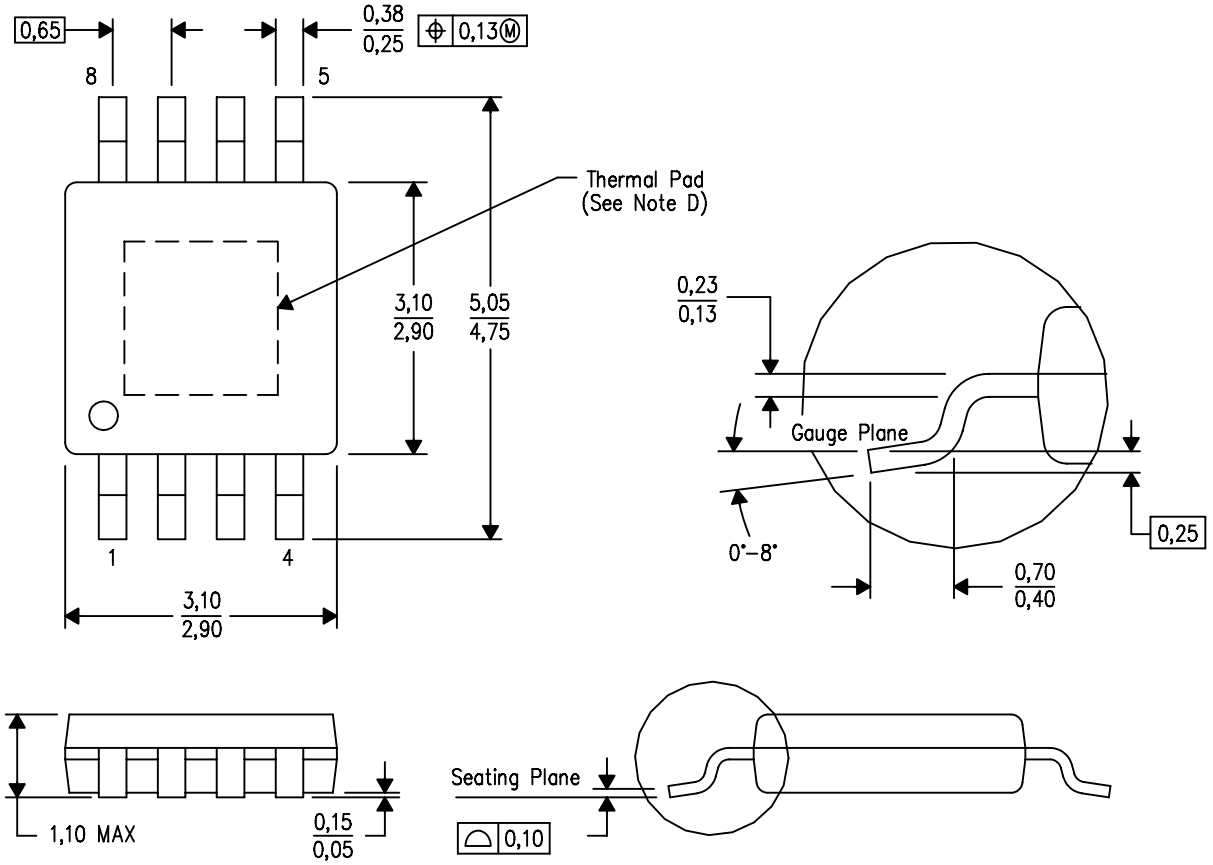
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3305-18DGNR	MSOP-PowerPAD	DGN	8	2500	358.0	335.0	35.0
TPS3305-18DR	SOIC	D	8	2500	346.0	346.0	29.0
TPS3305-25DGNR	MSOP-PowerPAD	DGN	8	2500	358.0	335.0	35.0
TPS3305-25DR	SOIC	D	8	2500	346.0	346.0	29.0
TPS3305-33DGNR	MSOP-PowerPAD	DGN	8	2500	358.0	335.0	35.0
TPS3305-33DR	SOIC	D	8	2500	346.0	346.0	29.0

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MO–187 variation AA–T

THERMAL PAD MECHANICAL DATA

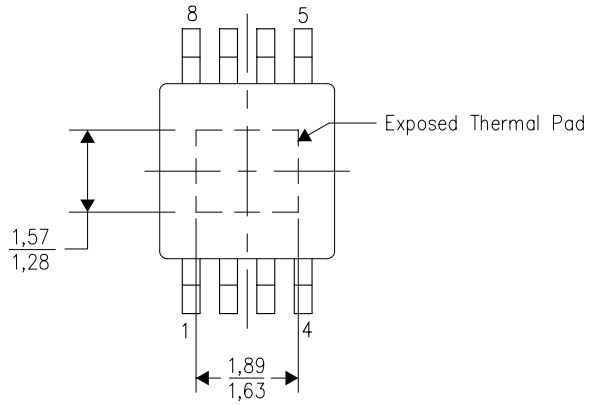
DGN (S–PDSO–G8)

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

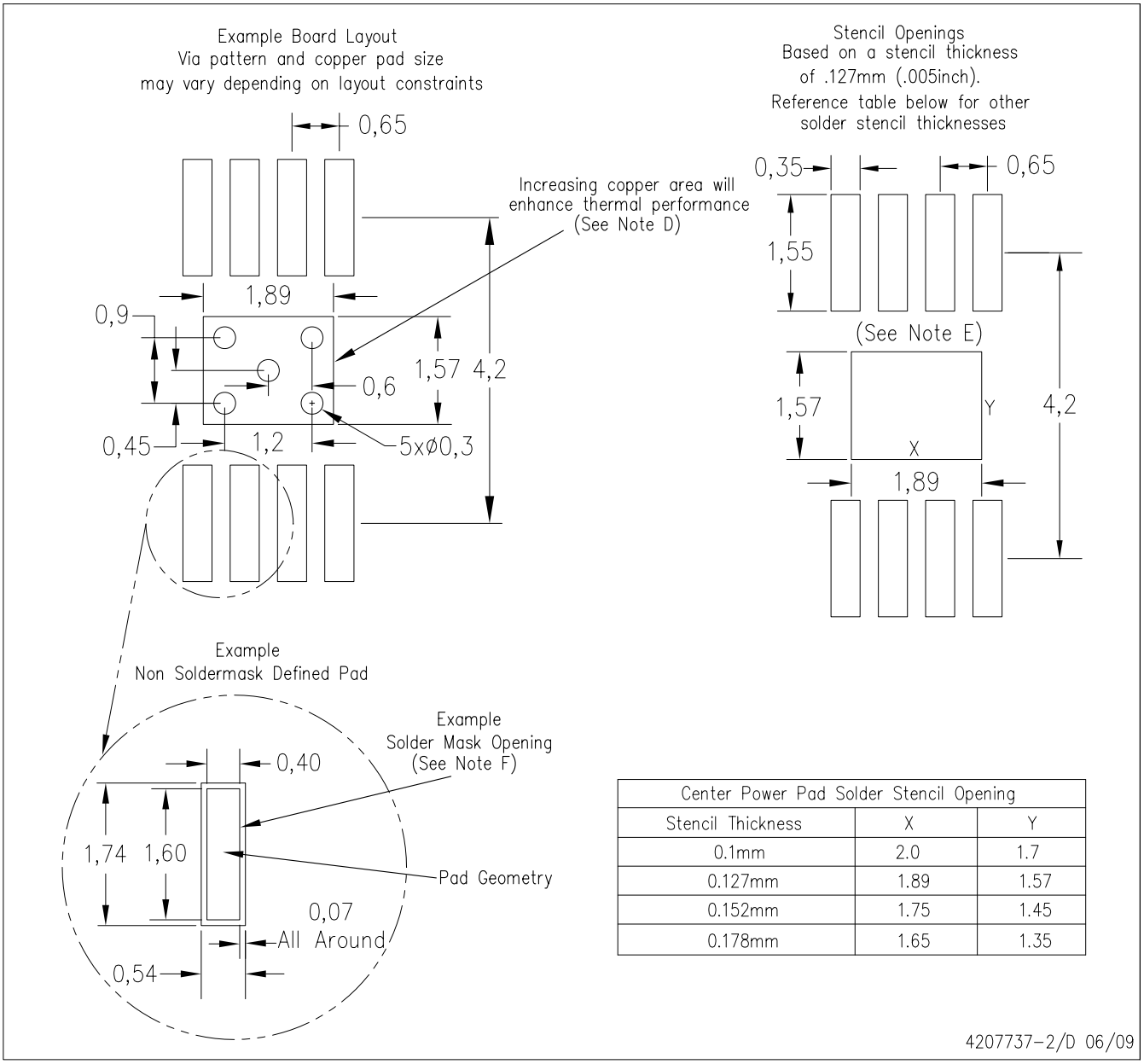


Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DGN (R–PDSO–G8) PowerPAD™



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.0	1.7
0.127mm	1.89	1.57
0.152mm	1.75	1.45
0.178mm	1.65	1.35

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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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