

### FEATURES

#### Low power operation

##### 5 V operation

1.2 mA per channel max @ 0 Mbps to 2 Mbps

3.5 mA per channel max @ 10 Mbps

32 mA per channel max @ 90 Mbps

##### 3 V operation

0.8 mA per channel max @ 0 Mbps to 2 Mbps

2.2 mA per channel max @ 10 Mbps

20 mA per channel max @ 90 Mbps

#### Bidirectional communication

#### 3 V/5 V level translation

#### High temperature operation: 105°C

#### High data rate: dc to 90 Mbps (NRZ)

#### Precise timing characteristics

2 ns max pulse width distortion

2 ns max channel-to-channel matching

#### High common-mode transient immunity: >25 kV/μs

#### Output enable function

#### 16-lead SOIC wide body package, Pb-free models available

#### Safety and regulatory approvals

UL recognition: 2500 V rms for 1 minute per UL 1577

CSA component acceptance notice #5A

VDE certificate of conformity

DIN EN 60747-5-2 (VDE 0884 Part 2): 2003-01

DIN EN 60950 (VDE 0805): 2001-12; EN 60950:2000

$V_{IORM} = 560$  V peak

TÜV approval: IEC/EN/UL/CSA 61010-1

### APPLICATIONS

#### General-purpose multichannel isolation

#### SPI® interface/data converter isolation

#### RS-232/RS-422/RS-485 transceiver

#### Industrial field bus isolation

### GENERAL DESCRIPTION

The ADuM130x<sup>1</sup> are 3-channel digital isolators based on Analog Devices' *iCoupler*® technology. Combining high speed CMOS and monolithic transformer technology, these isolation components provide outstanding performance characteristics superior to alternatives such as optocoupler devices.

By avoiding the use of LEDs and photodiodes, *iCoupler* devices remove the design difficulties commonly associated with optocouplers. The typical optocoupler concerns regarding uncertain current transfer ratios, nonlinear transfer functions, and temperature and lifetime effects are eliminated with the simple *iCoupler* digital interfaces and stable performance characteristics. The need for external drivers and other discrete components is eliminated with these *iCoupler* products. Furthermore, *iCoupler* devices consume one-tenth to one-sixth the power of optocouplers at comparable signal data rates.

The ADuM130x isolators provide three independent isolation channels in a variety of channel configurations and data rates (see the Ordering Guide). Both models operate with the supply voltage on either side ranging from 2.7 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling a voltage translation functionality across the isolation barrier. In addition, the ADuM130x provides low pulse width distortion (<2 ns for CRW grade) and tight channel-to-channel matching (<2 ns for CRW grade). Unlike other optocoupler alternatives, the ADuM130x isolators have a patented refresh feature that ensures dc correctness in the absence of input logic transitions and during power-up/power-down conditions.

<sup>1</sup> Protected by U.S. Patents 5,952,849 and 6,873,065. Other patents pending.

### FUNCTIONAL BLOCK DIAGRAMS

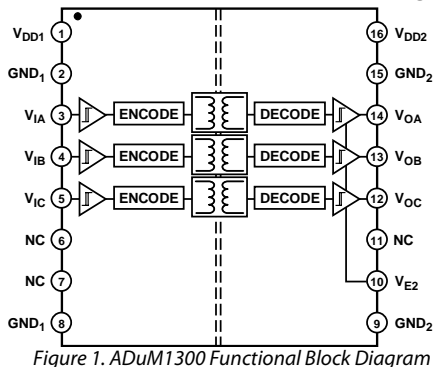


Figure 1. ADuM1300 Functional Block Diagram

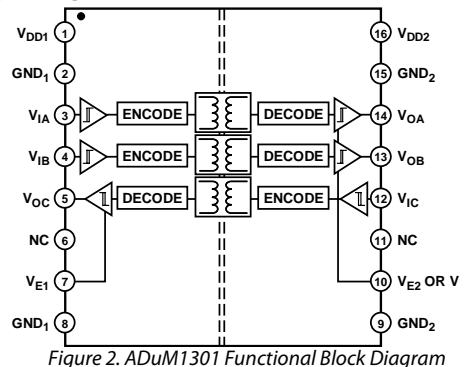


Figure 2. ADuM1301 Functional Block Diagram

#### Rev. E

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## REVISION HISTORY

### 2/06—Rev. D to Rev. E

Updated Format .....	Universal
Added TÜV Approval.....	Universal
Changes to Figure 2.....	1

### 5/05—Rev. C to Rev. D

Changes to Format .....	Universal
Changes to Figure 2.....	1
Changes to Table 6.....	10
Changes to Ordering Guide .....	18

### 6/04—Rev. B to Rev. C

Changes to Format .....	Universal
Changes to Features.....	1
Changes to Electrical Characteristics—5 V Operation .....	3
Changes to Electrical Characteristics—3 V Operation .....	5
Changes to Electrical Characteristics—Mixed 5 V/3 V or	

3 V/5 V Operation.....	7
Changes to Ordering Guide .....	18

### 5/04—Rev. A to Rev. B

Changes to the Format.....	Universal
Changes to the Features.....	1
Changes to Table 7 and Table 8 .....	14
Changes to Table 9.....	15
Changes to the DC Correctness and Magnetic Field Immunity	
Section.....	19
Changes to the Power Consumption Section .....	20
Changes to the Ordering Guide .....	21

### 9/03—Rev. 0 to Rev. A

Edits to Regulatory Information .....	13
Edits to Absolute Maximum Ratings.....	15
Deleted the Package Branding Information .....	16

## SPECIFICATIONS

### ELECTRICAL CHARACTERISTICS—5 V OPERATION<sup>1</sup>

4.5 V ≤ V<sub>DD1</sub> ≤ 5.5 V, 4.5 V ≤ V<sub>DD2</sub> ≤ 5.5 V; all min/max specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at T<sub>A</sub> = 25°C, V<sub>DD1</sub> = V<sub>DD2</sub> = 5 V.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
<b>DC SPECIFICATIONS</b>						
Input Supply Current per Channel, Quiescent	I <sub>DD1(Q)</sub>		0.50	0.53	mA	
Output Supply Current per Channel, Quiescent	I <sub>DDO(Q)</sub>		0.19	0.21	mA	
ADuM1300, Total Supply Current Three Channels <sup>2</sup>						
DC to 2 Mbps						
V <sub>DD1</sub> Supply Current	I <sub>DD1(Q)</sub>		1.6	2.5	mA	DC to 1 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	I <sub>DD2(Q)</sub>		0.7	1.0	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
V <sub>DD1</sub> Supply Current	I <sub>DD1(10)</sub>		6.5	8.1	mA	5 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	I <sub>DD2(10)</sub>		1.9	2.5	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)						
V <sub>DD1</sub> Supply Current	I <sub>DD1(90)</sub>		57	77	mA	45 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	I <sub>DD2(90)</sub>		16	18	mA	45 MHz logic signal freq.
ADuM1301, Total Supply Current, Three Channels <sup>2</sup>						
DC to 2 Mbps						
V <sub>DD1</sub> Supply Current	I <sub>DD1(Q)</sub>		1.3	2.1	mA	DC to 1 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	I <sub>DD2(Q)</sub>		1.0	1.4	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
V <sub>DD1</sub> Supply Current	I <sub>DD1(10)</sub>		5.0	6.2	mA	5 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	I <sub>DD2(10)</sub>		3.4	4.2	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)						
V <sub>DD1</sub> Supply Current	I <sub>DD1(90)</sub>		43	57	mA	45 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	I <sub>DD2(90)</sub>		29	37	mA	45 MHz logic signal freq.
For All Models						
Input Currents	I <sub>IA</sub> , I <sub>IB</sub> , I <sub>IC</sub> , I <sub>E1</sub> , I <sub>E2</sub>	-10	+0.01	+10	μA	0 ≤ V <sub>IA</sub> , V <sub>IB</sub> , V <sub>IC</sub> ≤ V <sub>DD1</sub> or V <sub>DD2</sub> , 0 ≤ V <sub>E1</sub> , V <sub>E2</sub> ≤ V <sub>DD1</sub> or V <sub>DD2</sub>
Logic High Input Threshold	V <sub>IH</sub> , V <sub>EH</sub>	2.0			V	
Logic Low Input Threshold	V <sub>IL</sub> , V <sub>EL</sub>			0.8	V	
Logic High Output Voltages	V <sub>OAH</sub> , V <sub>OBH</sub> , V <sub>OCH</sub>	V <sub>DD1</sub> , V <sub>DD2</sub> - 0.1	5.0		V	I <sub>Ox</sub> = -20 μA, V <sub>Ix</sub> = V <sub>IxH</sub>
		V <sub>DD1</sub> , V <sub>DD2</sub> - 0.4	4.8		V	I <sub>Ox</sub> = -4 mA, V <sub>Ix</sub> = V <sub>IxH</sub>
Logic Low Output Voltages	V <sub>OAL</sub> , V <sub>OBL</sub> , V <sub>OCL</sub>		0.0	0.1	V	I <sub>Ox</sub> = 20 μA, V <sub>Ix</sub> = V <sub>IxL</sub>
			0.04	0.1	V	I <sub>Ox</sub> = 400 μA, V <sub>Ix</sub> = V <sub>IxL</sub>
			0.2	0.4	V	I <sub>Ox</sub> = 4 mA, V <sub>Ix</sub> = V <sub>IxL</sub>
<b>SWITCHING SPECIFICATIONS</b>						
ADuM130xARW						
Minimum Pulse Width <sup>3</sup>	PW			1000	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Maximum Data Rate <sup>4</sup>		1			Mbps	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay <sup>5</sup>	t <sub>PHL</sub> , t <sub>PLH</sub>	50	65	100	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Pulse Width Distortion,  t <sub>PLH</sub> - t <sub>PHL</sub>   <sup>5</sup>	PWD			40	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay Skew <sup>6</sup>	t <sub>PSK</sub>			50	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Channel-to-Channel Matching <sup>7</sup>	t <sub>PSKCD/OD</sub>			50	ns	C <sub>L</sub> = 15 pF, CMOS signal levels

# ADuM1300/ADuM1301

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
ADuM130xBRW						
Minimum Pulse Width <sup>3</sup>	PW			100	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Maximum Data Rate <sup>4</sup>		10			Mbps	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay <sup>5</sup>	t <sub>PHL</sub> , t <sub>PLH</sub>	20	32	50	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Pulse Width Distortion,  t <sub>PLH</sub> – t <sub>PHL</sub>    <sup>5</sup>	PWD			3	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay Skew <sup>6</sup>	t <sub>PSK</sub>			15	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels <sup>7</sup>	t <sub>PSKCD</sub>			3	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels <sup>7</sup>	t <sub>PSKOD</sub>			6	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
ADuM130xCRW						
Minimum Pulse Width <sup>3</sup>	PW		8.3	11.1	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Maximum Data Rate <sup>4</sup>		90	120		Mbps	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay <sup>5</sup>	t <sub>PHL</sub> , t <sub>PLH</sub>	18	27	32	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Pulse Width Distortion,  t <sub>PLH</sub> – t <sub>PHL</sub>    <sup>5</sup>	PWD		0.5	2	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Change vs. Temperature			3		ps/°C	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay Skew <sup>6</sup>	t <sub>PSK</sub>			10	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels <sup>7</sup>	t <sub>PSKCD</sub>			2	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels <sup>7</sup>	t <sub>PSKOD</sub>			5	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
For All Models						
Output Disable Propagation Delay (High/Low to High Impedance)	t <sub>PHZ</sub> , t <sub>PLH</sub>		6	8	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Output Enable Propagation Delay (High Impedance to High/Low)	t <sub>PZH</sub> , t <sub>PZL</sub>		6	8	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t <sub>R</sub> /t <sub>F</sub>		2.5		ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output <sup>8</sup>	CM <sub>H</sub>	25	35		kV/μs	V <sub>ix</sub> = V <sub>DD1</sub> /V <sub>DD2</sub> , V <sub>CM</sub> = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output <sup>8</sup>	CM <sub>L</sub>	25	35		kV/μs	V <sub>ix</sub> = 0 V, V <sub>CM</sub> = 1000 V, transient magnitude = 800 V
Refresh Rate	f <sub>r</sub>		1.2		Mbps	
Input Dynamic Supply Current per Channel <sup>9</sup>	I <sub>DDI (D)</sub>		0.19		mA/Mbps	
Output Dynamic Supply Current per Channel <sup>9</sup>	I <sub>DDO (D)</sub>		0.05		mA/Mbps	

<sup>1</sup> All voltages are relative to their respective ground.

<sup>2</sup> The supply current values are for all three channels combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate may be calculated as described in the Power Consumption section. See Figure 6 through Figure 8 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 9 through Figure 12 for total V<sub>DD1</sub> and V<sub>DD2</sub> supply currents as a function of data rate for ADuM1300/ADuM1301 channel configurations.

<sup>3</sup> The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

<sup>4</sup> The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

<sup>5</sup> t<sub>PHL</sub> propagation delay is measured from the 50% level of the falling edge of the V<sub>ix</sub> signal to the 50% level of the falling edge of the V<sub>ox</sub> signal. t<sub>PLH</sub> propagation delay is measured from the 50% level of the rising edge of the V<sub>ix</sub> signal to the 50% level of the rising edge of the V<sub>ox</sub> signal.

<sup>6</sup> t<sub>PSK</sub> is the magnitude of the worst-case difference in t<sub>PHL</sub> or t<sub>PLH</sub> that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

<sup>7</sup> Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

<sup>8</sup> CM<sub>H</sub> is the maximum common-mode voltage slew rate that can be sustained while maintaining V<sub>o</sub> > 0.8 V<sub>DD2</sub>. CM<sub>L</sub> is the maximum common-mode voltage slew rate that can be sustained while maintaining V<sub>o</sub> < 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

<sup>9</sup> Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 6 through Figure 8 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

**ELECTRICAL CHARACTERISTICS—3 V OPERATION<sup>1</sup>**

2.7 V ≤ V<sub>DD1</sub> ≤ 3.6 V, 2.7 V ≤ V<sub>DD2</sub> ≤ 3.6 V; all min/max specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at T<sub>A</sub> = 25°C, V<sub>DD1</sub> = V<sub>DD2</sub> = 3.0 V.

**Table 2.**

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
<b>DC SPECIFICATIONS</b>						
Input Supply Current per Channel, Quiescent	I <sub>DD1 (Q)</sub>		0.26	0.31	mA	
Output Supply Current per Channel, Quiescent	I <sub>DDO (Q)</sub>		0.11	0.14	mA	
ADuM1300, Total Supply Current, Three Channels <sup>2</sup>						
DC to 2 Mbps						
V <sub>DD1</sub> Supply Current	I <sub>DD1 (Q)</sub>		0.9	1.7	mA	DC to 1 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	I <sub>DD2 (Q)</sub>		0.4	0.7	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
V <sub>DD1</sub> Supply Current	I <sub>DD1 (10)</sub>		3.4	4.9	mA	5 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	I <sub>DD2 (10)</sub>		1.1	1.6	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)						
V <sub>DD1</sub> Supply Current	I <sub>DD1 (90)</sub>		31	48	mA	45 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	I <sub>DD2 (90)</sub>		8	13	mA	45 MHz logic signal freq.
ADuM1301, Total Supply Current, Three Channels <sup>2</sup>						
DC to 2 Mbps						
V <sub>DD1</sub> Supply Current	I <sub>DD1 (Q)</sub>		0.7	1.4	mA	DC to 1 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	I <sub>DD2 (Q)</sub>		0.6	0.9	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
V <sub>DD1</sub> Supply Current	I <sub>DD1 (10)</sub>		2.6	3.7	mA	5 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	I <sub>DD2 (10)</sub>		1.8	2.5	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)						
V <sub>DD1</sub> Supply Current	I <sub>DD1 (90)</sub>		24	36	mA	45 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	I <sub>DD2 (90)</sub>		16	23	mA	45 MHz logic signal freq.
For All Models						
Input Currents	I <sub>IA</sub> , I <sub>IB</sub> , I <sub>IC</sub> , I <sub>E1</sub> , I <sub>E2</sub>	-10	+0.01	+10	μA	0 ≤ V <sub>IA</sub> , V <sub>IB</sub> , V <sub>IC</sub> ≤ V <sub>DD1</sub> or V <sub>DD2</sub> , 0 ≤ V <sub>E1</sub> , V <sub>E2</sub> ≤ V <sub>DD1</sub> or V <sub>DD2</sub>
Logic High Input Threshold	V <sub>IH</sub> , V <sub>EH</sub>	1.6			V	
Logic Low Input Threshold	V <sub>IL</sub> , V <sub>EL</sub>			0.4	V	
Logic High Output Voltages	V <sub>OAH</sub> , V <sub>OBH</sub> , V <sub>OCH</sub>	V <sub>DD1</sub> , V <sub>DD2</sub> - 0.1	3.0		V	I <sub>Ox</sub> = -20 μA, V <sub>Ix</sub> = V <sub>IxH</sub>
		V <sub>DD1</sub> , V <sub>DD2</sub> - 0.4	2.8		V	I <sub>Ox</sub> = -4 mA, V <sub>Ix</sub> = V <sub>IxH</sub>
Logic Low Output Voltages	V <sub>OAL</sub> , V <sub>OBL</sub> , V <sub>OCL</sub>		0.0	0.1	V	I <sub>Ox</sub> = 20 μA, V <sub>Ix</sub> = V <sub>IxL</sub>
			0.04	0.1	V	I <sub>Ox</sub> = 400 μA, V <sub>Ix</sub> = V <sub>IxL</sub>
			0.2	0.4	V	I <sub>Ox</sub> = 4 mA, V <sub>Ix</sub> = V <sub>IxL</sub>
<b>SWITCHING SPECIFICATIONS</b>						
ADuM130xARW						
Minimum Pulse Width <sup>3</sup>	PW			1000	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Maximum Data Rate <sup>4</sup>		1			Mbps	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay <sup>5</sup>	t <sub>PHL</sub> , t <sub>PLH</sub>	50	75	100	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Pulse Width Distortion,  t <sub>PLH</sub> - t <sub>PHL</sub>   <sup>5</sup>	PWD			40	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay Skew <sup>6</sup>	t <sub>PSK</sub>			50	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Channel-to-Channel Matching <sup>7</sup>	t <sub>PSKCD/OD</sub>			50	ns	C <sub>L</sub> = 15 pF, CMOS signal levels

# ADuM1300/ADuM1301

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
<b>ADuM130xBRW</b>						
Minimum Pulse Width <sup>3</sup>	PW			100	ns	$C_L = 15$ pF, CMOS signal levels
Maximum Data Rate <sup>4</sup>		10			Mbps	$C_L = 15$ pF, CMOS signal levels
Propagation Delay <sup>5</sup>	$t_{PHL}, t_{PLH}$	20	38	50	ns	$C_L = 15$ pF, CMOS signal levels
Pulse Width Distortion, $ t_{PLH} - t_{PHL} $ <sup>5</sup>	PWD			3	ns	$C_L = 15$ pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	$C_L = 15$ pF, CMOS signal levels
Propagation Delay Skew <sup>6</sup>	$t_{PSK}$			26	ns	$C_L = 15$ pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels <sup>7</sup>	$t_{PSKCD}$			3	ns	$C_L = 15$ pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels <sup>7</sup>	$t_{PSKOD}$			6	ns	$C_L = 15$ pF, CMOS signal levels
<b>ADuM130xCRW</b>						
Minimum Pulse Width <sup>3</sup>	PW		8.3	11.1	ns	$C_L = 15$ pF, CMOS signal levels
Maximum Data Rate <sup>4</sup>		90	120		Mbps	$C_L = 15$ pF, CMOS signal levels
Propagation Delay <sup>5</sup>	$t_{PHL}, t_{PLH}$	20	34	45	ns	$C_L = 15$ pF, CMOS signal levels
Pulse Width Distortion, $ t_{PLH} - t_{PHL} $ <sup>5</sup>	PWD		0.5	2	ns	$C_L = 15$ pF, CMOS signal levels
Change vs. Temperature			3		ps/°C	$C_L = 15$ pF, CMOS signal levels
Propagation Delay Skew <sup>6</sup>	$t_{PSK}$			16	ns	$C_L = 15$ pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels <sup>7</sup>	$t_{PSKCD}$			2	ns	$C_L = 15$ pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels <sup>7</sup>	$t_{PSKOD}$			5	ns	$C_L = 15$ pF, CMOS signal levels
<b>For All Models</b>						
Output Disable Propagation Delay (High/Low to High Impedance)	$t_{PHZ}, t_{PLH}$		6	8	ns	$C_L = 15$ pF, CMOS signal levels
Output Enable Propagation Delay (High Impedance to High/Low)	$t_{PZH}, t_{PZL}$		6	8	ns	$C_L = 15$ pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	$t_R/t_F$		3		ns	$C_L = 15$ pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output <sup>8</sup>	$ CM_H $	25	35		kV/μs	$V_{ix} = V_{DD1}/V_{DD2}, V_{CM} = 1000$ V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output <sup>8</sup>	$ CM_L $	25	35		kV/μs	$V_{ix} = 0$ V, $V_{CM} = 1000$ V, transient magnitude = 800 V
Refresh Rate	$f_r$		1.1		Mbps	
Input Dynamic Supply Current, per Channel <sup>9</sup>	$I_{DDI(D)}$		0.10		mA/Mbps	
Output Dynamic Supply Current, per Channel <sup>9</sup>	$I_{DDO(D)}$		0.03		mA/Mbps	

<sup>1</sup> All voltages are relative to their respective ground.

<sup>2</sup> The supply current values are for all three channels combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate may be calculated as described in the Power Consumption section. See Figure 6 through Figure 8 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 9 through Figure 12 for total  $V_{DD1}$  and  $V_{DD2}$  supply currents as a function of data rate for ADuM1300/ADuM1301 channel configurations.

<sup>3</sup> The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

<sup>4</sup> The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

<sup>5</sup>  $t_{PHL}$  propagation delay is measured from the 50% level of the falling edge of the  $V_{ix}$  signal to the 50% level of the falling edge of the  $V_{ox}$  signal.  $t_{PLH}$  propagation delay is measured from the 50% level of the rising edge of the  $V_{ix}$  signal to the 50% level of the rising edge of the  $V_{ox}$  signal.

<sup>6</sup>  $t_{PSK}$  is the magnitude of the worst-case difference in  $t_{PHL}$  or  $t_{PLH}$  that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

<sup>7</sup> Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

<sup>8</sup>  $CM_H$  is the maximum common-mode voltage slew rate that can be sustained while maintaining  $V_o > 0.8 V_{DD2}$ .  $CM_L$  is the maximum common-mode voltage slew rate that can be sustained while maintaining  $V_o < 0.8$  V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

<sup>9</sup> Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 6 through Figure 8 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

**ELECTRICAL CHARACTERISTICS—MIXED 5 V/3 V OR 3 V/5 V OPERATION<sup>1</sup>**

5 V/3 V operation:  $4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$ ,  $2.7\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$ ; 3 V/5 V operation:  $2.7\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$ ,  $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$ ; all min/max specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at  $T_A = 25^\circ\text{C}$ ;  $V_{DD1} = 3.0\text{ V}$ ,  $V_{DD2} = 5\text{ V}$  or  $V_{DD1} = 5\text{ V}$ ,  $V_{DD2} = 3.0\text{ V}$ .

**Table 3.**

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
<b>DC SPECIFICATIONS</b>						
Input Supply Current per Channel, Quiescent	$I_{DD1(Q)}$					
5 V/3 V Operation			0.50	0.53	mA	
3 V/5 V Operation			0.26	0.31	mA	
Output Supply Current per Channel, Quiescent	$I_{DDO(Q)}$					
5 V/3 V Operation			0.11	0.14	mA	
3 V/5 V Operation			0.19	0.21	mA	
<b>ADuM1300, Total Supply Current, Three Channels<sup>2</sup></b>						
<b>DC to 2 Mbps</b>						
$V_{DD1}$ Supply Current	$I_{DD1(Q)}$					
5 V/3 V Operation			1.6	2.5	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			0.9	1.7	mA	DC to 1 MHz logic signal freq.
$V_{DD2}$ Supply Current	$I_{DD2(Q)}$					
5 V/3 V Operation			0.4	0.7	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			0.7	1.0	mA	DC to 1 MHz logic signal freq.
<b>10 Mbps (BRW and CRW Grades Only)</b>						
$V_{DD1}$ Supply Current	$I_{DD1(10)}$					
5 V/3 V Operation			6.5	8.1	mA	5 MHz logic signal freq.
3 V/5 V Operation			3.4	4.9	mA	5 MHz logic signal freq.
$V_{DD2}$ Supply Current	$I_{DD2(10)}$					
5 V/3 V Operation			1.1	1.6	mA	5 MHz logic signal freq.
3 V/5 V Operation			1.9	2.5	mA	5 MHz logic signal freq.
<b>90 Mbps (CRW Grade Only)</b>						
$V_{DD1}$ Supply Current	$I_{DD1(90)}$					
5 V/3 V Operation			57	77	mA	45 MHz logic signal freq.
3 V/5 V Operation			31	48	mA	45 MHz logic signal freq.
$V_{DD2}$ Supply Current	$I_{DD2(90)}$					
5 V/3 V Operation			8	13	mA	45 MHz logic signal freq.
3 V/5 V Operation			16	18	mA	45 MHz logic signal freq.
<b>ADuM1301, Total Supply Current, Three Channels<sup>2</sup></b>						
<b>DC to 2 Mbps</b>						
$V_{DD1}$ Supply Current	$I_{DD1(Q)}$					
5 V/3 V Operation			1.3	2.1	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			0.7	1.4	mA	DC to 1 MHz logic signal freq.
$V_{DD2}$ Supply Current	$I_{DD2(Q)}$					
5 V/3 V Operation			0.6	0.9	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			1.0	1.4	mA	DC to 1 MHz logic signal freq.
<b>10 Mbps (BRW and CRW Grades Only)</b>						
$V_{DD1}$ Supply Current	$I_{DD1(10)}$					
5 V/3 V Operation			5.0	6.2	mA	5 MHz logic signal freq.
3 V/5 V Operation			2.6	3.7	mA	5 MHz logic signal freq.
$V_{DD2}$ Supply Current	$I_{DD2(10)}$					
5 V/3 V Operation			1.8	2.5	mA	5 MHz logic signal freq.
3 V/5 V Operation			3.4	4.2	mA	5 MHz logic signal freq.

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Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
90 Mbps (CRW Grade Only)						
$V_{DD1}$ Supply Current	$I_{DD1(90)}$					
5 V/3 V Operation			43	57	mA	45 MHz logic signal freq.
3 V/5 V Operation			24	36	mA	45 MHz logic signal freq.
$V_{DD2}$ Supply Current	$I_{DD2(90)}$					
5 V/3 V Operation			16	23	mA	45 MHz logic signal freq.
3 V/5 V Operation			29	37	mA	45 MHz logic signal freq.
For All Models						
Input Currents	$I_{IA}, I_{IB}, I_{IC}, I_{E1}, I_{E2}$	-10	+0.01	+10	$\mu$ A	$0 \leq V_{IA}, V_{IB}, V_{IC} \leq V_{DD1}$ or $V_{DD2}$ , $0 \leq V_{E1}, V_{E2} \leq V_{DD1}$ or $V_{DD2}$
Logic High Input Threshold	$V_{IH}, V_{EH}$					
5 V/3 V Operation		2.0			V	
3 V/5 V Operation		1.6			V	
Logic Low Input Threshold	$V_{IL}, V_{EL}$					
5 V/3 V Operation				0.8	V	
3 V/5 V Operation				0.4	V	
Logic High Output Voltages	$V_{OAH}, V_{OBH}, V_{OCH}$	$V_{DD1}, V_{DD2} - 0.1$	$V_{DD1}, V_{DD2}$		V	$I_{OX} = -20 \mu$ A, $V_{IX} = V_{IXH}$
		$V_{DD1}, V_{DD2} - 0.4$	$V_{DD1}, V_{DD2} - 0.2$		V	$I_{OX} = -4$ mA, $V_{IX} = V_{IXH}$
Logic Low Output Voltages	$V_{OAL}, V_{OBL}, V_{OCL}$		0.0	0.1	V	$I_{OX} = 20 \mu$ A, $V_{IX} = V_{IXL}$
			0.04	0.1	V	$I_{OX} = 400 \mu$ A, $V_{IX} = V_{IXL}$
			0.2	0.4	V	$I_{OX} = 4$ mA, $V_{IX} = V_{IXL}$
<b>SWITCHING SPECIFICATIONS</b>						
<b>ADuM130xARW</b>						
Minimum Pulse Width <sup>3</sup>	PW			1000	ns	$C_L = 15$ pF, CMOS signal levels
Maximum Data Rate <sup>4</sup>		1			Mbps	$C_L = 15$ pF, CMOS signal levels
Propagation Delay <sup>5</sup>	$t_{PHL}, t_{PLH}$	50	70	100	ns	$C_L = 15$ pF, CMOS signal levels
Pulse Width Distortion, $ t_{PLH} - t_{PHL} $ <sup>5</sup>	PWD			40	ns	$C_L = 15$ pF, CMOS signal levels
Propagation Delay Skew <sup>6</sup>	$t_{PSK}$			50	ns	$C_L = 15$ pF, CMOS signal levels
Channel-to-Channel Matching <sup>7</sup>	$t_{PSKCD/OD}$			50	ns	$C_L = 15$ pF, CMOS signal levels
<b>ADuM130xBRW</b>						
Minimum Pulse Width <sup>3</sup>	PW			100	ns	$C_L = 15$ pF, CMOS signal levels
Maximum Data Rate <sup>4</sup>		10			Mbps	$C_L = 15$ pF, CMOS signal levels
Propagation Delay <sup>5</sup>	$t_{PHL}, t_{PLH}$	15	35	50	ns	$C_L = 15$ pF, CMOS signal levels
Pulse Width Distortion, $ t_{PLH} - t_{PHL} $ <sup>5</sup>	PWD			3	ns	$C_L = 15$ pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	$C_L = 15$ pF, CMOS signal levels
Propagation Delay Skew <sup>6</sup>	$t_{PSK}$			6	ns	$C_L = 15$ pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels <sup>7</sup>	$t_{PSKCD}$			3	ns	$C_L = 15$ pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels <sup>7</sup>	$t_{PSKOD}$			22	ns	$C_L = 15$ pF, CMOS signal levels
<b>ADuM130xCRW</b>						
Minimum Pulse Width <sup>3</sup>	PW		8.3	11.1	ns	$C_L = 15$ pF, CMOS signal levels
Maximum Data Rate <sup>4</sup>		90	120		Mbps	$C_L = 15$ pF, CMOS signal levels
Propagation Delay <sup>5</sup>	$t_{PHL}, t_{PLH}$	20	30	40	ns	$C_L = 15$ pF, CMOS signal levels
Pulse Width Distortion, $ t_{PLH} - t_{PHL} $ <sup>5</sup>	PWD		0.5	2	ns	$C_L = 15$ pF, CMOS signal levels
Change vs. Temperature			3		ps/°C	$C_L = 15$ pF, CMOS signal levels
Propagation Delay Skew <sup>6</sup>	$t_{PSK}$			14	ns	$C_L = 15$ pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels <sup>7</sup>	$t_{PSKCD}$			2	ns	$C_L = 15$ pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels <sup>7</sup>	$t_{PSKOD}$			5	ns	$C_L = 15$ pF, CMOS signal levels



Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
For All Models						
Output Disable Propagation Delay (High/Low to High Impedance)	$t_{PHZ}, t_{PLH}$		6	8	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
Output Enable Propagation Delay (High Impedance to High/Low)	$t_{PZH}, t_{PZL}$		6	8	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
Output Rise/Fall Time (10% to 90%)	$t_r/t_f$					$C_L = 15 \text{ pF}$ , CMOS signal levels
5 V/3 V Operation			3.0		ns	
3 V/5 V Operation			2.5		ns	
Common-Mode Transient Immunity at Logic High Output <sup>8</sup>	$ CM_H $	25	35		kV/ $\mu$ s	$V_{ix} = V_{DD1}/V_{DD2}$ , $V_{CM} = 1000 \text{ V}$ , transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output <sup>8</sup>	$ CM_L $	25	35		kV/ $\mu$ s	$V_{ix} = 0 \text{ V}$ , $V_{CM} = 1000 \text{ V}$ , transient magnitude = 800 V
Refresh Rate	$f_r$					
5 V/3 V Operation			1.2		Mbps	
3 V/5 V Operation			1.1		Mbps	
Input Dynamic Supply Current, per Channel <sup>9</sup>	$I_{DDI(D)}$					
5 V/3 V Operation			0.19		mA/Mbps	
3 V/5 V Operation			0.10		mA/Mbps	
Output Dynamic Supply Current, per Channel <sup>9</sup>	$I_{DDI(D)}$					
5 V/3 V Operation			0.03		mA/Mbps	
3 V/5 V Operation			0.05		mA/Mbps	

<sup>1</sup> All voltages are relative to their respective ground.

<sup>2</sup> The supply current values are for all three channels combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate may be calculated as described in the Power Consumption section. See Figure 6 through Figure 8 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 9 through Figure 12 for total  $V_{DD1}$  and  $V_{DD2}$  supply currents as a function of data rate for ADuM1300/ADuM1301 channel configurations.

<sup>3</sup> The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

<sup>4</sup> The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

<sup>5</sup>  $t_{PHL}$  propagation delay is measured from the 50% level of the falling edge of the  $V_{ix}$  signal to the 50% level of the falling edge of the  $V_{ox}$  signal.  $t_{PLH}$  propagation delay is measured from the 50% level of the rising edge of the  $V_{ix}$  signal to the 50% level of the rising edge of the  $V_{ox}$  signal.

<sup>6</sup>  $t_{PSK}$  is the magnitude of the worst-case difference in  $t_{PHL}$  or  $t_{PLH}$  that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

<sup>7</sup> Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

<sup>8</sup>  $CM_H$  is the maximum common-mode voltage slew rate that can be sustained while maintaining  $V_O > 0.8 V_{DD2}$ .  $CM_L$  is the maximum common-mode voltage slew rate that can be sustained while maintaining  $V_O < 0.8 \text{ V}$ . The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

<sup>9</sup> Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 6 through Figure 8 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

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## PACKAGE CHARACTERISTICS

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input-to-Output) <sup>1</sup>	R <sub>I-O</sub>		10 <sup>1,2</sup>		Ω	
Capacitance (Input-to-Output) <sup>1</sup>	C <sub>I-O</sub>		1.7		pF	f = 1 MHz
Input Capacitance <sup>2</sup>	C <sub>I</sub>		4.0		pF	
IC Junction-to-Case Thermal Resistance, Side 1	θ <sub>JC1</sub>		33		°C/W	Thermocouple located
IC Junction-to-Case Thermal Resistance, Side 2	θ <sub>JC2</sub>		28		°C/W	at center of package underside

<sup>1</sup> Device considered a 2-terminal device; Pins 1, 2, 3, 4, 5, 6, 7, and 8 shorted together and Pins 9, 10, 11, 12, 13, 14, 15, and 16 shorted together.

<sup>2</sup> Input capacitance is from any input data pin to ground.

## REGULATORY INFORMATION

The ADuM130x have been approved by the organizations listed in Table 5.

Table 5.

UL	CSA	VDE	TÜV
Recognized under 1577 component recognition program <sup>1</sup>	Approved under CSA Component Acceptance Notice #5A	Certified according to DIN EN 60747-5-2 (VDE 0884 Part 2): 2003-01 <sup>2</sup>	Approved according to: IEC 61010-1:2001 (2 <sup>nd</sup> Edition), EN 61010-1:2001 (2 <sup>nd</sup> Edition) UL 61010-1:2004 CSA C22.2.61010.1:2005
Double/reinforced insulation, 2500 V rms isolation voltage	Reinforced insulation per CSA 60950-1-03 and IEC 60950-1, 400 V rms maximum working voltage	Basic insulation, 560 V peak	Reinforced insulation, 400 V rms maximum working voltage
File E214100	File 205078	Complies with DIN EN 60747-5-2 (VDE 0884 Part 2): 2003-01, DIN EN 60950 (VDE 0805): 2001-12; EN 60950: 2000 Reinforced insulation, 560 V peak File 2471900-4880-0001	Certificate U8V 05 06 56232 002

<sup>1</sup> In accordance with UL1577, each ADuM130x is proof tested by applying an insulation test voltage ≥3000 V rms for 1 sec (current leakage detection limit = 5 μA).

<sup>2</sup> In accordance with DIN EN 60747-5-2, each ADuM130x is proof tested by applying an insulation test voltage ≥1050 V peak for 1 sec (partial discharge detection limit = 5 pC). The \* marking branded on the component designates DIN EN 60747-5-2 approval.

## INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 6.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		2500	V rms	1 minute duration
Minimum External Air Gap (Clearance)	L(I01)	7.7 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	8.1 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

**DIN EN 60747-5-2 (VDE 0884 PART 2) INSULATION CHARACTERISTICS**

**Table 7.**

Description	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110 For Rated Mains Voltage $\leq 150$ V rms For Rated Mains Voltage $\leq 300$ V rms For Rated Mains Voltage $\leq 400$ V rms		I-IV I-III I-II	
Climatic Classification		40/105/21	
Pollution Degree (DIN VDE 0110, Table 1)		2	
Maximum Working Insulation Voltage	$V_{IORM}$	560	V peak
Input-to-Output Test Voltage, Method b1 $V_{IORM} \times 1.875 = V_{PR}$ , 100% Production Test, $t_m = 1$ sec, Partial Discharge $< 5$ pC	$V_{PR}$	1050	V peak
Input-to-Output Test Voltage, Method a After Environmental Tests Subgroup 1 $V_{IORM} \times 1.6 = V_{PR}$ , $t_m = 60$ sec, Partial Discharge $< 5$ pC After Input and/or Safety Test Subgroup 2/3 $V_{IORM} \times 1.2 = V_{PR}$ , $t_m = 60$ sec, Partial Discharge $< 5$ pC	$V_{PR}$	896 672	V peak V peak
Highest Allowable Overvoltage (Transient Overvoltage, $t_{TR} = 10$ sec)	$V_{TR}$	4000	V peak
Safety-Limiting Values (Maximum Value Allowed in the Event of a Failure; also see Figure 3) Case Temperature	$T_S$	150	$^{\circ}C$
Side 1 Current	$I_{S1}$	265	mA
Side 2 Current	$I_{S2}$	335	mA
Insulation Resistance at $T_S, V_{IO} = 500$ V	$R_S$	$>10^9$	$\Omega$

These isolators are suitable for basic electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits.

The \* marking on packages denotes DIN EN 60747-5-2 approval.

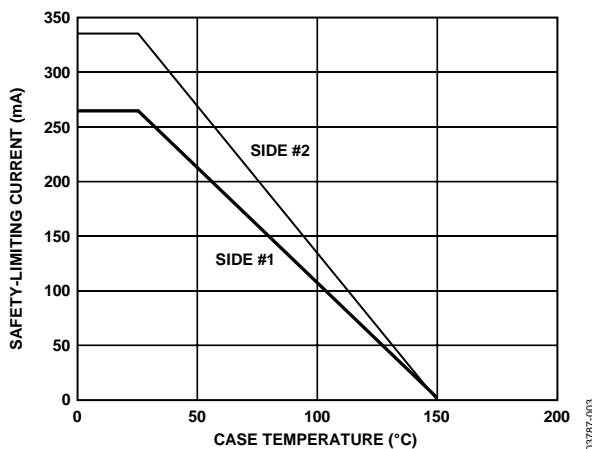


Figure 3. Thermal Derating Curve, Dependence of Safety-Limiting Values with Case Temperature per DIN EN 60747-5-2

**RECOMMENDED OPERATING CONDITIONS**

**Table 8.**

Parameter	Symbol	Min	Max	Unit
Operating Temperature	$T_A$	-40	+105	$^{\circ}C$
Supply Voltages <sup>1</sup>	$V_{DD1}, V_{DD2}$	2.7	5.5	V
Input Signal Rise and Fall Times			1.0	ms

<sup>1</sup> All voltages are relative to their respective ground. See the DC Correctness and Magnetic Field Immunity section for information on immunity to external magnetic fields.

# ADuM1300/ADuM1301

## ABSOLUTE MAXIMUM RATINGS

Ambient temperature = 25°C, unless otherwise noted.

Table 9.

Parameter	Symbol	Min	Max	Unit
Storage Temperature	$T_{ST}$	-65	+150	°C
Ambient Operating Temperature	$T_A$	-40	+105	°C
Supply Voltages <sup>1</sup>	$V_{DD1}, V_{DD2}$	-0.5	+7.0	V
Input Voltage <sup>1,2</sup>	$V_{IA}, V_{IB}, V_{IC}, V_{E1}, V_{E2}$	-0.5	$V_{DD1} + 0.5$	V
Output Voltage <sup>1,2</sup>	$V_{OA}, V_{OB}, V_{OC}$	-0.5	$V_{DD0} + 0.5$	V
Average Output Current per Pin <sup>3</sup>				
Side 1	$I_{O1}$	-23	+23	mA
Side 2	$I_{O2}$	-30	+30	mA
Common-Mode Transients <sup>4</sup>		-100	+100	kV/ $\mu$ s

<sup>1</sup> All voltages are relative to their respective ground.

<sup>2</sup>  $V_{DD1}$  and  $V_{DD0}$  refer to the supply voltages on the input and output sides of a given channel, respectively. See PC Board Layout section.

<sup>3</sup> See Figure 3 for maximum rated current values for various temperatures.

<sup>4</sup> Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the Absolute Maximum Ratings may cause latch-up or permanent damage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



Table 10. Truth Table (Positive Logic)

$V_{IX}$ Input <sup>1</sup>	$V_{EX}$ Input <sup>2</sup>	$V_{DD1}$ State <sup>1</sup>	$V_{DD0}$ State <sup>1</sup>	$V_{OX}$ Output <sup>1</sup>	Notes
H	H or NC	Powered	Powered	H	Outputs return to the input state within 1 $\mu$ s of $V_{DD1}$ power restoration.
L	H or NC	Powered	Powered	L	
X	L	Powered	Powered	Z	
X	H or NC	Unpowered	Powered	H	
X	L	Unpowered	Powered	Z	Outputs return to the input state within 1 $\mu$ s of $V_{DD0}$ power restoration, if $V_{EX}$ state is H or NC. Outputs returns to high impedance state within 8 ns of $V_{DD0}$ power restoration, if $V_{EX}$ state is L.
X	X	Powered	Unpowered	Indeterminate	

<sup>1</sup>  $V_{IX}$  and  $V_{OX}$  refer to the input and output signals of a given channel (A, B, or C).  $V_{EX}$  refers to the output enable signal on the same side as the  $V_{OX}$  outputs.  $V_{DD1}$  and  $V_{DD0}$  refer to the supply voltages on the input and output sides of the given channel, respectively.

<sup>2</sup> In noisy environments, connecting  $V_{EX}$  to an external logic high or low is recommended.

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

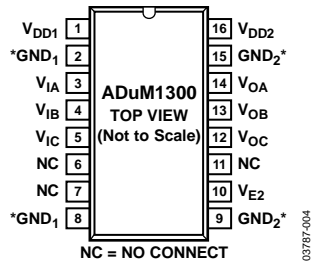


Figure 4. ADuM1300 Pin Configuration

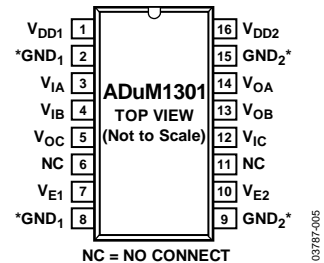


Figure 5. ADuM1301 Pin Configuration

\*Pins 2 and 8 are internally connected, and connecting both to GND<sub>1</sub> is recommended. Pins 9 and 15 are internally connected, and connecting both to GND<sub>2</sub> is recommended. Output enable Pin 10 on the ADuM1300 can be left disconnected if outputs are to be always enabled. Output enable Pins 7 and 10 on the ADuM1301 can be left disconnected if outputs are to be always enabled. In noisy environments, connecting Pin 7 (for ADuM1301) and Pin 10 (for both models) to an external logic high or low is recommended.

Table 11. ADuM1300 Pin Function Descriptions

Pin No.	Mnemonic	Function
1	V <sub>DD1</sub>	Supply Voltage for Isolator Side 1, 2.7 V to 5.5 V.
2	GND <sub>1</sub>	Ground 1. Ground reference for isolator Side 1.
3	V <sub>IA</sub>	Logic Input A.
4	V <sub>IB</sub>	Logic Input B.
5	V <sub>IC</sub>	Logic Input C.
6	NC	No Connect.
7	NC	No Connect.
8	GND <sub>1</sub>	Ground 1. Ground reference for isolator Side 1.
9	GND <sub>2</sub>	Ground 2. Ground reference for isolator Side 2.
10	V <sub>E2</sub>	Output Enable 2. Active high logic input. V <sub>OA</sub> , V <sub>OB</sub> , and V <sub>OC</sub> outputs are enabled when V <sub>E2</sub> is high or disconnected. V <sub>OA</sub> , V <sub>OB</sub> , and V <sub>OC</sub> outputs are disabled when V <sub>E2</sub> is low. In noisy environments, connecting V <sub>E2</sub> to an external logic high or low is recommended.
11	NC	No Connect.
12	V <sub>OC</sub>	Logic Output C.
13	V <sub>OB</sub>	Logic Output B.
14	V <sub>OA</sub>	Logic Output A.
15	GND <sub>2</sub>	Ground 2. Ground reference for isolator Side 2.
16	V <sub>DD2</sub>	Supply Voltage for Isolator Side 2, 2.7 V to 5.5 V.

Table 12. ADuM1301 Pin Function Descriptions

Pin No.	Mnemonic	Function
1	V <sub>DD1</sub>	Supply Voltage for Isolator Side 1, 2.7 V to 5.5 V.
2	GND <sub>1</sub>	Ground 1. Ground reference for isolator Side 1.
3	V <sub>IA</sub>	Logic Input A.
4	V <sub>IB</sub>	Logic Input B.
5	V <sub>OC</sub>	Logic Output C.
6	NC	No Connect.
7	V <sub>E1</sub>	Output Enable 1. Active high logic input. V <sub>OC</sub> output is enabled when V <sub>E1</sub> is high or disconnected. V <sub>OC</sub> is disabled when V <sub>E1</sub> is low. In noisy environments, connecting V <sub>E1</sub> to an external logic high or low is recommended.
8	GND <sub>1</sub>	Ground 1. Ground reference for isolator Side 1.
9	GND <sub>2</sub>	Ground 2. Ground reference for isolator Side 2.
10	V <sub>E2</sub>	Output Enable 2. Active high logic input. V <sub>OA</sub> and V <sub>OB</sub> outputs are enabled when V <sub>E2</sub> is high or disconnected. V <sub>OA</sub> and V <sub>OB</sub> outputs are disabled when V <sub>E2</sub> is low. In noisy environments, connecting V <sub>E2</sub> to an external logic high or low is recommended.
11	NC	No Connect.
12	V <sub>IC</sub>	Logic Input C.
13	V <sub>OB</sub>	Logic Output B.
14	V <sub>OA</sub>	Logic Output A.
15	GND <sub>2</sub>	Ground 2. Ground reference for isolator Side 2.
16	V <sub>DD2</sub>	Supply Voltage for Isolator Side 2, 2.7 V to 5.5 V.

## TYPICAL PERFORMANCE CHARACTERISTICS

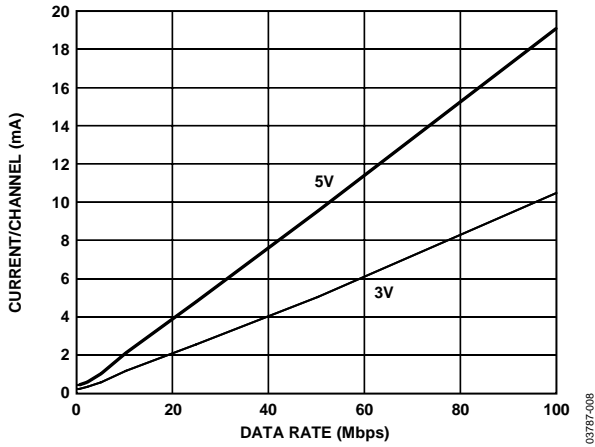


Figure 6. Typical Input Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation

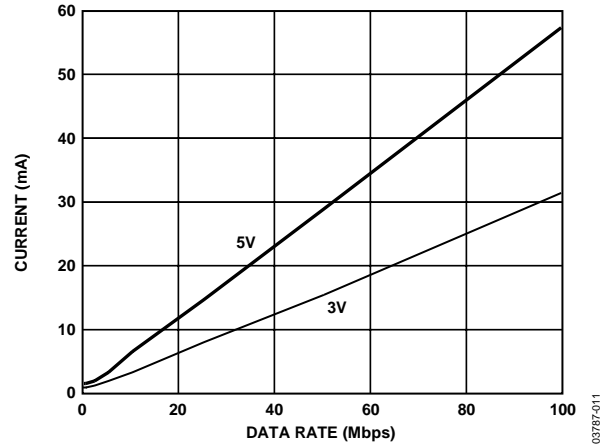


Figure 9. Typical ADuM1300  $V_{DD1}$  Supply Current vs. Data Rate for 5 V and 3 V Operation

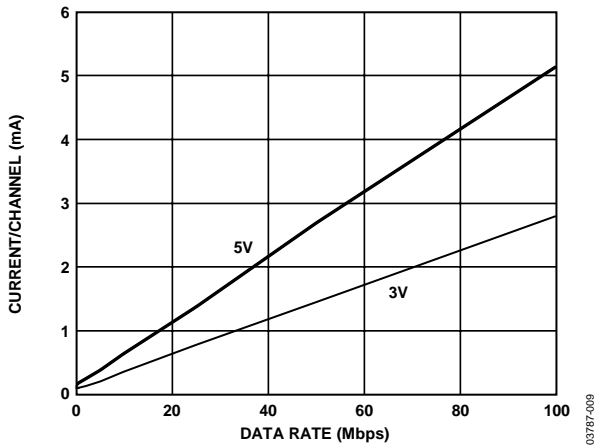


Figure 7. Typical Output Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation (No Output Load)

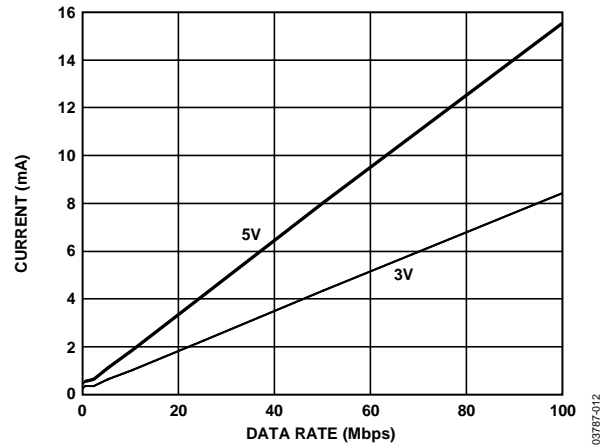


Figure 10. Typical ADuM1300  $V_{DD2}$  Supply Current vs. Data Rate for 5 V and 3 V Operation

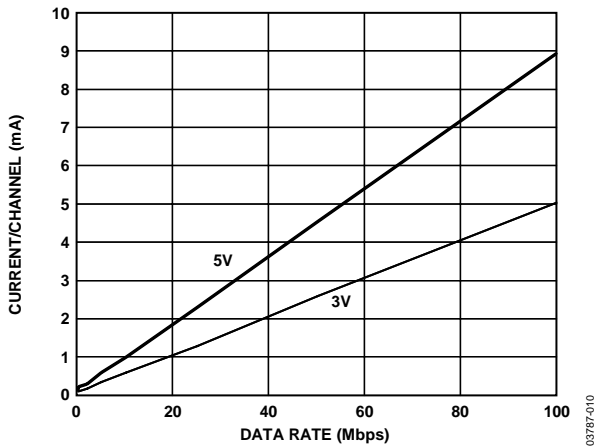


Figure 8. Typical Output Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation (15 pF Output Load)

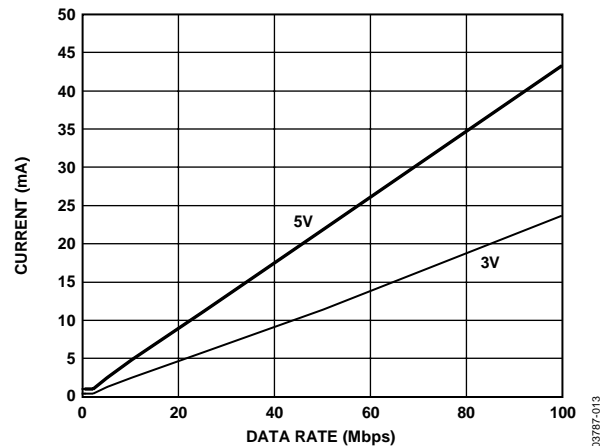


Figure 11. Typical ADuM1301  $V_{DD1}$  Supply Current vs. Data Rate for 5 V and 3 V Operation

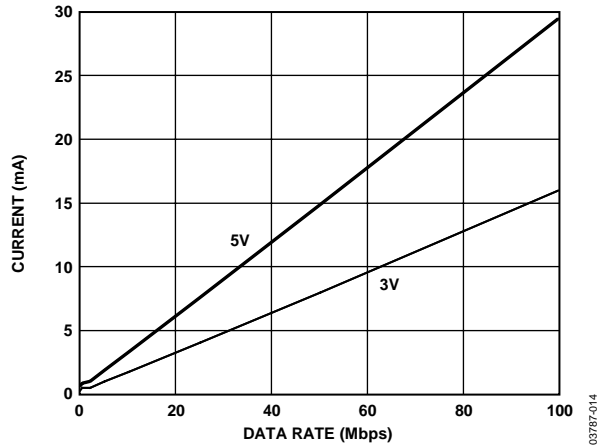


Figure 12. Typical ADuM1301 V<sub>DD2</sub> Supply Current vs. Data Rate for 5 V and 3 V Operation

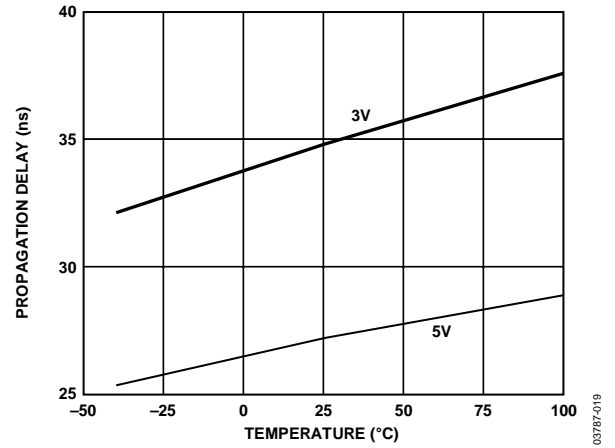


Figure 13. Propagation Delay vs. Temperature, C Grade

## APPLICATION INFORMATION

### PC BOARD LAYOUT

The ADuM130x digital isolator requires no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins (Figure 14). Bypass capacitors are most conveniently connected between Pins 1 and 2 for  $V_{DD1}$  and between Pins 15 and 16 for  $V_{DD2}$ . The capacitor value should be between  $0.01 \mu\text{F}$  and  $0.1 \mu\text{F}$ . The total lead length between both ends of the capacitor and the input power supply pin should not exceed 20 mm. Bypassing between Pins 1 and 8 and between Pins 9 and 16 should also be considered unless the ground pair on each package side is connected close to the package.

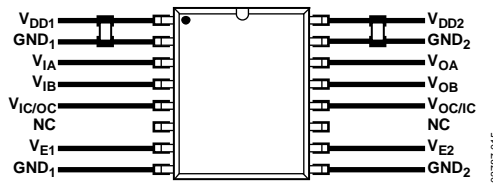


Figure 14. Recommended Printed Circuit Board Layout

In applications involving high common-mode transients, care should be taken to ensure that board coupling across the isolation barrier is minimized. Furthermore, the board layout should be designed such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this could cause voltage differentials between pins exceeding the device's Absolute Maximum Ratings, thereby leading to latch-up or permanent damage.

### PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The propagation delay to a logic low output may differ from the propagation delay to a logic high.

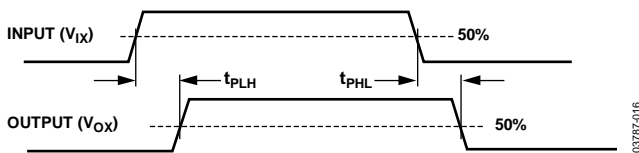


Figure 15. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the input signal's timing is preserved.

Channel-to-channel matching refers to the maximum amount that the propagation delay differs between channels within a single ADuM130x component.

Propagation delay skew refers to the maximum amount that the propagation delay differs between multiple ADuM130x components operating under the same conditions.

### DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow ( $\sim 1 \text{ ns}$ ) pulses to be sent to the decoder via the transformer. The decoder is bistable and is therefore either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than  $2 \mu\text{s}$ , a periodic set of refresh pulses indicative of the correct input state are sent to ensure dc correctness at the output. If the decoder receives no internal pulses for more than about  $5 \mu\text{s}$ , the input side is assumed to be unpowered or nonfunctional, in which case the isolator output is forced to a default state (see Table 10) by the watchdog timer circuit.

The ADuM130x is extremely immune to external magnetic fields. The limitation on the ADuM130x's magnetic field immunity is set by the condition in which induced voltage in the transformer's receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this may occur. The 3 V operating condition of the ADuM130x is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt) \sum \pi r_n^2; n = 1, 2, \dots, N$$

where:

$\beta$  is magnetic flux density (gauss).

$N$  is the number of turns in the receiving coil.

$r_n$  is the radius of the  $n^{\text{th}}$  turn in the receiving coil (cm).

Given the geometry of the receiving coil in the ADuM130x and an imposed requirement that the induced voltage be at most 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated as shown in Figure 16.

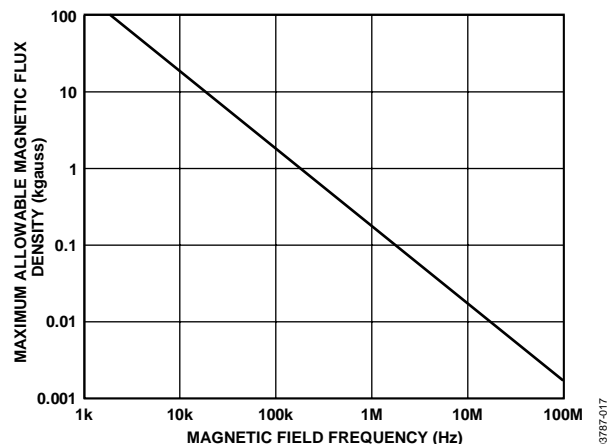


Figure 16. Maximum Allowable External Magnetic Flux Density



For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event were to occur during a transmitted pulse (and was of the worst-case polarity), it would reduce the received pulse from >1.0 V to 0.75 V—still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the ADuM130x transformers. Figure 17 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown, the ADuM130x is extremely immune and can be affected only by extremely large currents operated at high frequency very close to the component. For the 1 MHz example noted, one would have to place a 0.5 kA current 5 mm away from the ADuM130x to affect the component's operation.

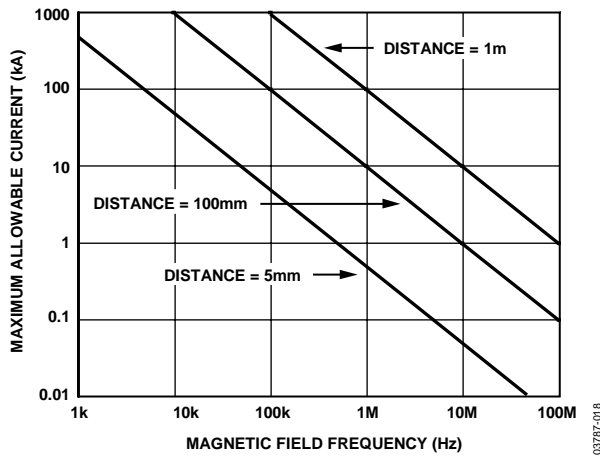


Figure 17. Maximum Allowable Current for Various Current-to-ADuM130x Spacings

Note that at combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces could induce error voltages sufficiently large enough to trigger

the thresholds of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

## POWER CONSUMPTION

The supply current at a given channel of the ADuM130x isolator is a function of the supply voltage, the channel's data rate, and the channel's output load.

For each input channel, the supply current is given by

$$I_{DDI} = I_{DDI(Q)} \quad f \leq 0.5 f_r$$

$$I_{DDI} = I_{DDI(D)} \times (2f - f_r) + I_{DDI(Q)} \quad f > 0.5 f_r$$

For each output channel, the supply current is given by

$$I_{DDO} = I_{DDO(Q)} \quad f \leq 0.5 f_r$$

$$I_{DDO} = (I_{DDO(D)} + (0.5 \times 10^{-3}) \times C_L \times V_{DDO}) \times (2f - f_r) + I_{DDO(Q)} \quad f > 0.5 f_r$$

where:

$I_{DDI(D)}$ ,  $I_{DDO(D)}$  are the input and output dynamic supply currents per channel (mA/Mbps).

$C_L$  is the output load capacitance (pF).

$V_{DDO}$  is the output supply voltage (V).

$f$  is the input logic signal frequency (MHz); it is half of the input data rate expressed in units of Mbps.

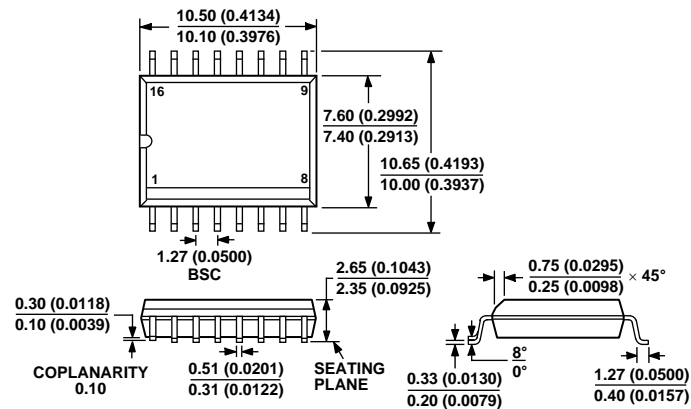
$f_r$  is the input stage refresh rate (Mbps).

$I_{DDI(Q)}$ ,  $I_{DDO(Q)}$  are the specified input and output quiescent supply currents (mA).

To calculate the total  $V_{DD1}$  and  $V_{DD2}$  supply current, the supply currents for each input and output channel corresponding to  $V_{DD1}$  and  $V_{DD2}$  are calculated and totaled. Figure 6 and Figure 7 provide per-channel supply currents as a function of data rate for an unloaded output condition. Figure 8 provides per-channel supply current as a function of data rate for a 15 pF output condition. Figure 9 through Figure 12 provide total  $V_{DD1}$  and  $V_{DD2}$  supply current as a function of data rate for ADuM1300/ADuM1301 channel configurations.

# ADuM1300/ADuM1301

## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AA  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 18. 16-Lead Standard Small Outline Package [SOIC\_W]  
 Wide Body (RW-16)  
 Dimensions shown in millimeters and (inches)

## ORDERING GUIDE

Model	Number of Inputs, V <sub>DD1</sub> Side	Number of Inputs, V <sub>DD2</sub> Side	Maximum Data Rate (Mbps)	Maximum Propagation Delay, 5 V (ns)	Maximum Pulse Width Distortion (ns)	Temperature Range (°C)	Package Option <sup>1</sup>
ADuM1300ARW <sup>2</sup>	3	0	1	100	40	-40 to +105	RW-16
ADuM1300BRW <sup>2</sup>	3	0	10	50	3	-40 to +105	RW-16
ADuM1300CRW <sup>2</sup>	3	0	90	32	2	-40 to +105	RW-16
ADuM1300ARWZ <sup>2,3</sup>	3	0	1	100	40	-40 to +105	RW-16
ADuM1300BRWZ <sup>2,3</sup>	3	0	10	50	3	-40 to +105	RW-16
ADuM1300CRWZ <sup>2,3</sup>	3	0	90	32	2	-40 to +105	RW-16
ADuM1301ARW <sup>2</sup>	2	1	1	100	40	-40 to +105	RW-16
ADuM1301BRW <sup>2</sup>	2	1	10	50	3	-40 to +105	RW-16
ADuM1301CRW <sup>2</sup>	2	1	90	32	2	-40 to +105	RW-16
ADuM1301ARWZ <sup>2,3</sup>	2	1	1	100	40	-40 to +105	RW-16
ADuM1301BRWZ <sup>2,3</sup>	2	1	10	50	3	-40 to +105	RW-16
ADuM1301CRWZ <sup>2,3</sup>	2	1	90	32	2	-40 to +105	RW-16

<sup>1</sup> RW-16 = 16-lead wide body SOIC.

<sup>2</sup> Tape and reel are available. The addition of an -RL suffix designates a 13" (1,000 units) tape-and-reel option.

<sup>3</sup> Z = Pb-free part.

**NOTES**

**NOTES**