R8610
Datasheet Brief
32-BIT RISC MICROPROCESSOR

RDC ***RISC DSP Communication***

RDC Semiconductor Co., Ltd
http://www.rdc.com.tw
TEL: 886-3-666-2866
FAX: 886-3-563-1498

1. Overview

The R8610 is a high performance and fully static 32-bit RISC microcontroller with the compatibility of Windows based, Linux and most popular 32-bit RTOS. It also integrates 16KB write direct map L1 cache, PCI rev. 2.1 32-bit bus interface at 33 MHz, SDRAM/ROM/memory controller, IPC (Internal Peripheral Controllers with DMA and interrupt timer/counter included), Fast Ethernet MAC, FIFO UART, 10/100M MAC and USB2.0 Host within a single 216-pin LQFP package to form a system-on-a-chip (SOC). It provides an ideal solution for the embedded system and communications products (such as thin client, NAT router, home gateway, access point and tablet PC) to bring about desired performance.

2. Features

- ***Embedded RISC Controller***
  - Full 32-bit RISC architecture
  - Supports diverse operation systems, including Windows based, Linux and most popular 32-bit RTOS
  - 6-stage pipeline
  - Speeds up to 133 MHz and above
  - Supports MMU function which includes 32 TLB entries
- ***MAC Controller***
  - Supports two-port 10/100 Fast Ethernet MAC
  - IEEE 802.3u MII interface
  - IEEE 802.3x flow control in full-duplex mode
  - Descriptor architecture for packet TX/RX
- ***Interrupt Controller***
  - Provides two 8259 compatible interrupt controllers which are cascaded internally
  - Independent programmable level/edge-triggered interrupt channels
  - Serial IRQ supported
- ***DMA Controller***
  - Provides two 8237 DMA compatible controllers which are cascaded internally
  - 4 channels for 8-bit DMA transfer and 3 channels for 16-bit transfer
  - Supports 8/16/32-bit channel 4 bus master on the LPC bus
- ***Two USB 2.0 Host Port Support***
  - Supports HS, FS and LS
- ***FIFO UART Port***
  - A high performance UART port with transmit and receive FIFOs
  - Supports the programmable baud rate generator with the data rates from 50 to 115,200 bps
  - The character options are programmable for 1 start bit; 1, 1.5 or 2 stop bits; even, odd or no parity; 5~8 data bits
- ***PCI Control Interface***
  - Supports PCI Rev 2.1 specification
  - 32-bit bus interface
  - Supports PCI clock at 33 MHz
  - Supports PCI host
  - Supports PCI master/slave
  - Up to 133 Mbytes/sec maximum bandwidth
  - Supports up to 3 external master devices on PCI
  - Provides four PCI interrupt channels
- ***LPC (Low Pin Count) Bus Interface***
  - LPC revision 1.0 compliant
  - Supports LPC/FWH (Firmware Hub) compliant interfaces
  - Provides the interface to connect an LPC/FWH Flash ROM or Super I/O chip
  - Supports LPC DMA
  - Supports serial IRQ
  - Supports bus master mode
- ***X-Bus Interface***
  - Provides the interface to boot ROM BIOS & DOC (Disk On Chip).
  - Supports 8/16-bit data width
  - Provides ROMCS_n for booting from X-bus Flash ROM

- Supports from 64K-byte to Max. 16M-byte ROM space addressing
- Supports two independent and programmable CSs (Chip Selects)

■ ***SDRAM Control Interface***

- PC100/PC133 compliant
- Supports 16-bit data bus width
- Supports speeds up to 133 MHz and above
- Supports maximum 128 MB memory space

■ ***On-Chip L1 16KB Cache***

- Unifies instructions and data cache
- Supports write through for cache write policy
- Snooping mechanism support for data coherence between main memory and cache
- Direct map

■ ***General Programmable I/O***

- Supports 56 programmable I/O pins
- Each GPIO pin can be individually configured to be an input/output pin

■ ***Counter/Timers***

- 8254 compatible timers
- Provides three independent programmable timers / counters
- Supports a watchdog timer (WDT)
- Supports a speaker output

■ ***Real Time Clock (External)***

- Provides a direct interface to external RTC chips

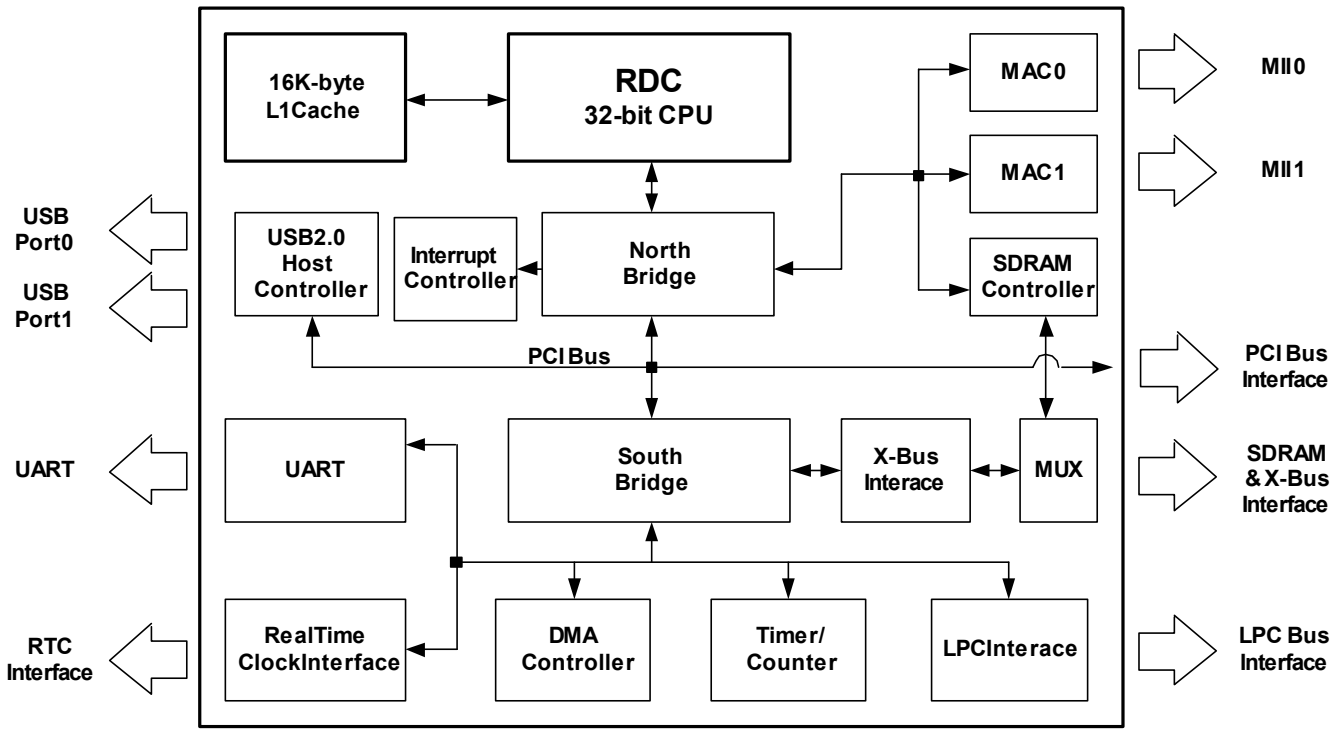
■ ***Operating Voltage Range***

- Core voltage: 1.8 V ± 5%
- I/O voltage: 3.3 V ± 10%

■ ***Package Type***

- 216-pin LQFP

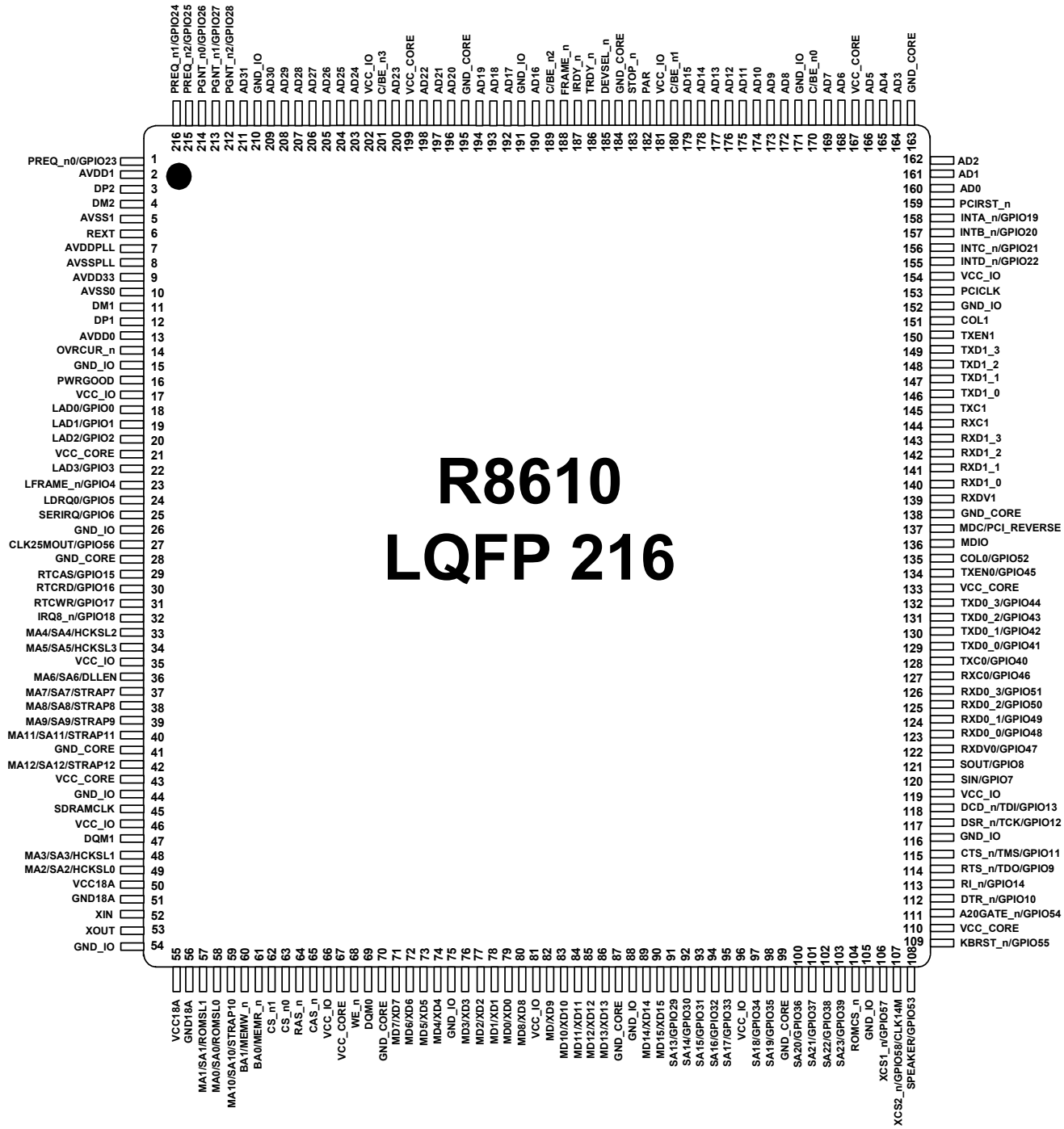
3. Block Diagram



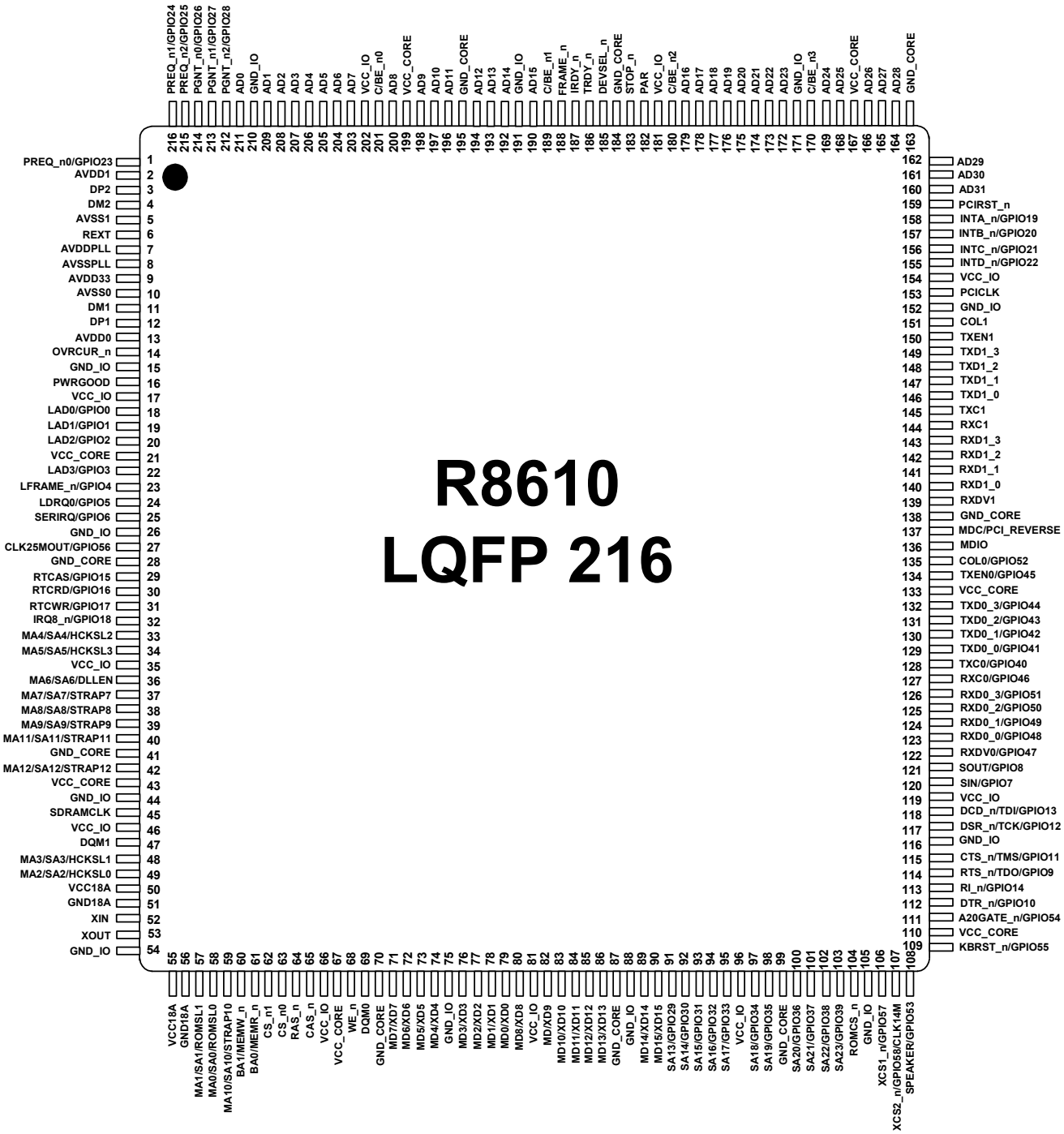
4. PIN Description

4.1 PIN Placement

4.1.1 MDC pulled low

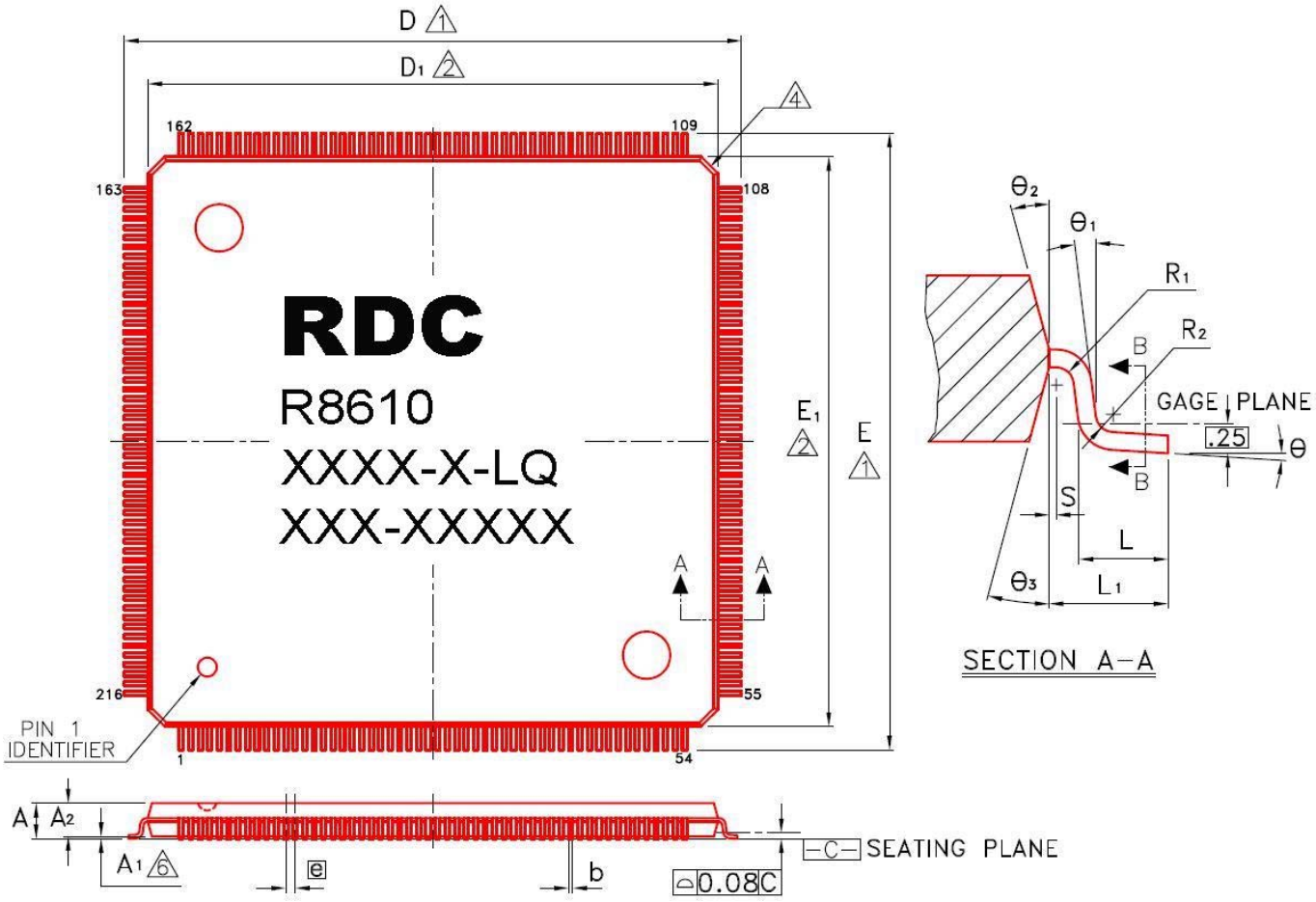


4.1.2 MDC pulled high



5. Package Information

LQFP: 216 pins



6. Revision History

Rev.	Date	History
D01	01/31/2005	Draft Version 0.1
D02	02/22/2005	Draft Version 0.2