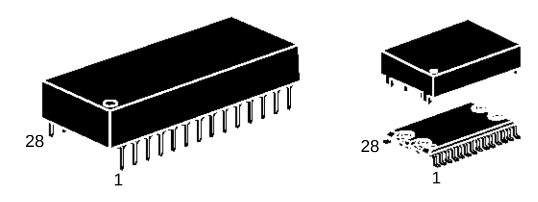
CMOS 8K x 8 TIMEKEEPER SRAM

- INTEGRATED ULTRA LOW POWER SRAM, REAL TIME CLOCK and POWER-FAIL CONTROL CIRCUIT
- BYTEWIDE RAM-LIKE CLOCK ACCESS
- BCD CODED YEAR, MONTH, DAY, DATE, HOURS, MINUTES and SECONDS
- CLOCK ACCURACY of ± 1 MINUTE a MONTH, @ 25°C
- SOFTWARE CONTROLLED CLOCK CALIBRATION for HIGH ACCURACY APPLICATIONS
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- CHOICE of TWO WRITE PROTECT VOLTAGES:
  - M48T08: 4.5V ≤ V_{PFD} ≤ 4.75V
  - M48T18: 4.2V ≤ V_{PFD} ≤ 4.5V
- SELF CONTAINED BATTERY and CRYSTAL in the CAPHAT DIP PACKAGE
- SMALL OUTLINE PACKAGE PROVIDES DIRECT CONNECTION for a SNAPHAT HOUSING CONTAINING the BATTERY and CRYSTAL
- SNAPHAT HOUSING (BATTERY and CRYSTAL) REPLACEABLE
- 10 YEARS of DATA RETENTION and CLOCK OPERATION in the ABSENCE of POWER
- PIN and FUNCTION COMPATIBLE with JEDEC STANDARD 8K x 8 SRAMs



PCDIP28 (PC)
Battery CAPHAT

SOH28 (MH)
Battery SNAPHAT

Table 1. Signal Names

A0-A12	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{\text{INT}}$	Power Fail Interrupt
$\overline{\text{E1}}$	Chip Enable 1
E2	Chip Enable 2
$\overline{\text{G}}$	Output Enable
$\overline{\text{W}}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

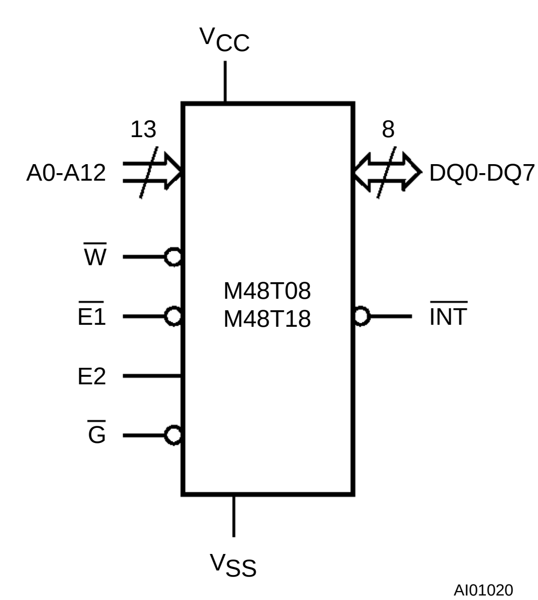


Figure 2A. DIP Pin Connections

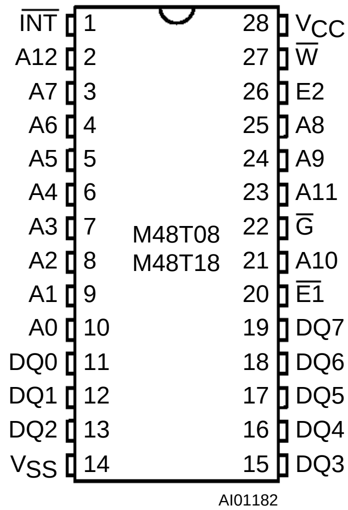


Figure 2B. SO Pin Connections

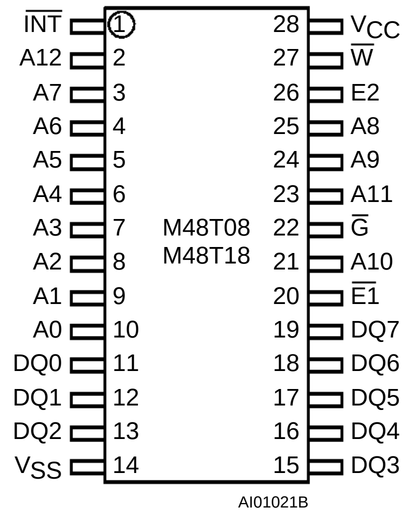


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature (V_{CC} Off, Oscillator Off)	–40 to 85	°C
V_{IO}	Input or Output Voltages	–0.3 to 7	V
V_{CC}	Supply Voltage	–0.3 to 7	V
I_O	Output Current	20	mA
P_D	Power Dissipation	1	W

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

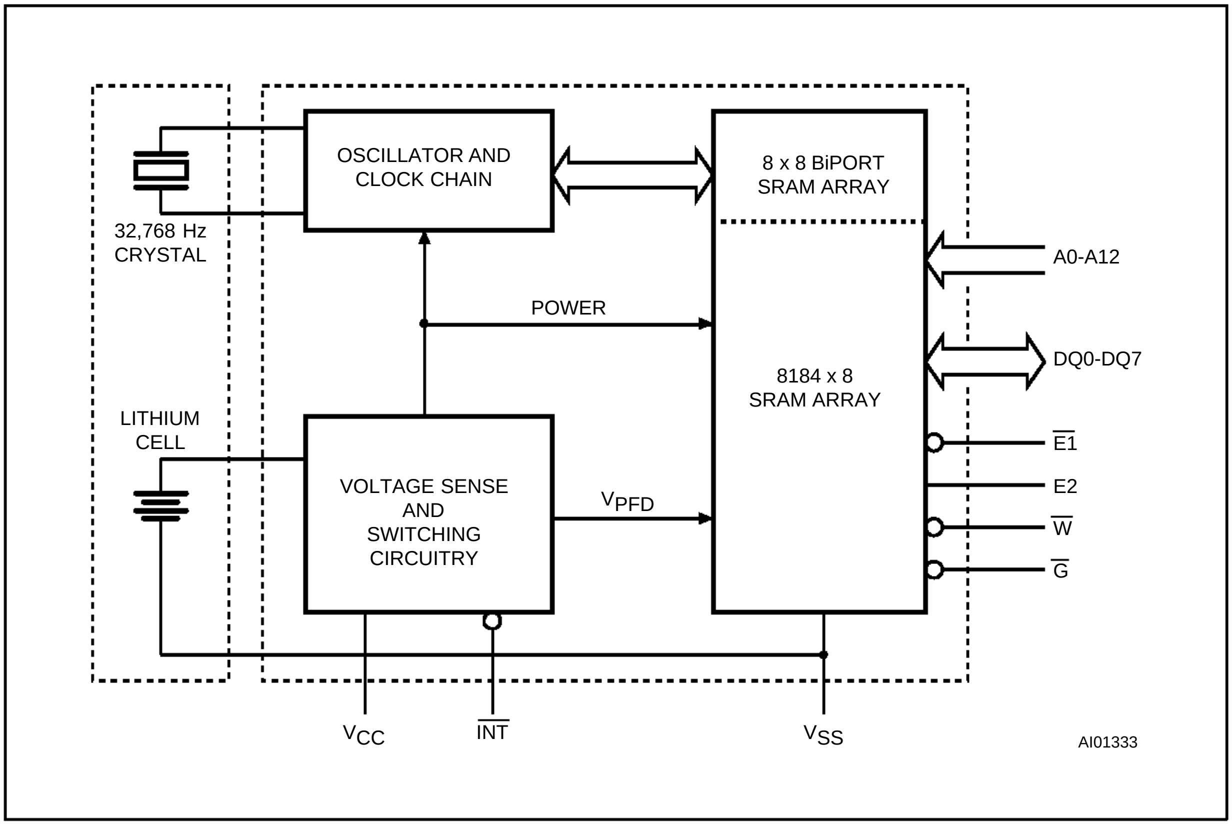
CAUTION: *Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

Table 3. Operating Modes

Mode	V_{CC}	$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.75V to 5.5V or 4.5V to 5.5V	V_{IH}	X	X	X	High Z	Standby
Deselect		X	V_{IL}	X	X	High Z	Standby
Write		V_{IL}	V_{IH}	X	V_{IL}	D_{IN}	Active
Read		V_{IL}	V_{IH}	V_{IL}	V_{IH}	D_{OUT}	Active
Read		V_{IL}	V_{IH}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min)	X	X	X	X	High Z	CMOS Standby
Deselect	$\leq V_{SO}$	X	X	X	X	High Z	Battery Back-up Mode

Note: X = V_{IH} or V_{IL}

Figure 3. Block Diagram



DESCRIPTION

The M48T08,18 TIMEKEEPER™ RAM is an 8K x 8 non-volatile static RAM and real time clock which is pin and functional compatible with the MK48T08,18. The monolithic chip is available in two special packages to provide a highly integrated battery backed-up memory and real time clock solution.

The M48T08,18 is a non-volatile pin and function equivalent to any JEDEC standard 8K x 8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The 28 pin 600mil DIP CAPHAT™ houses the M48T08,18 silicon with a quartz crystal and a long life lithium button cell in a single package.

The 28 pin 330mil SO provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT™ housing containing the battery and crystal. The unique design allows the SNAPHAT battery package to be mounted on top of the SO package after the completion of the surface mount process.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

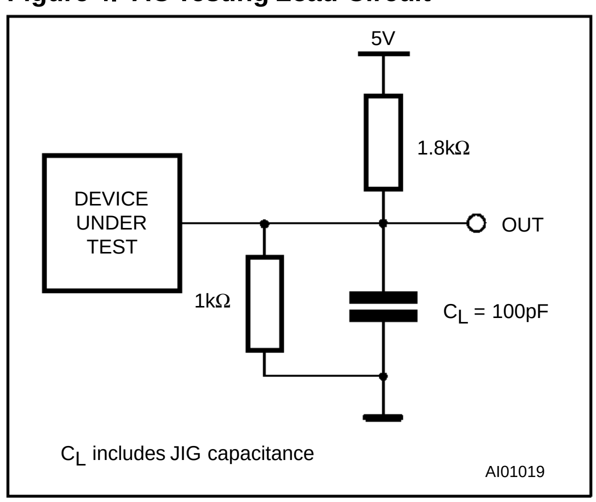


Table 4. Capacitance [1] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		10	pF
C_{IO} [2]	Input / Output Capacitance	V_{OUT} = 0V		10	pF

Notes: 1. Effective capacitance calculated from the equation C = IΔt/ΔV with ΔV = 3V and power supply at 5V.
2. Outputs deselected

Table 5. DC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI} [1]	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±1	µA
I_{LO} [1]	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±5	µA
I_{CC}	Supply Current	Outputs open		80	mA
I_{CC1} [2]	Supply Current (Standby) TTL	$\overline{E1}$ = V_{IH}, E2 = V_{IL}		3	mA
I_{CC2} [2]	Supply Current (Standby) CMOS	$\overline{E1}$ = V_{CC} – 0.2V, E2 = V_{SS} + 0.2V		3	mA
V_{IL} [3]	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
	Output Low Voltage ($\overline{INT}$) [4]	I_{OL} = 0.5mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4		V

Notes: 1. Outputs Deselected.
2. Measured with Control Bits set as follows: R = '1'; W, ST, FT = '0'.
3. Negative spikes of –1V allowed for up to 10ns once per Cycle.
4. The $\overline{INT}$ pin is Open Drain.

Table 6. Power Down/Up Trip Points DC Characteristics [1] (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage (M48T08)	4.5	4.6	4.75	V
V_{PFD}	Power-fail Deselect Voltage (M48T18)	4.2	4.3	4.5	V
V_{SO}	Battery Back-up Switchover Voltage		3.0		V
t_{DR} [2]	Expected Data Retention Time	10			YEARS

Notes: 1. All voltages referenced to V_{SS}.
2. @ 25°C

DESCRIPTION (cont'd)

Insertion of the SNAPHAT housing after reflow prevents potential battery and crystal damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is keyed to prevent reverse insertion.

The SO and battery packages are shipped separately in plastic anti-static tubes. The SO package is also available to ship in Tape & Reel form. For the 28 lead SO, the battery package (i.e. SNAPHAT) part number is "M4T28-BR12SH1".

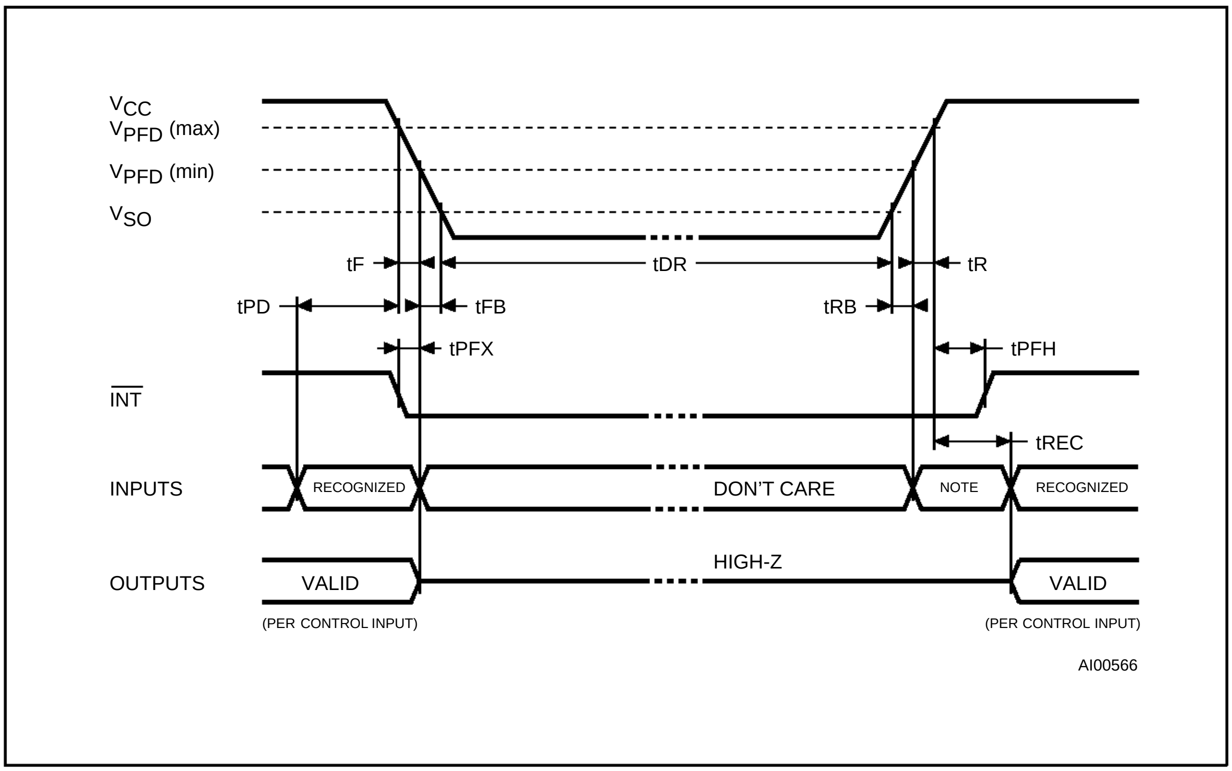
As Figure 3 shows, the static memory array and the quartz controlled clock oscillator of the M48T08,18 are integrated on one silicon chip. The two circuits are interconnected at the upper eight memory locations to provide user accessible BYTEWIDE™ clock information in the bytes with addresses 1FF8h-1FFFh. The clock locations contain the year, month, date, day, hour, minute, and second in

Table 7. Power Down/Up Mode AC Characteristics (T_A = 0 to 70°C)

Symbol	Parameter	Min	Max	Unit
t_{PD}	$\overline{E1}$ or $\overline{W}$ at V_{IH} or E2 at V_{IL} before Power Down	0		µs
t_F (1)	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs
t_{FB} (2)	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs
t_R	V_{PFD}(min) to V_{PFD} (max) V_{CC} Rise Time	0		µs
t_{RB}	V_{SO} to V_{PFD} (min) V_{CC} Rise Time	1		µs
t_{REC}	$\overline{E1}$ or $\overline{W}$ at V_{IH} or E2 at V_{IL} after Power Up	1		ms
t_{PFX}	$\overline{INT}$ Low to Auto Deselect	10	40	µs
t_{PFH} (3)	V_{PFD} (max) to $\overline{INT}$ High		120	µs

Notes: 1. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).
2. V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.
3. INT may go high anytime after V_{CC} exceeds V_{PFD} (min) and is guaranteed to go high t_{PFH} after V_{CC} exceeds V_{PFD} (max).

Figure 5. Power Down/Up Mode AC Waveforms



Note: Inputs may or may not be recognized at this time. Caution should be taken to keep $\overline{E1}$ high or E2 low as V_{CC} rises past V_{PFD}(min). Some systems may performs inadvertent write cycles after V_{CC} rises above V_{PFD}(min) but before normal system operations begins. Even though a power on reset is being applied to the processor a reset condition may not occur until after the system clock is running.

Table 8. Read Mode AC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48T08 / 18				Unit
		-100		-150		
		Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	100		150		ns
t_{AVQV}	Address Valid to Output Valid		100		150	ns
t_{E1LQV}	Chip Enable 1 Low to Output Valid		100		150	ns
t_{E2HQV}	Chip Enable 2 High to Output Valid		100		150	ns
t_{GLQV}	Output Enable Low to Output Valid		50		75	ns
t_{E1LQX}	Chip Enable 1 Low to Output Transition	10		10		ns
t_{E2HQX}	Chip Enable 2 High to Output Transition	10		10		ns
t_{GLQX}	Output Enable Low to Output Transition	5		5		ns
t_{E1HQZ}	Chip Enable 1 High to Output Hi-Z		50		75	ns
t_{E2LQZ}	Chip Enable 2 Low to Output Hi-Z		50		75	ns
t_{GHQZ}	Output Enable High to Output Hi-Z		40		60	ns
t_{AXQX}	Address Transition to Output Transition	5		5		ns

Figure 6. Read Mode AC Waveforms

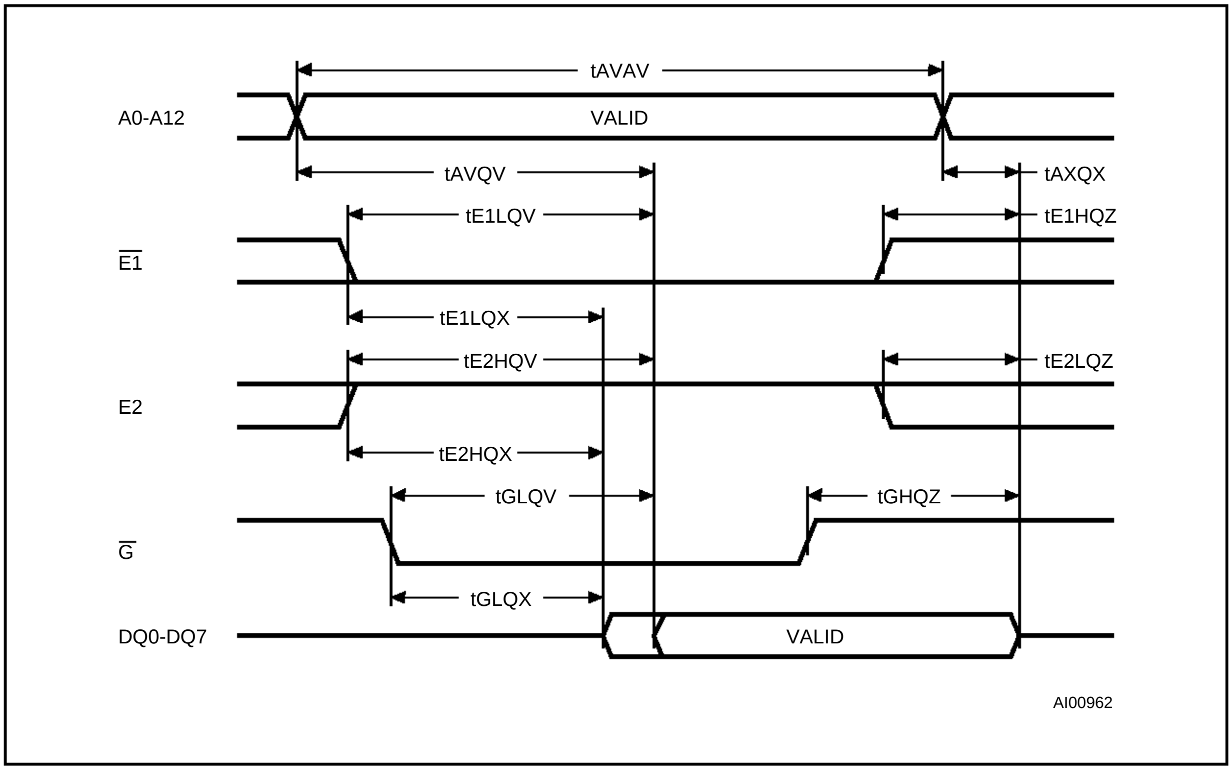


Table 9. Write Mode AC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48T08 / 18				Unit
		-100		-150		
		Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	100		150		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		ns
t_{AVE1L}	Address Valid to Chip Enable 1 Low	0		0		ns
t_{AVE2H}	Address Valid to Chip Enable 2 High	0		0		ns
t_{WLWH}	Write Enable Pulse Width	80		100		ns
t_{E1LE1H}	Chip Enable 1 Low to Chip Enable 1 High	80		130		ns
t_{E2HE2L}	Chip Enable 2 High to Chip Enable 2 Low	80		130		ns
t_{WHAX}	Write Enable High to Address Transition	10		10		ns
t_{E1HAX}	Chip Enable 1 High to Address Transition	10		10		ns
t_{E2LAX}	Chip Enable 2 Low to Address Transition	10		10		ns
t_{DVWH}	Input Valid to Write Enable High	50		70		ns
t_{DVE1H}	Input Valid to Chip Enable 1 High	50		70		ns
t_{DVE2L}	Input Valid to Chip Enable 2 Low	50		70		ns
t_{WHDX}	Write Enable High to Input Transition	5		5		ns
t_{E1HDX}	Chip Enable 1 High to Input Transition	5		5		ns
t_{E2LDX}	Chip Enable 2 Low to Input Transition	5		5		ns
t_{WLQZ}	Write Enable Low to Output Hi-Z		50		70	ns
t_{AVWH}	Address Valid to Write Enable High	80		130		ns
t_{AVE1H}	Address Valid to Chip Enable 1 High	80		130		ns
t_{AVE2L}	Address Valid to Chip Enable 2 Low	80		130		ns
t_{WHQX}	Write Enable High to Output Transition	10		10		ns

Figure 7. Write Enable Controlled, Write AC Waveforms

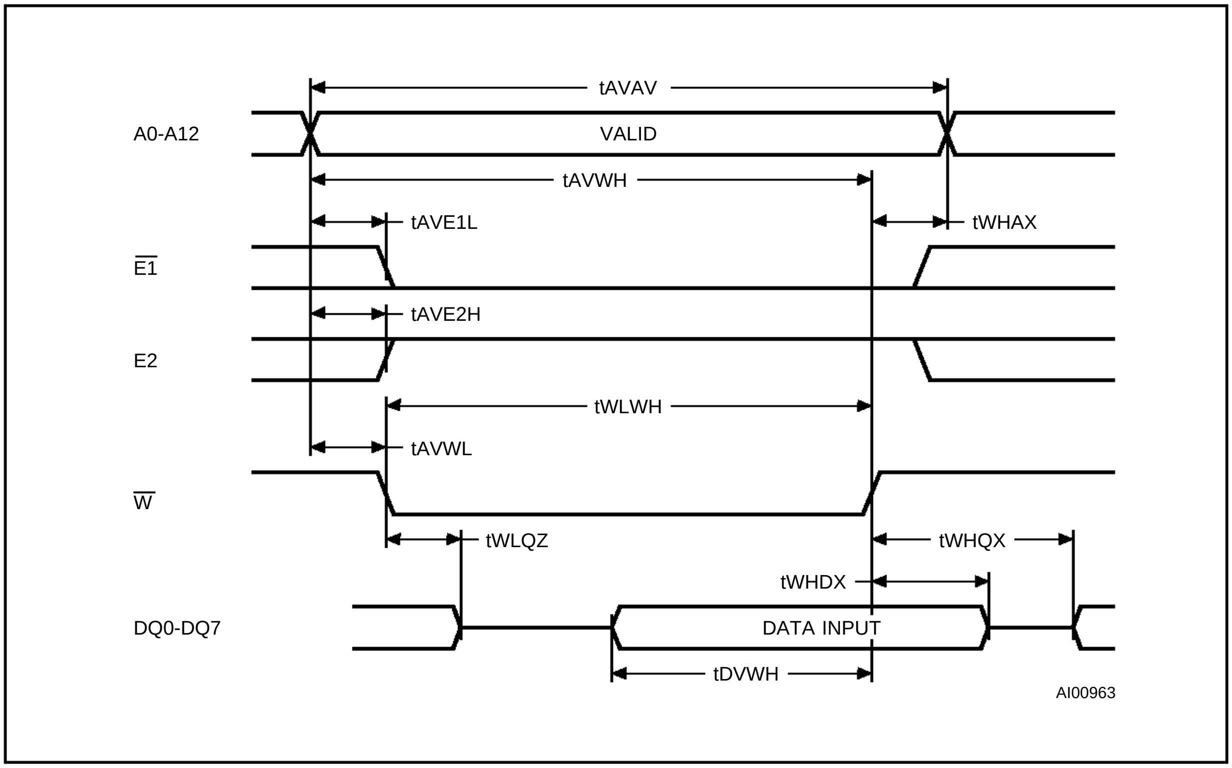
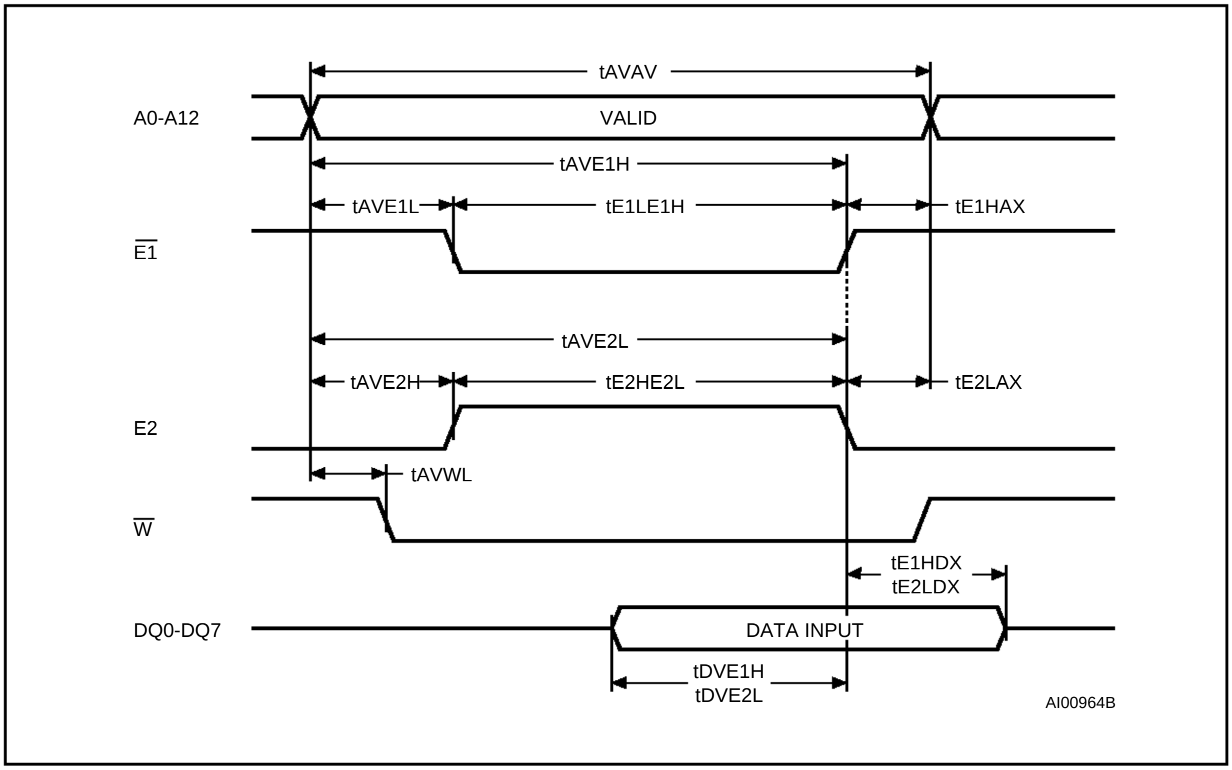


Figure 8. Chip Enable Controlled, Write AC Waveforms



DESCRIPTION (cont'd)

24 hour BCD format. Corrections for 28, 29 (leap year), 30, and 31 day months are made automatically. Byte 1FF8h is the clock control register. This byte controls user access to the clock information and also stores the clock calibration setting.

The eight clock bytes are not the actual clock counters themselves; they are memory locations consisting of BiPORT™ read/write memory cells. The M48T08,18 includes a clock control circuit which updates the clock bytes with current information once per second. The information can be accessed by the user in the same manner as any other location in the static memory array.

The M48T08,18 also has its own Power-fail Detect circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the battery which maintains data and clock operation until valid power returns.

READ MODE

The M48T08,18 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high, $\overline{E1}$ (Chip Enable 1) is low, and E2 (Chip Enable 2) is high. The device architecture allows ripple- through access of data from eight of 65,536 locations in the static storage array. Thus, the unique address specified by the 13 Address Inputs defines which one of the 8,192 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} (Address Access Time) after the last address input signal is stable, providing that the $\overline{E1}$, E2, and $\overline{G}$ access times are also satisfied. If the $\overline{E1}$, E2 and $\overline{G}$ access times are not met, valid data will be available after the latter of the Chip Enable Access Times (t_{E1LQV} or t_{E2HQV}) or Output Enable Access Time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by $\overline{E1}$, E2 and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E1}$, E2 and $\overline{G}$ remain active, output data will remain valid for t_{AXQX} (Output Data Hold Time) but will go indeterminate until the next Address Access.

WRITE MODE

The M48T08,18 is in the Write Mode whenever $\overline{W}$, $\overline{E1}$, and E2 are active. The start of a write is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E1}$, or the rising edge of E2. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E1}$, or the falling edge of E2. The addresses must be held valid throughout the cycle. $\overline{E1}$ or $\overline{W}$ must return high or E2 low for minimum of t_{E1HAX} or t_{E2LAX} from Chip Enable or t_{WHAX} from Write Enable prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} afterward. $\overline{G}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E1}$ and $\overline{G}$ and a high on E2, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

DATA RETENTION MODE

With valid V_{CC} applied, the M48T08,18 operates as a conventional BYTEWIDE static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD}(max), V_{PFD}(min) window. All outputs become high impedance, and all inputs are treated as "don't care."

Note: A power failure during a write cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD}(min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The M48T08,18 may respond to transient noise spikes on V_{CC} that reach into the deselect window during the time the device is sampling V_{CC}. Therefore, decoupling of the power supply lines is recommended.

When V_{CC} drops below V_{SO}, the control circuit switches power to the internal battery which preserves data and powers the clock. The internal button cell will maintain data in the M48T08,18 for an accumulated period of at least 10 years when V_{CC} is less than V_{SO}. As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}. Write protection continues until V_{CC} reaches V_{PFD}(min). $\overline{E1}$ should be kept high or E2 low as V_{CC} rises past V_{PFD}(min) to prevent inadvertent write cycles prior to processor stabilization. Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD}(max).

POWER FAIL INTERRUPT PIN

The M48T08,18 continuously monitors V_{CC}. When V_{CC} falls to the power-fail detect trip point, an interrupt is immediately generated. An internal clock provides a delay of between 10µs and 40µs before automatically deselecting the M48T08,18. The $\overline{INT}$ pin is an open drain output and requires an external pull up resistor, even if the interrupt output function is not being used.

SYSTEM BATTERY LIFE

The useful life of the battery in the M48T08,18 is expected to ultimately come to an end for one of two reasons: either because it has been discharged while providing current to the RAM and clock in the battery back-up mode, or because the effects of aging render the cell useless before it can actually be completely discharged. The two effects are virtually unrelated allowing discharge, or Capacity Consumption, and the effects of aging, or Storage Life, to be treated as two independent but simultaneous mechanisms. The earlier occurring failure mechanism defines the battery system life of the M48T08,18.

Cell Storage Life

Storage life is primarily a function of temperature. Figure 9 illustrates the approximate storage life of the M48T08,18 battery over temperature. The results in Figure 9 are derived from temperature accelerated life test studies performed at SGS-THOMSON. For the purpose of the testing, a cell failure is defined as the inability of a cell stabilized at 25°C to produce a 2.4V closed circuit voltage across a 250 kΩ load resistor. The two lines, $t_{1\%}$ and $t_{50\%}$, represent different failure rate distributions for the cell's storage life. At 70°C, for example, the $t_{1\%}$ line indicates that an M48T08,18 has a 1% chance of having a battery failure 11 years into its life while the $t_{50\%}$ shows the part has a 50% chance of failure at the 20 year mark. The $t_{1\%}$ line represents the practical onset of wear out and can be considered the worst case Storage Life for the cell. The $t_{50\%}$ can be considered the normal or average life.

Calculating Storage Life

The following formula can be used to predict storage life:

$$\frac{1}{\{[(TA1/TT)/SL1]+[(TA2/TT)/SL2]+...+[(TAN/TT)/SLN]\}}$$

where,

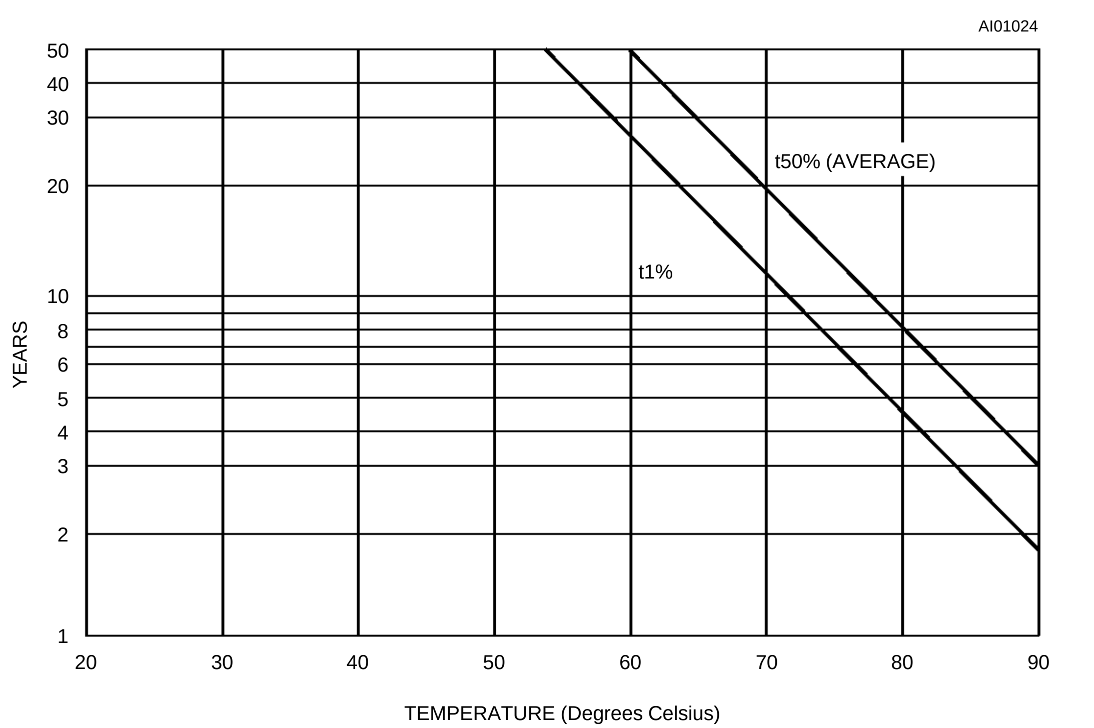
– TA1, TA2, TAN = time at ambient temperature 1, 2, etc.

– TT = total time = TA1+TA2+...+TAN

– SL1, SL2, SLN = storage life at temperature 1, 2, etc.

For example an M48T08,18 is exposed to temperatures of 55°C or less for 8322 hrs/yr, and temperatures greater than 60°C but less than 70°C for the remaining 438 hrs/yr. Reading predicted $t_{1\%}$ values from Figure 9,

Figure 9. Predicted Battery Storage Life versus Temperature



– SL1 = 41 yrs, SL2 = 11.4 yrs
– TT = 8760 hrs/yr
– TA1 = 8322 hrs/yr, TA2 = 438 hrs/yr

Predicted storage life ≥

$$\frac{1}{\{[(8322/8760)/41]+[(431/8760)/11.4]\}}$$

or 36 years.

Cell Capacity Life

The M48T08,18 internal cell has a rated capacity of 50mAh. The device places a nominal RAM and TIMEKEEPER load of less than 520nA at room temperature. At this rate, the capacity consumption life is 50E-3/520E-9 = 96,153 hours or about 11 years. Capacity consumption life can be extended by applying V_{CC} or turning off the clock oscillator prior to system power down.

Calculating Capacity Life

The RAM and TIMEKEEPER load remains relatively constant over the operating temperature range. Thus, worst case cell capacity life is essentially a function of one variable, V_{CC} duty cycle. For example, if the oscillator runs 100% of the time with V_{CC} applied 60% of the time, the capacity consumption life is 10/(1-0.6), or 25 years.

Estimated System Life

Since either storage life or capacity consumption can end the battery's life, the system life is marked by which ever occurs first. In the above example, this would be 25 years.

Reference for System Life

Each M48T08,18 is marked with a nine digit manufacturing date code in the form of H99XXYYZZ. For example, H995B9431 is:

H = fabricated in Carrollton, TX

9 = assembled in Muar, Malaysia,

9 = tested in Muar, Malaysia,

5B = lot designator,

9431 = assembled in the year 1994, work week 31.

CLOCK OPERATIONS

Reading the Clock

Updates to the TIMEKEEPER registers should be halted before clock data is read to prevent reading data in transition. Because the BiPORT TIMEKEEPER cells in the RAM array are only data registers, and not the actual clock counters, updating the registers can be halted without disturbing the clock itself.

Updating is halted when a '1' is written to the READ bit, the seventh bit in the control register. As long as a '1' remains in that position, updating is halted. After a halt is issued, the registers reflect the count; that is, the day, date, and the time that were current at the moment the halt command was issued.

All of the TIMEKEEPER registers are updated simultaneously. A halt will not interrupt an update in progress. Updating is within a second after the bit is reset to a '0'.

Setting the Clock

The eighth bit of the control register is the WRITE bit. Setting the WRITE bit to a '1', like the READ bit, halts updates to the TIMEKEEPER registers. The user can then load them with the correct day, date, and time data in 24 hour BCD format (see Table 10). Resetting the WRITE bit to a '0' then transfers the values of all time registers (1FF9h-1FFFh) to the actual TIMEKEEPER counters and allows normal operation to resume. The FT bit and the bits marked as '0' in Table 10 must be written to '0' to allow for normal TIMEKEEPER and RAM operation.

Stopping and Starting the Oscillator

The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain on the battery. The STOP bit is the MSB of the seconds register. Setting it to a '1' stops the oscillator. The M48T08,18 is shipped from SGS-THOMSON with the STOP bit set to a '1'. When reset to a '0', the M48T08,18 oscillator starts within 1 second.

Calibrating the Clock

The M48T08,18 is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. A typical M48T08,18 is accurate within ±1 minute per month at 25°C without calibration. The devices are tested not to exceed 35 PPM (parts per million) oscillator frequency error at 25°C, which equates to about ± 1.53 minutes per month. Of course the oscillation rate of any crystal changes with temperature. Figure 11 shows the frequency error that can be expected at various temperatures. Most clock chips compensate for crystal frequency and temperature shift error with cumbersome trim capacitors. The M48T08,18 design, however, employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 128 stage, as shown in Figure 10. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five bit Calibration byte found in the Control Register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The Calibration byte occupies the five lower order bits in the Control register. This byte can be set to represent any value between 0 and 31 in binary

CLOCK OPERATIONS (cont'd)

form. The sixth bit is a sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or -2.034 PPM of adjustment per calibration step in the calibration register. Assuming that the oscillator is in fact running at exactly 32,768 Hz, each of the 31 increments in the Calibration byte would represent +10.7 or - 5.35 seconds per month which corresponds to a total range of +5.5 or - 2.75 minutes per month.

Two methods are available for ascertaining how much calibration a given M48T08,18 may require. The first involves simply setting the clock, letting it run for a month and comparing it to a known accurate reference (like WWV broadcasts). While that may seem crude, it allows the designer to give the end user the ability to calibrate his clock as his environment may require, even after the final product is packaged in a non-user serviceable enclosure. All the designer has to do is provide a simple utility that accesses the Calibration byte. The utility could even be menu driven and made foolproof.

The second approach is better suited to a manufacturing environment, and involves the use of some test equipment. When the Frequency Test (FT) bit, the seventh-most significant bit in the Day Register, is set to a '1', and the oscillator is running at 32,768 Hz, the LSB (DQ0) of the Seconds Register will toggle at 512 Hz. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.01024 Hz would indicate a +20 PPM oscillator frequency error, requiring a -10(001010) to be loaded into the Calibration Byte for correction. Note that setting or changing the Calibration Byte does not affect the Frequency test output frequency. The device must be selected and addresses must stable at Address 1FF9h when reading the 512 Hz on DQ0.

The FT bit must be set using the same method used to set the clock, using the Write bit. The LSB of the Seconds Register is monitored by holding the M48T08,18 in an extended read of the Seconds Register, without having the Read bit set. The FT bit MUST be reset to '0' for normal clock operations to resume.

Table 10. Register Map

Address	Data								Function/Range BCD Format	
	D7	D6	D5	D4	D3	D2	D1	D0		
1FFFh	10 Years				Year				Year	00-99
1FFEh	0	0	0	10 M.	Month				Month	01-12
1FFDh	0	0	10 Date		Date				Date	01-31
1FFCh	0	FT	0	0	0	Day			Day	01-07
1FFBh	0	0	10 Hours		Hours				Hour	00-23
1FFAh	0	10 Minutes			Minutes				Minutes	00-59
1FF9h	ST	10 Seconds			Seconds				Seconds	00-59
1FF8h	W	R	S	Calibration					Control	

Keys: **S** = SIGN Bit
FT = FREQUENCY TEST Bit (Set to '0' for normal clock operation)
R = READ Bit
W = WRITE Bit
ST = STOP Bit
0 = Must be set to '0'

Figure 10. Clock Calibration

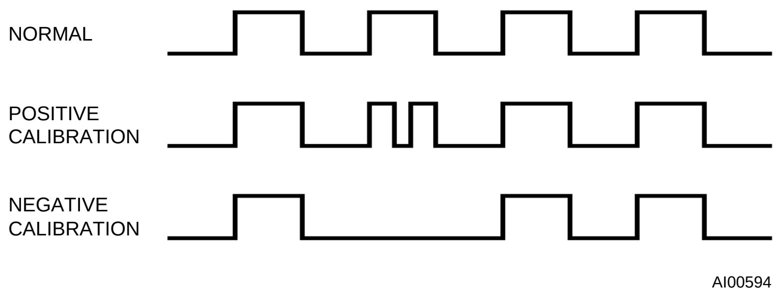
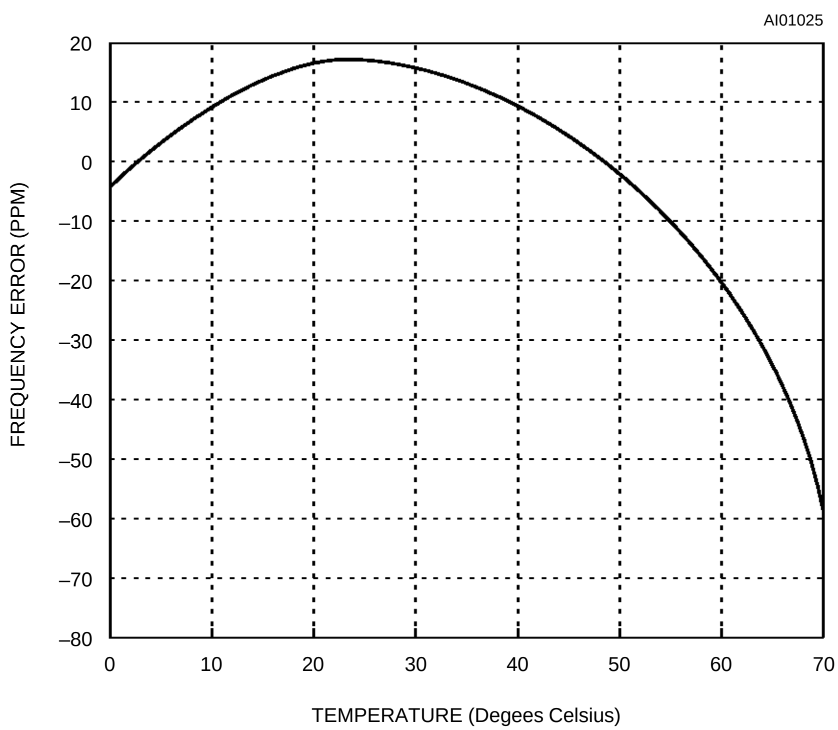


Figure 11. Crystal Frequency Error



ORDERING INFORMATION SCHEME

Example: M48T18 -100 MH 1 TR

Supply Voltage and Write Protect Voltage	Speed	Package	Temp. Range	Shipping Method for SO
08* V_{CC} = 4.75V to 5.5V V_{PFD} = 4.5V to 4.75V	-100 100ns	PC PCDIP28	1 0 to 70 °C	blank Tubes
18 V_{CC} = 4.5V to 5.5V V_{PFD} = 4.2V to 4.5V	-150 150ns	MH SOH28		TR Tape &Reel

Note: 08* CAPHAT package only.

The SO and battery packages are shipped separately in plastic anti-static tubes. The SO package is also available to ship in Tape & Reel form. For the M48T18 28 lead SO, the battery package (i.e. SNAPHAT) part number is "M4T28-BR12SH1".

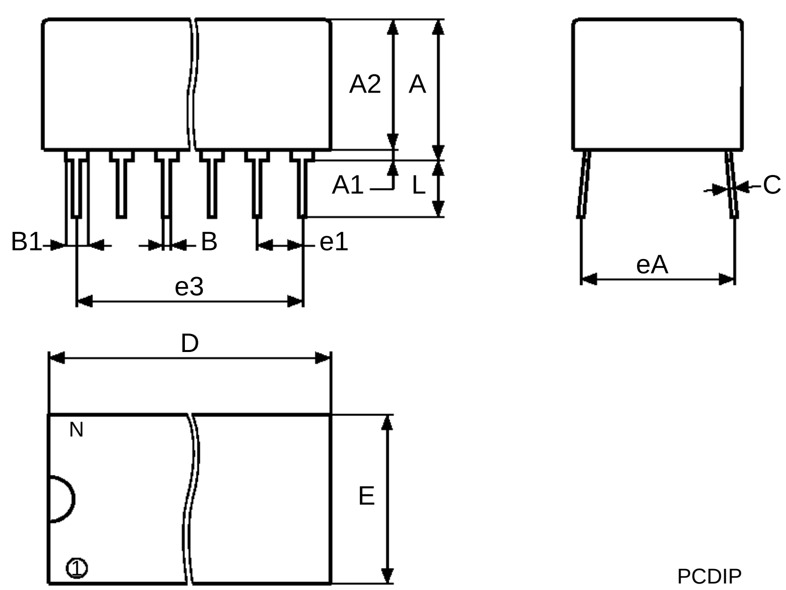
For a list of available options (Supply Voltage, Speed, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

PCDIP28 - 28 pin Plastic DIP, battery CAPHAT

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		8.89	9.65		0.350	0.380
A1		0.38	0.76		0.015	0.030
A2		8.38	8.89		0.330	0.350
B		0.38	0.53		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.31		0.008	0.012
D		39.37	39.88		1.550	1.570
E		17.83	18.34		0.702	0.722
e1		2.29	2.79		0.090	0.110
e3		29.72	36.32		1.170	1.430
eA		15.24	16.00		0.600	0.630
L		3.05	3.81		0.120	0.150
N	28			28		

PCDIP28

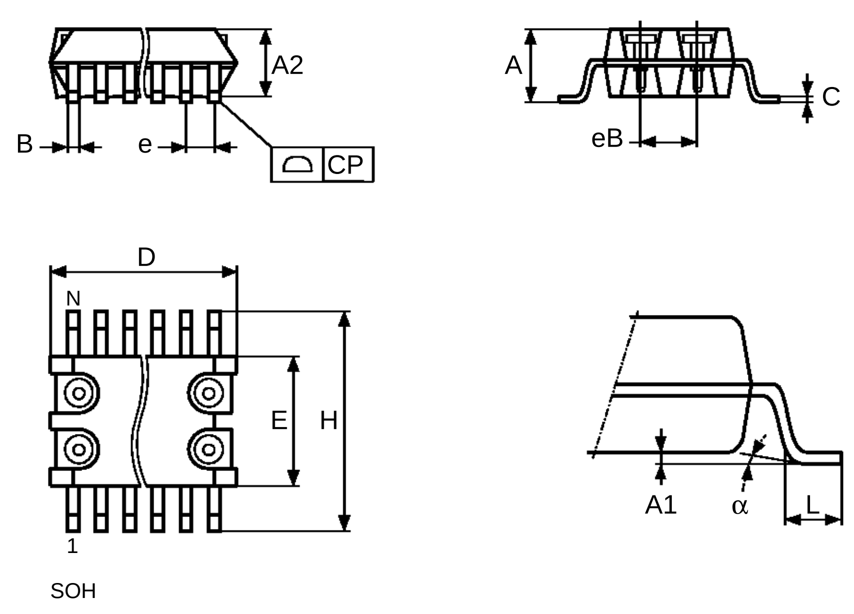


Drawing is not to scale

SOH28 - 28 lead Plastic Small Outline, battery SNAPHAT

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			3.05			0.120
A1		0.05	0.36		0.002	0.014
A2		2.34	2.69		0.092	0.106
B		0.36	0.51		0.014	0.020
C		0.15	0.32		0.006	0.012
D		17.71	18.49		0.697	0.728
E		8.23	8.89		0.324	0.350
e	1.27	–	–	0.050	–	–
eB		3.20	3.61		0.126	0.142
H		11.51	12.70		0.453	0.500
L		0.41	1.27		0.016	0.050
α		0°	8°		0°	8°
N	28			28		
CP			0.10			0.004

SOH28

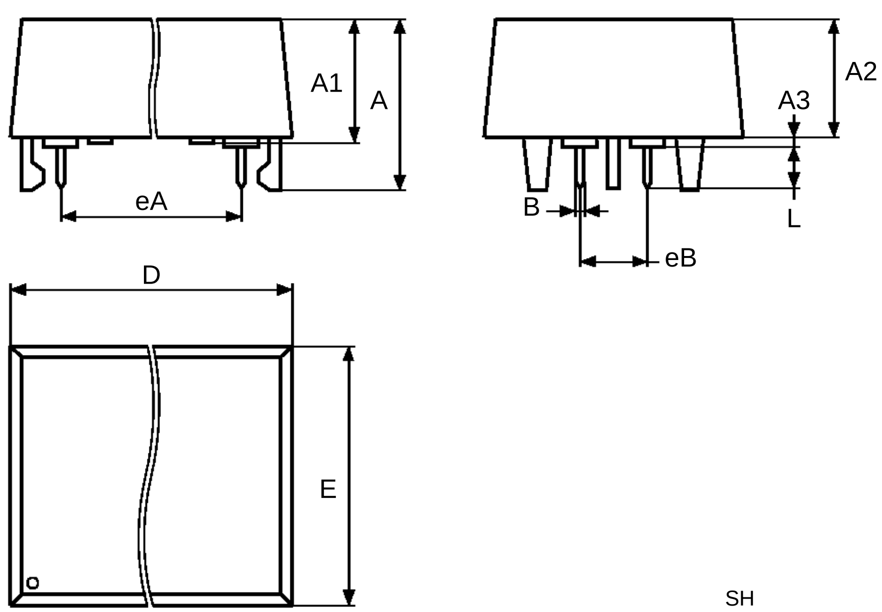


Drawing is not to scale

SH28 - SNAPHAT Housing for 28 lead Plastic Small Outline

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			9.78			0.385
A1		6.73	7.24		0.265	0.285
A2		6.48	6.99		0.255	0.275
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		14.22	14.99		0.560	0.590
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

SH28



Drawing is not to scale

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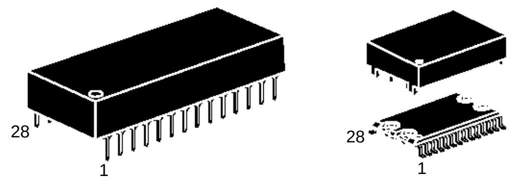
SGS-THOMSON
MICROELECTRONICS

M48Z08
M48Z18

CMOS 8K x 8 ZEROPOWER SRAM

- INTEGRATED ULTRA LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT and BATTERY
- UNLIMITED WRITE CYCLES
- READ CYCLE TIME EQUALS WRITE CYCLE TIME
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- CHOICE of TWO WRITE PROTECT VOLTAGES:
  - M48Z08: $4.5V \leq V_{PFD} \leq 4.75V$
  - M48Z18: $4.2V \leq V_{PFD} \leq 4.5V$
- SELF CONTAINED BATTERY in the CAPHAT DIP PACKAGE
- SMALL OUTLINE PACKAGE PROVIDES DIRECT CONNECTION for a SNAPHAT HOUSING CONTAINING the BATTERY
- SNAPHAT HOUSING (BATTERY) REPLACEABLE
- 11 YEARS of DATA RETENTION in the ABSENCE of POWER
- PIN and FUNCTION COMPATIBLE with the MK48Z08, 18 and JEDEC STANDARD 8K x 8 SRAMs



PCDIP28 (PC)
Battery CAPHAT

SOH28 (MH)
Battery SNAPHAT

DESCRIPTION

The M48Z08,18 ZEOPOWER® RAM is an 8K x 8 non-volatile static RAM which is pin and functional compatible with the MK48Z08,18. The monolithic chip is available in two special packages to provide a highly integrated battery backed-up memory solution.

Table 1. Signal Names

A0-A12	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

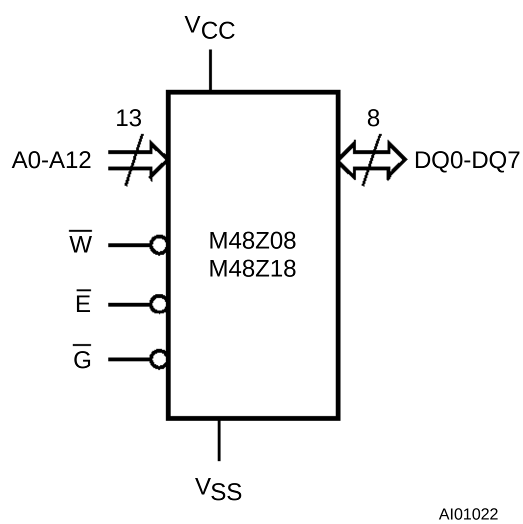
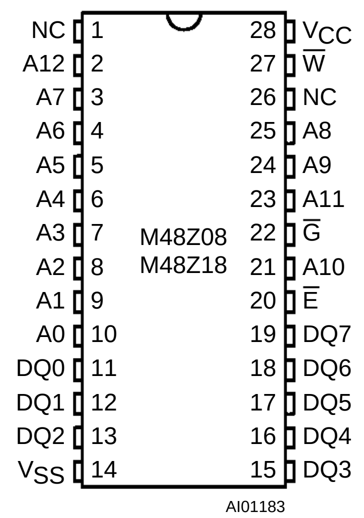
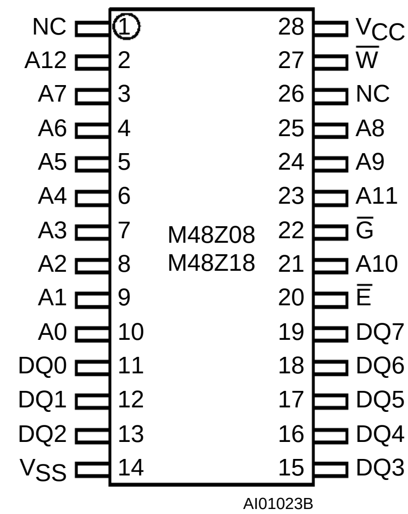


Figure 2A. DIP Pin Connections



Warning: NC = Not Connected

Figure 2B. SO Pin Connections



Warning: NC = Not Connected

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature grade 1 grade 6	0 to 70 –40 to 85	°C
T_{STG}	Storage Temperature (V_{CC} Off)	–40 to 85	°C
V_{IO}	Input or Output Voltages	–0.3 to 7	V
V_{CC}	Supply Voltage	–0.3 to 7	V
I_O	Output Current	20	mA
P_D	Power Dissipation	1	W

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

CAUTION: *Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

Table 3. Operating Modes

Mode	V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.75V to 5.5V or 4.5V to 5.5V	V_{IH}	X	X	High Z	Standby
Write		V_{IL}	X	V_{IL}	D_{IN}	Active
Read		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Read		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min)	X	X	X	High Z	CMOS Standby
Deselect	$\leq V_{SO}$	X	X	X	High Z	Battery Back-up Mode

Note: X = V_{IH} or V_{IL}

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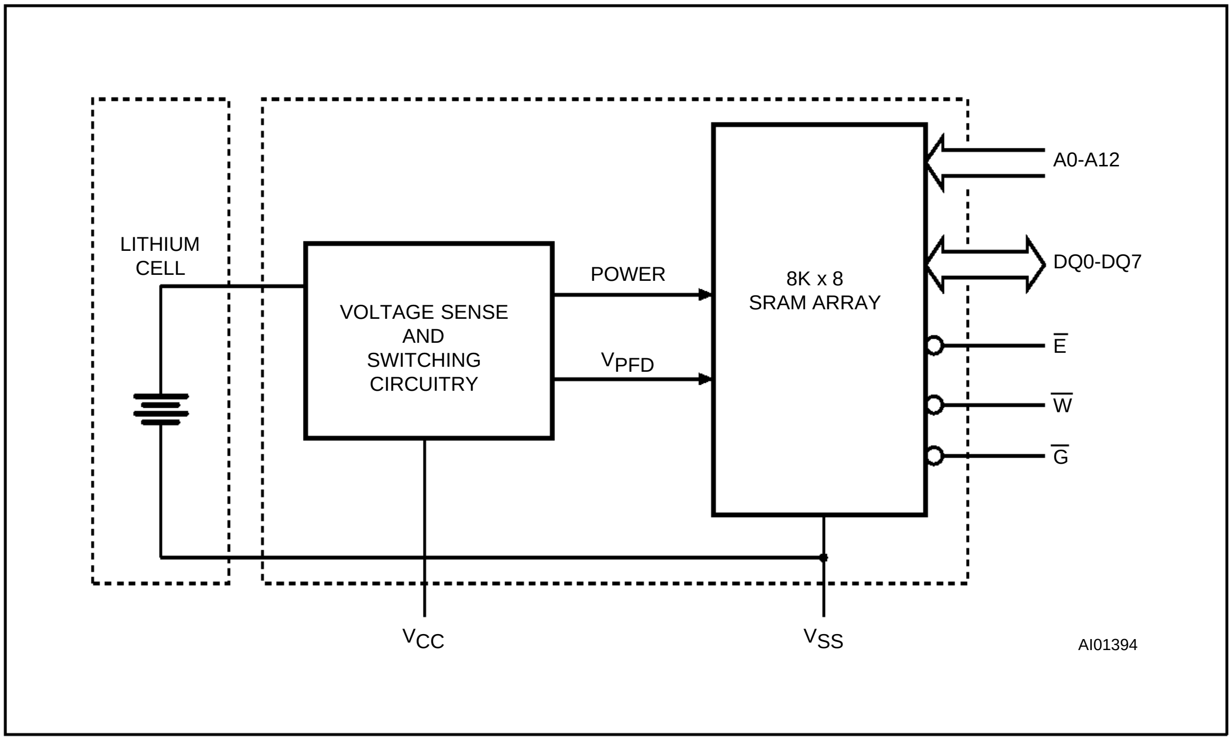
Figure 3. Block Diagram



DESCRIPTION (cont'd)

The M48Z08,18 is a non-volatile pin and function equivalent to any JEDEC standard 8K x 8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The 28 pin 600mil DIP CAPHAT™ houses the M48Z08,18 silicon with a long life lithium button cell in a single package.

The 28 pin 330mil SO provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT™ housing containing the battery. The unique design allows the SNAPHAT battery package to be mounted on top of the SO package after the completion of the surface mount process. Insertion of the SNAPHAT housing after reflow prevents potential battery damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is keyed to prevent reverse insertion.

The SO and battery packages are shipped separately in plastic anti-static tubes. The SO package is also available to ship in Tape & Reel form.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

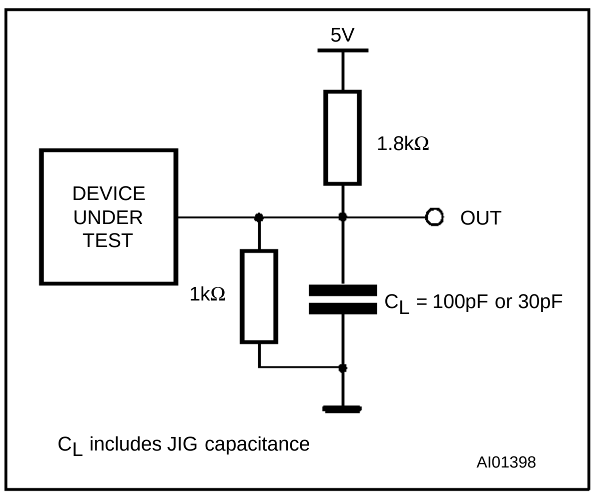


Table 4. Capacitance [1] (T_A = 25 °C)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		10	pF
C_{IO} [2]	Input / Output Capacitance	V_{OUT} = 0V		10	pF

Notes: 1. Effective capacitance calculated from the equation C = IΔt/ΔV with ΔV = 3V and power supply at 5V.
2. Outputs deselected

Table 5. DC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±5	µA
I_{CC}	Supply Current	Outputs open		80	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		3	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} - 0.2V$		3	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4		V

Table 6. Power Down/Up Trip Points DC Characteristics [1] (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage (M48Z08)	4.5	4.6	4.75	V
V_{PFD}	Power-fail Deselect Voltage (M48Z18)	4.2	4.3	4.5	V
V_{SO}	Battery Back-up Switchover Voltage		3.0		V
t_{DR}	Expected Data Retention Time	11			YEARS

Note: 1. All voltages referenced to V_{SS}.

DESCRIPTION (cont'd)

For the 28 lead SO, the battery package (i.e. SNAPHAT) part number is "M4Z28-BR00SH1".

The M48Z08,18 also has its own Power-fail Detect circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition.

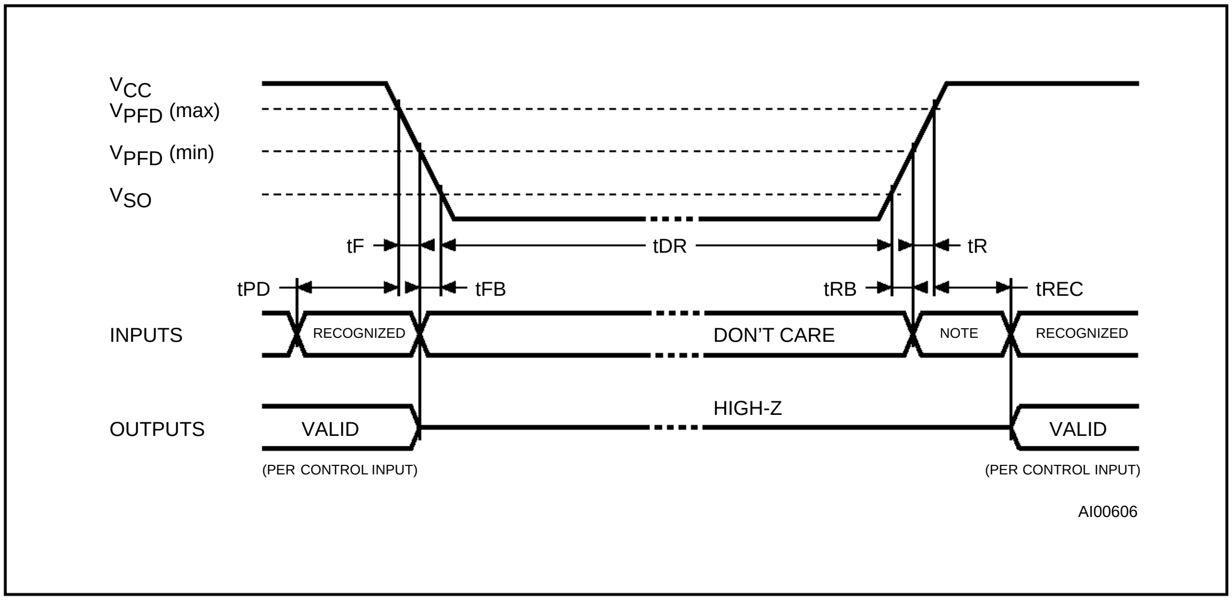
When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the battery which maintains data until valid power returns.

Table 7. Power Down/Up Mode AC Characteristics (T_A = 0 to 70°C)

Symbol	Parameter	Min	Max	Unit
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0		µs
t_F (1)	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs
t_{FB} (2)	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs
t_R	V_{PFD}(min) to V_{PFD} (max) V_{CC} Rise Time	0		µs
t_{RB}	V_{SO} to V_{PFD} (min) V_{CC} Rise Time	1		µs
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} after Power Up	1		ms

Notes: 1. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).
2. V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.

Figure 5. Power Down/Up Mode AC Waveforms



Note: Inputs may or may not be recognized at this time. Caution should be taken to keep $\overline{E}$ high as V_{CC} rises past V_{PFD}(min). Some systems may performs inadvertent write cycles after V_{CC} rises above V_{PFD}(min) but before normal system operations begins. Even though a power on reset is being applied to the processor a reset condition may not occur until after the system clock is running.

Table 8. Read Mode AC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48Z08 / 18 -100 Min	M48Z08 / 18 -100 Max	Unit
t_{AVAV}	Read Cycle Time	100		ns
t_{AVQV} (1)	Address Valid to Output Valid		100	ns
t_{ELQV} (1)	Chip Enable Low to Output Valid		100	ns
t_{GLQV} (1)	Output Enable Low to Output Valid		50	ns
t_{ELQX} (2)	Chip Enable Low to Output Transition	10		ns
t_{GLQX} (2)	Output Enable Low to Output Transition	5		ns
t_{EHQZ} (2)	Chip Enable High to Output Hi-Z		50	ns
t_{GHQZ} (2)	Output Enable High to Output Hi-Z		40	ns
t_{AXQX} (1)	Address Transition to Output Transition	5		ns

Notes: 1. C_L = 100pF (see Figure 4).
2. C_L = 30pF (see Figure 4).

Figure 6. Read Mode AC Waveforms

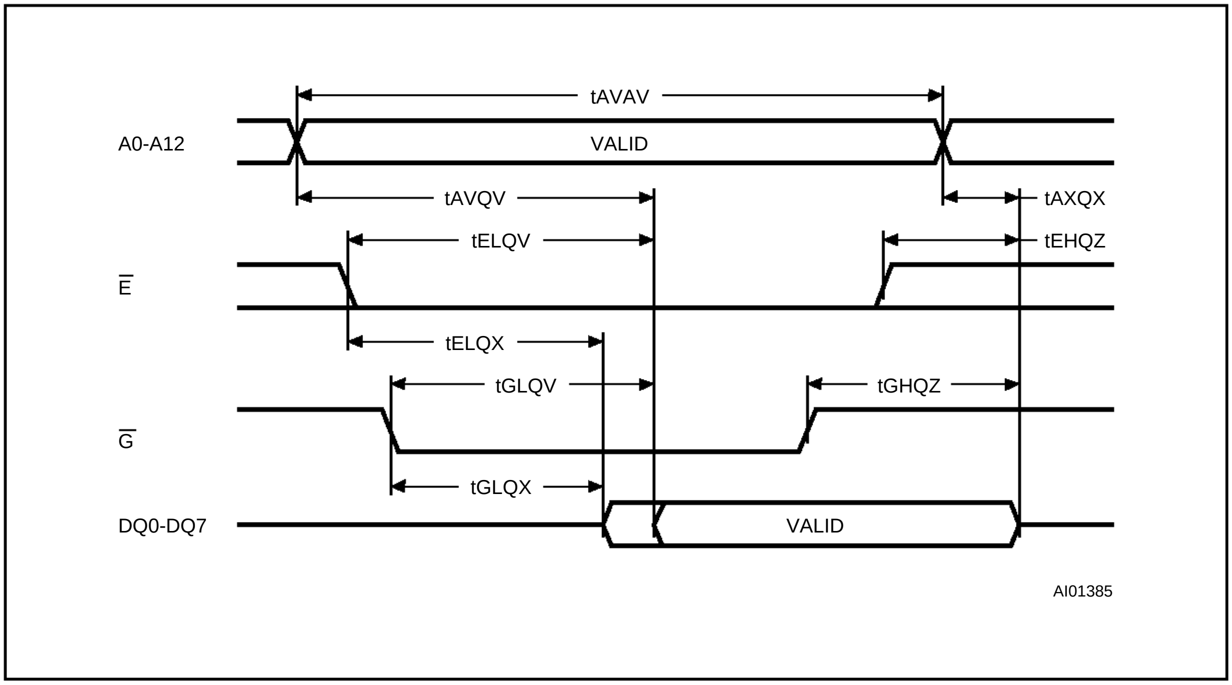


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Table 9. Write Mode AC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48Z08 / 18 -100 Min	M48Z08 / 18 -100 Max	Unit
t_{AVAV}	Write Cycle Time	100		ns
t_{AVWL}	Address Valid to Write Enable Low	0		ns
t_{AVEL}	Address Valid to Chip Enable Low	0		ns
t_{WLWH}	Write Enable Pulse Width	80		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	80		ns
t_{WHAX}	Write Enable High to Address Transition	10		ns
t_{EHAX}	Chip Enable High to Address Transition	10		ns
t_{DVWH}	Input Valid to Write Enable High	50		ns
t_{DVEH}	Input Valid to Chip Enable High	30		ns
t_{WHDX}	Write Enable High to Input Transition	5		ns
t_{E1HDX}	Chip Enable High to Input Transition	5		ns
t_{WLQZ} (1, 2)	Write Enable Low to Output Hi-Z		50	ns
t_{AVWH}	Address Valid to Write Enable High	80		ns
t_{AVEH}	Address Valid to Chip Enable High	80		ns
t_{WHQX} (1, 2)	Write Enable High to Output Transition	10		ns

Notes: 1. C_L = 30pF (see Figure 4).
2. If $\overline{E}$ goes low simultaneously with $\overline{W}$ going low, the outputs remain in the high impedance state.

READ MODE

The M48Z08,18 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low. The device architecture allows ripple- through access of data from eight of 65,536 locations in the static storage array. Thus, the unique address specified by the 13 Address Inputs defines which one of the 8,192 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} (Address Access Time) after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the latter of the Chip Enable Access Time (t_{ELQV}) or Output Enable Access Time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain active, output data will remain valid for t_{AXQX} (Output Data Hold Time) but will go indeterminate until the next Address Access.

WRITE MODE

The M48Z08,18 is in the Write Mode whenever $\overline{W}$ and $\overline{E}$ are active. The start of a write is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$.

A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high of t_{EHAX} from Chip Enable or t_{WHAX} from Write Enable prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} afterward. $\overline{G}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

Figure 7. Write Enable Controlled, Write AC Waveforms

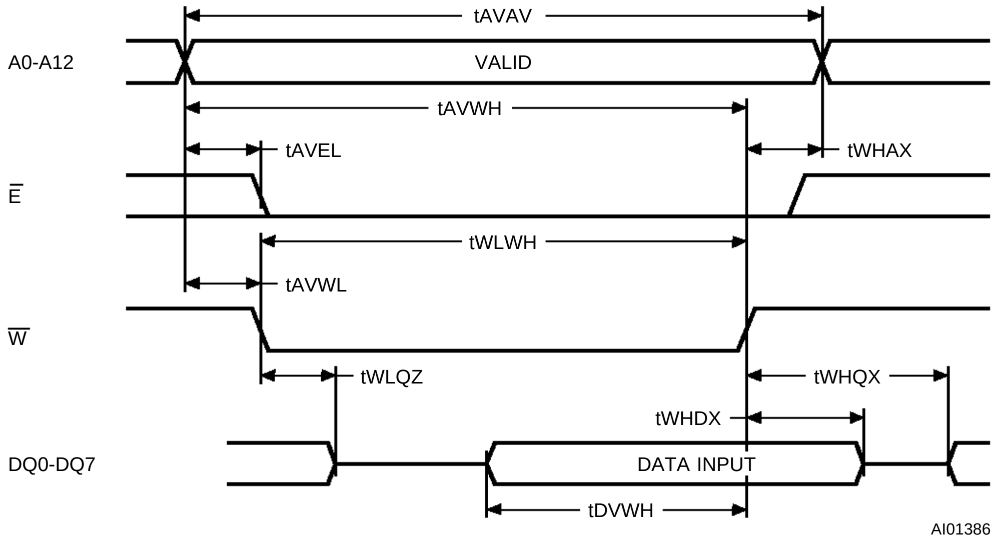
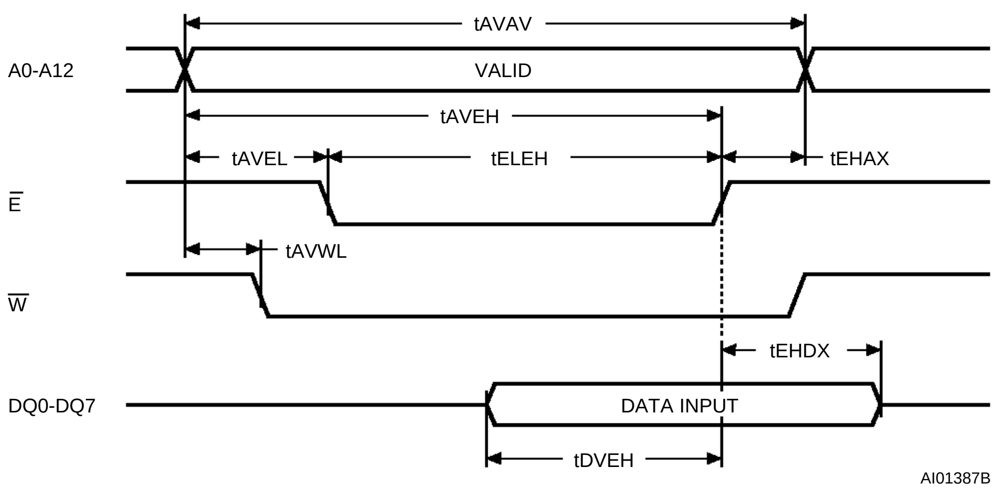


Figure 8. Chip Enable Controlled, Write AC Waveforms



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DATA RETENTION MODE

With valid V_{CC} applied, the M48Z08,18 operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD}(max), V_{PFD}(min) window. All outputs become high impedance, and all inputs are treated as "don't care."

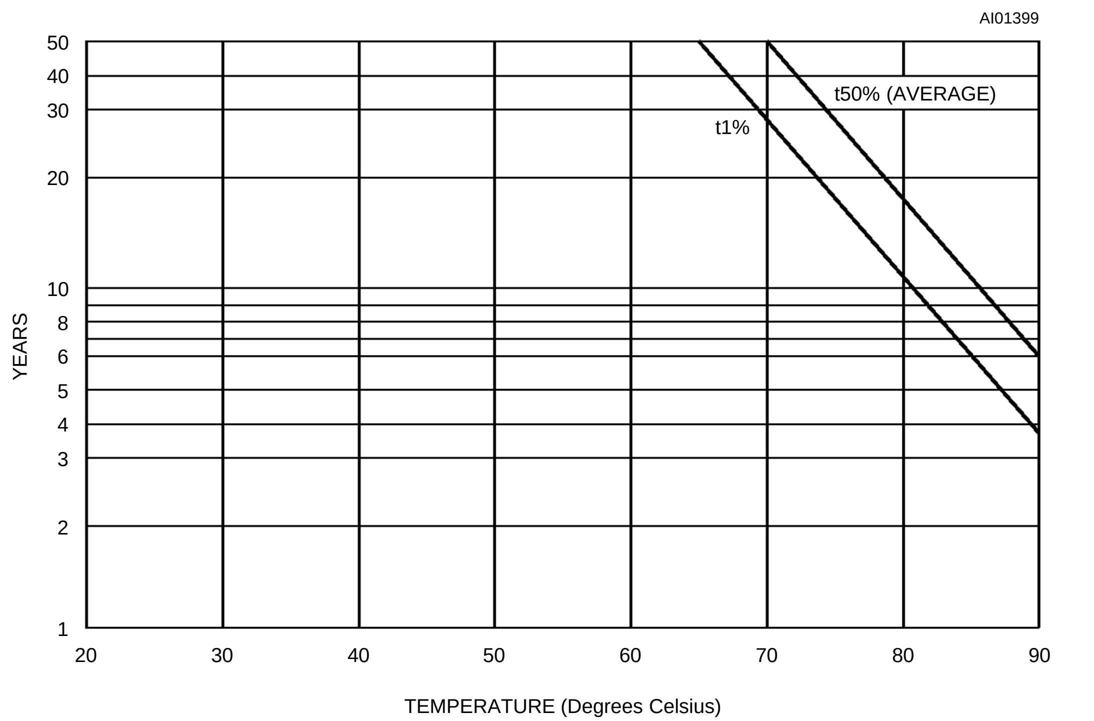
Note: A power failure during a write cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD}(min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The M48Z08,18 may respond to transient noise spikes on V_{CC} that reach into the deselect window during the time the device is sampling V_{CC}. Therefore, decoupling of the power supply lines is recommended.

When V_{CC} drops below V_{SO}, the control circuit switches power to the internal battery which preserves data and powers the clock. The internal button cell will maintain data in the M48Z08,18 for an accumulated period of at least 10 years when V_{CC} is less than V_{SO}. As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}. Write protection continues until V_{CC} reaches V_{PFD}(min). $\overline{E}$ should be kept high as V_{CC} rises past V_{PFD}(min) to prevent inadvertent write cycles prior to processor stabilization. Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD}(max).

SYSTEM BATTERY LIFE

The useful life of the battery in the M48Z08,18 is expected to ultimately come to an end for one of two reasons: either because it has been discharged while providing current to the RAM in the battery back-up mode, or because the effects of aging render the cell useless before it can actually be completely discharged. The two effects are virtually unrelated allowing discharge, or Capacity Consumption, and the effects of aging, or Storage Life, to be treated as two independent but simultaneous mechanisms. The earlier occurring failure mechanism defines the battery system life of the M48Z08,18.

Figure 9. Predicted Battery Storage Life versus Temperature



Cell Storage Life

Storage life is primarily a function of temperature. Figure 9 illustrates the approximate storage life of the M48Z08,18 battery over temperature. The results in Figure 9 are derived from temperature accelerated life test studies performed at SGS-THOMSON. For the purpose of the testing, a cell failure is defined as the inability of a cell stabilized at 25°C to produce a 2.4V closed circuit voltage across a 250 kΩ load resistor. The two lines, $t_{1\%}$ and $t_{50\%}$, represent different failure rate distributions for the cell's storage life. At 70°C, for example, the $t_{1\%}$ line indicates that an M48Z08,18 has a 1% chance of having a battery failure 28 years into its life while the $t_{50\%}$ shows the part has a 50% chance of failure at the 50 year mark. The $t_{1\%}$ line represents the practical onset of wear out and can be considered the worst case Storage Life for the cell. The $t_{50\%}$ can be considered the normal or average life.

Calculating Storage Life

The following formula can be used to predict storage life:

$$\frac{1}{\{[(TA1/TT)/SL1]+[(TA2/TT)/SL2]+...+[(TAN/TT)/SLN]\}}$$

where,

– TA1, TA2, TAN = time at ambient temperature 1, 2, etc.

– TT = total time = TA1+TA2+...+TAN

– SL1, SL2, SLN = storage life at temperature 1, 2, etc.

For example an M48Z08,18 is exposed to temperatures of 55°C or less for 8322 hrs/yr, and temperatures greater than 60°C but less than 70°C for the remaining 438 hrs/yr. Reading predicted $t_{1\%}$ values from Figure 9,

– SL1 ≅ 200 yrs, SL2 = 28 yrs

– TT = 8760 hrs/yr

– TA1 = 8322 hrs/yr, TA2 = 438 hrs/yr

Predicted storage life ≥

$$\frac{1}{\{[(8322/8760)/200]+[(431/8760)/28]\}}$$

or 154 years.

As can been seen from these calculations and the results, the expected lifetime of the M48Z08, 18 should exced most system requirements.

Estimated System Life

Since either storage life or capacity consumption can end the battery's life, the system life is marked by which ever occurs first.

Reference for System Life

Each M48Z08,18 is marked with a nine digit manufacturing date code in the form of H99XXYYZZ. For example, H995B9431 is:

H = fabricated in Carrollton, TX

9 = assembled in Muar, Malaysia,

9 = tested in Muar, Malaysia,

5B = lot designator,

9431 = assembled in the year 1994, work week 31.

ORDERING INFORMATION SCHEME

Example: M48Z18 -100 MH 1 TR

Supply Voltage and Write Protect Voltage	Speed	Package	Temp. Range	Shipping Method for SO
08* V_{CC} = 4.75V to 5.5V V_{PFD} = 4.5V to 4.75V	-100 100ns	PC PCDIP28	1 0 to 70 °C	blank Tubes
18 V_{CC} = 4.5V to 5.5V V_{PFD} = 4.2V to 4.5V		MH SOH28	6** –40 to 85 °C	TR Tape &Reel

Notes: 08* CAPHAT package only.
6** Temperature range available for M48Z18 product only.

The SO and battery packages are shipped separately in plastic anti-static tubes. The SO package is also available to ship in Tape & Reel form. For the M48T18 28 lead SO, the battery package (i.e. SNAPHAT) part number is ”M4Z28-BR00SH1”.

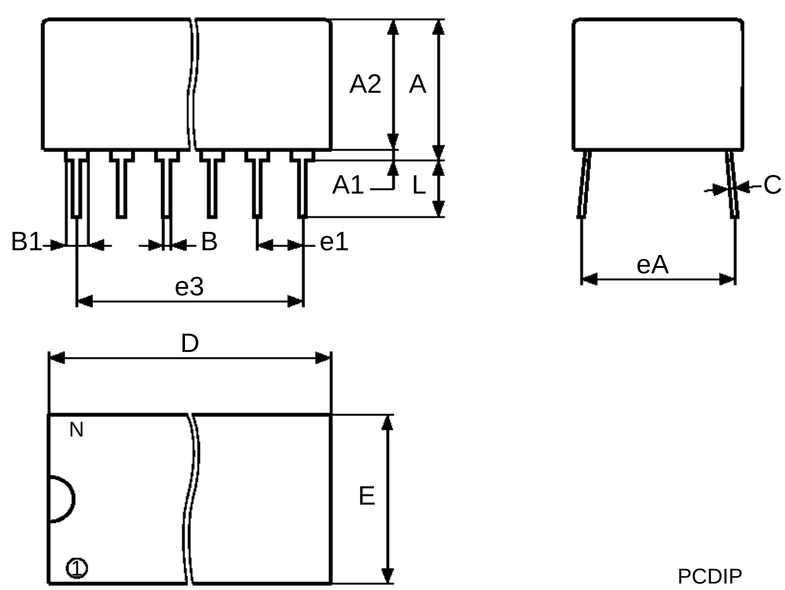
For a list of available options (Supply Voltage, Speed, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

PCDIP28 - 28 pin Plastic DIP, battery CAPHAT

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		8.89	9.65		0.350	0.380
A1		0.38	0.76		0.015	0.030
A2		8.38	8.89		0.330	0.350
B		0.38	0.53		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.31		0.008	0.012
D		39.37	39.88		1.550	1.570
E		17.83	18.34		0.702	0.722
e1		2.29	2.79		0.090	0.110
e3		29.72	36.32		1.170	1.430
eA		15.24	16.00		0.600	0.630
L		3.05	3.81		0.120	0.150
N	28			28		

PCDIP28



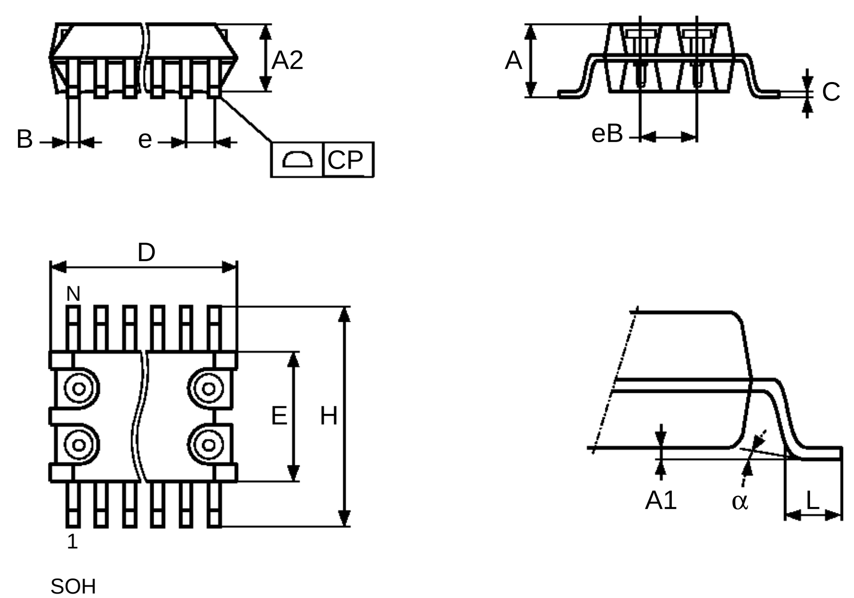
Drawing is not to scale

SGS-THOMSON MICROELECTRONICS

SOH28 - 28 lead Plastic Small Outline, battery SNAPHAT

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			3.05			0.120
A1		0.05	0.36		0.002	0.014
A2		2.34	2.69		0.092	0.106
B		0.36	0.51		0.014	0.020
C		0.15	0.32		0.006	0.012
D		17.71	18.49		0.697	0.728
E		8.23	8.89		0.324	0.350
e	1.27	–	–	0.050	–	–
eB		3.20	3.61		0.126	0.142
H		11.51	12.70		0.453	0.500
L		0.41	1.27		0.016	0.050
α		0°	8°		0°	8°
N	28			28		
CP			0.10			0.004

SOH28



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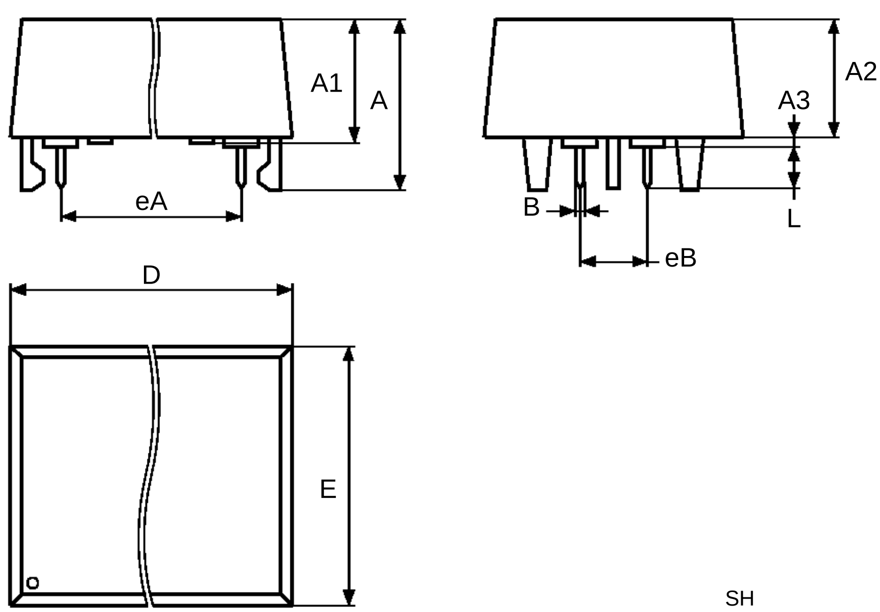
SH28 - SNAPHAT Housing for 28 lead Plastic Small Outline

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			9.78			0.385
A1		6.73	7.24		0.265	0.285
A2		6.48	6.99		0.255	0.275
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		14.22	14.99		0.560	0.590
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

SH28



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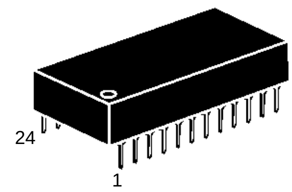
CMOS 2K x 8 TIMEKEEPER SRAM

- INTEGRATED ULTRA LOW POWER SRAM, REAL TIME CLOCK and POWER-FAIL CONTROL CIRCUIT
- BYTEWIDE RAM-LIKE CLOCK ACCESS
- BCD CODED YEAR, MONTH, DAY, DATE, HOURS, MINUTES and SECONDS
- CLOCK ACCURACY of ± 1 MINUTE a MONTH, @ 25°C
- SOFTWARE CONTROLLED CLOCK CALIBRATION for HIGH ACCURACY APPLICATIONS
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- CHOICE of TWO WRITE PROTECT VOLTAGES:
  – M48T02: $4.5V \leq V_{PFD} \leq 4.75V$
  – M48T12: $4.2V \leq V_{PFD} \leq 4.5V$
- SELF CONTAINED BATTERY and CRYSTAL in the CAPHAT DIP PACKAGE
- 10 YEARS of DATA RETENTION and CLOCK OPERATION in the ABSENCE of POWER
- PIN and FUNCTION COMPATIBLE with JEDEC STANDARD 2K x 8 SRAMs



PCDIP24 (PC)
Battery CAPHAT

DESCRIPTION

The M48T02,12 TIMEKEEPER™ RAM is a 2K x 8 non-volatile static RAM and real time clock which is pin and functional compatible with the MK48T02,12.

Table 1. Signal Names

A0-A10	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

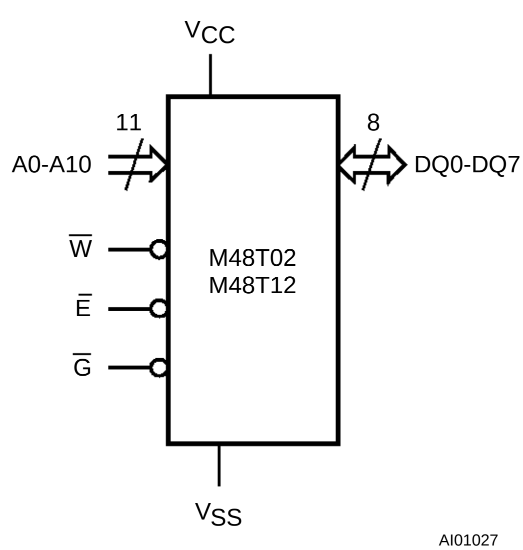


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature (V_{CC} Off, Oscillator Off)	–40 to 85	°C
V_{IO}	Input or Output Voltages	–0.3 to 7	V
V_{CC}	Supply Voltage	–0.3 to 7	V
I_O	Output Current	20	mA
P_D	Power Dissipation	1	W

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

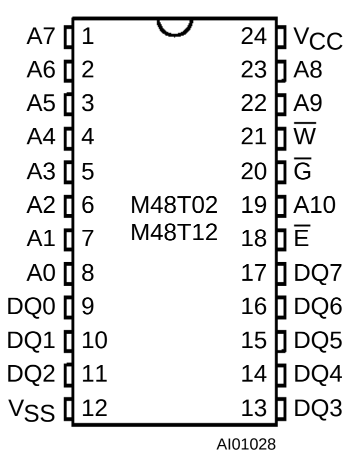
CAUTION: *Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

Table 3. Operating Modes

Mode	V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.75V to 5.5V or 4.5V to 5.5V	V_{IH}	X	X	High Z	Standby
Write		V_{IL}	X	V_{IL}	D_{IN}	Active
Read		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Read		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min)	X	X	X	High Z	CMOS Standby
Deselect	$\leq V_{SO}$	X	X	X	High Z	Battery Back-up Mode

Note: X = V_{IH} or V_{IL}

Figure 2. DIP Pin Connections



DESCRIPTION (cont'd)

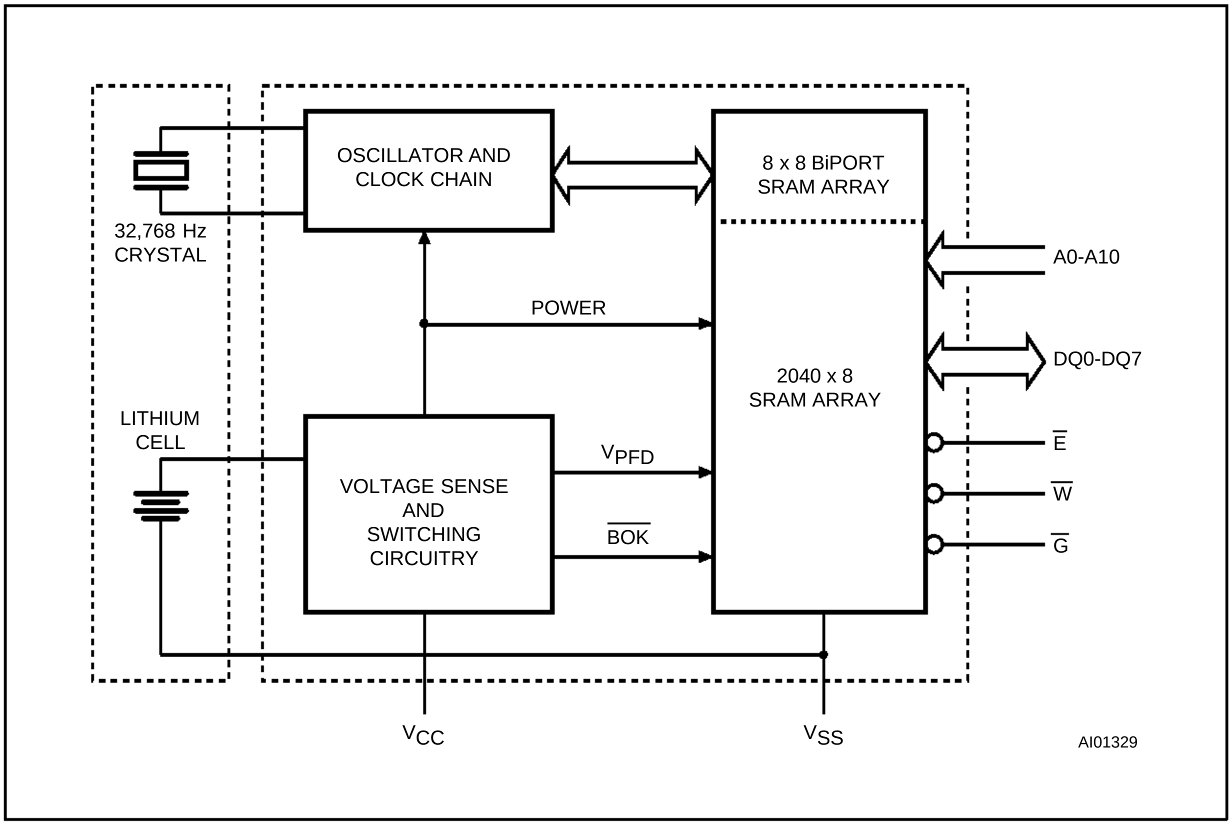
A special 24 pin 600mil DIP CAPHAT™ package houses the M48T02,12 silicon with a quartz crystal and a long life lithium button cell to form a highly integrated battery backed-up memory and real time clock solution.

The M48T02,12 button cell has sufficient capacity and storage life to maintain data and clock functionality for an accumulated time period of at least 10 years in the absence of power over the operating temperature range.

The M48T02,12 is a non-volatile pin and function equivalent to any JEDEC standard 2K x 8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

As Figure 3 shows, the static memory array and the quartz controlled clock oscillator of the M48T02,12 are integrated on one silicon chip. The two circuits are interconnected at the upper eight memory locations to provide user accessible BYTEWIDE™

Figure 3. Block Diagram



clock information in the bytes with addresses 7F8h-7FFh. The clock locations contain the year, month, date, day, hour, minute, and second in 24 hour BCD format. Corrections for 28, 29 (leap year), 30, and 31 day months are made automatically. Byte 7F8h is the clock control register. This byte controls user access to the clock information and also stores the clock calibration setting.

The eight clock bytes are not the actual clock counters themselves; they are memory locations consisting of BiPORT™ read/write memory cells. The M48T02,12 includes a clock control circuit which updates the clock bytes with current information once per second. The information can be accessed by the user in the same manner as any other location in the static memory array.

The M48T02,12 also has its own Power-fail Detect circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the battery which maintains data and clock operation until valid power returns.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0.6V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.2V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

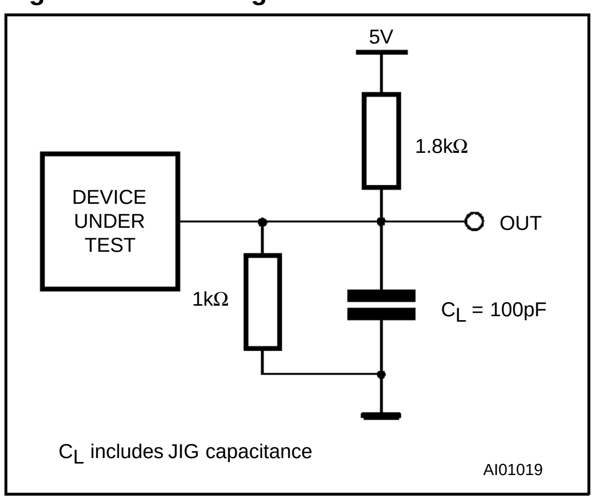


Table 4. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		10	pF
C_{IO} (2)	Input / Output Capacitance	V_{OUT} = 0V		10	pF

Notes: 1. Effective capacitance calculated from the equation C = IΔt/ΔV with ΔV = 3V and power supply at 5V.
2. Outputs deselected

Table 5. DC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI} (1)	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±1	µA
I_{LO} (1)	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±5	µA
I_{CC}	Supply Current	Outputs open		80	mA
I_{CC1} (2)	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		3	mA
I_{CC2} (2)	Supply Current (Standby) CMOS	$\overline{E}$ = V_{CC} – 0.2V		3	mA
V_{IL} (3)	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4		V

Notes: 1. Outputs Deselected.
2. Measured with Control Bits set as follows: R = '1'; W, ST, KS, FT = '0'.
3. Negative spikes of –1V allowed for up to 10ns once per Cycle.

Table 6. Power Down/Up Trip Points DC Characteristics (1) (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage (M48T02)	4.5	4.6	4.75	V
V_{PFD}	Power-fail Deselect Voltage (M48T12)	4.2	4.3	4.5	V
V_{SO}	Battery Back-up Switchover Voltage		3.0		V
t_{DR} (2)	Expected Data Retention Time	10			YEARS

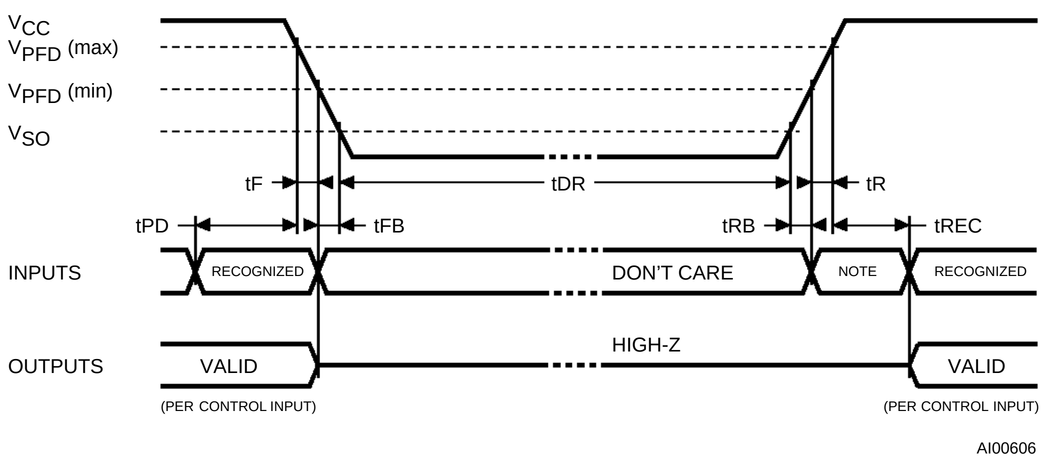
Notes: 1. All voltages referenced to V_{SS}.
2. @ 25°C

Table 7. Power Down/Up Mode AC Characteristics (T_A = 0 to 70°C)

Symbol	Parameter	Min	Max	Unit
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0		µs
t_F (1)	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs
t_{FB} (2)	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs
t_R	V_{PFD}(min) to V_{PFD} (max) V_{CC} Rise Time	0		µs
t_{RB}	V_{SO} to V_{PFD} (min) V_{CC} Rise Time	1		µs
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} after Power Up	2		ms

Notes: 1. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 50 µs after V_{CC} passes V_{PFD} (min).
2. V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.

Figure 5. Power Down/Up Mode AC Waveforms



Note: Inputs may or may not be recognized at this time. Caution should be taken to keep $\overline{E}$ high as V_{CC} rises past V_{PFD}(min). Some systems may performs inadvertent write cycles after V_{CC} rises above V_{PFD}(min) but before normal system operations begins. Even though a power on reset is being applied to the processor a reset condition may not occur until after the system clock is running.

Table 8. Read Mode AC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48T02 / 12						Unit
		-120		-150		-200		
		Min	Max	Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	120		150		200		ns
t_{AVQV}	Address Valid to Output Valid		120		150		200	ns
t_{ELQV}	Chip Enable Low to Output Valid		120		150		200	ns
t_{GLQV}	Output Enable Low to Output Valid		75		75		80	ns
t_{ELQX}	Chip Enable Low to Output Transition	10		10		10		ns
t_{GLQX}	Output Enable Low to Output Transition	5		5		5		ns
t_{EHQZ}	Chip Enable High to Output Hi-Z		30		35		40	ns
t_{GHQZ}	Output Enable High to Output Hi-Z		30		35		40	ns
t_{AXQX}	Address Transition to Output Transition	5		5		5		ns

Figure 6. Read Mode AC Waveforms

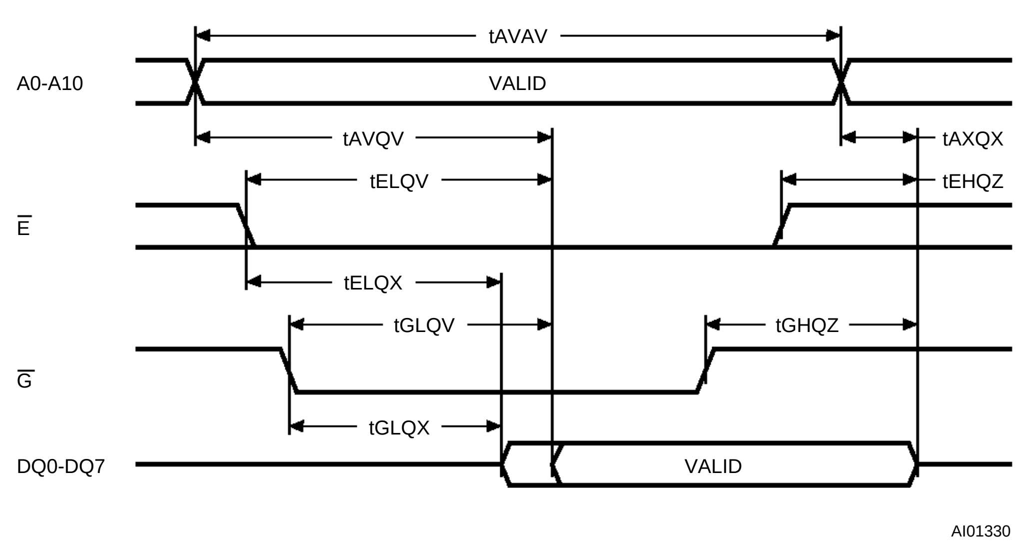


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Table 9. Write Mode AC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48T02 / 12						Unit
		-120		-150		-200		
		Min	Max	Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	120		150		200		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		0		ns
t_{AVEL}	Address Valid to Chip Enable Low	0		0		0		ns
t_{WLWH}	Write Enable Pulse Width	75		90		120		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	75		90		120		ns
t_{WHAX}	Write Enable High to Address Transition	10		10		10		ns
t_{EHAX}	Chip Enable High to Address Transition	10		10		10		ns
t_{DVWH}	Input Valid to Write Enable High	35		40		60		ns
t_{DVEH}	Input Valid to Chip Enable High	35		40		60		ns
t_{WHDX}	Write Enable High to Input Transition	5		5		5		ns
t_{EHDX}	Chip Enable High to Input Transition	5		5		5		ns
t_{WLQZ}	Write Enable Low to Output Hi-Z		40		50		60	ns
t_{AVWH}	Address Valid to Write Enable High	90		120		140		ns
t_{AVEH}	Address Valid to Chip Enable High	90		120		140		ns
t_{WHQX}	Write Enable High to Output Transition	10		10		10		ns

READ MODE

The M48T02,12 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low. The device architecture allows ripple-through access of data from eight of 16,384 locations in the static storage array. Thus, the unique address specified by the 11 Address Inputs defines which one of the 2,048 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} (Address Access Time) after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the latter of the Chip Enable Access Time (t_{ELQV}) or Output Enable Access Time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain active, output data will remain valid for t_{AXQX} (Output Data Hold Time) but will go indeterminate until the next Address Access.

WRITE MODE

The M48T02,12 is in the Write Mode whenever $\overline{W}$ and $\overline{E}$ are active. The start of a write is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for minimum of t_{EHAX} from Chip Enable or t_{WHAX} from Write Enable prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} afterward. $\overline{G}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

Figure 7. Write Enable Controlled, Write AC Waveforms

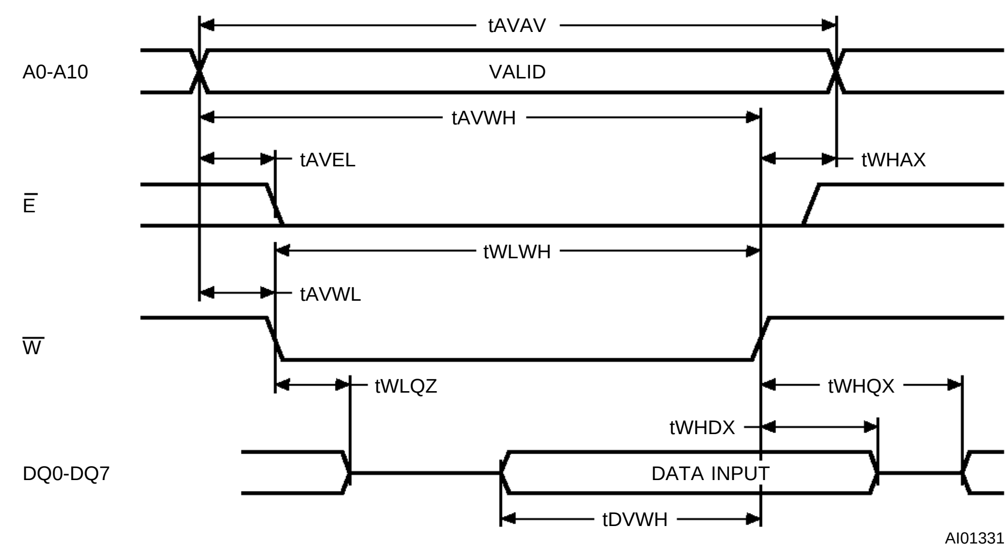
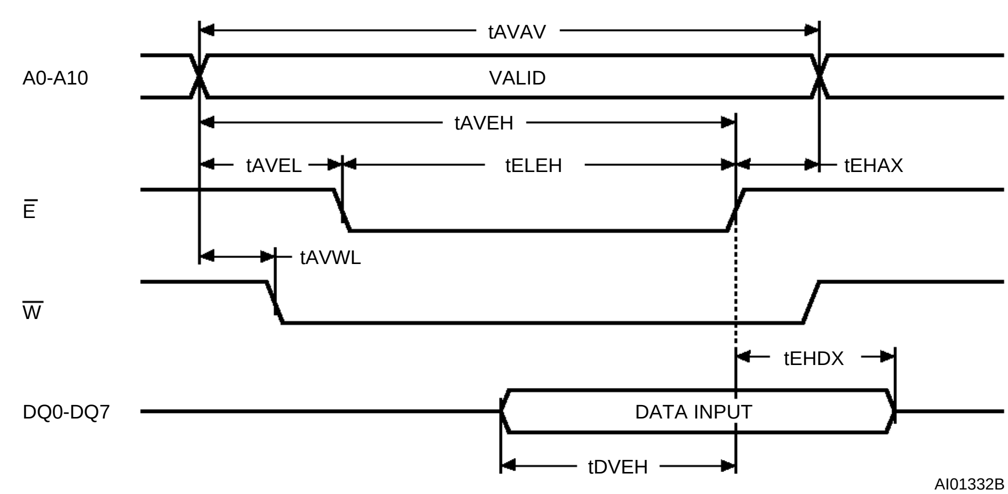


Figure 8. Chip Enable Controlled, Write AC Waveforms



DATA RETENTION MODE

With valid V_{CC} applied, the M48T02,12 operates as a conventional BYTEWIDE static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD}(max), V_{PFD}(min) window. All outputs become high impedance, and all inputs are treated as "don't care."

Note: A power failure during a write cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD}(min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The M48T02,12 may respond to transient noise spikes on V_{CC} that reach into the deselect window during the time the device is sampling V_{CC}. Therefore, decoupling of the power supply lines is recommended.

The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above V_{SO}. As V_{CC} rises, the battery voltage is checked. If the voltage is too low, an internal Battery Not OK ($\overline{\text{BOK}}$) flag will be set. The $\overline{\text{BOK}}$ flag can be checked after power up. If the $\overline{\text{BOK}}$ flag is set, the first write attempted will be blocked. The flag is automatically cleared after the first write, and normal RAM operation resumes. Figure 9 illustrates how a $\overline{\text{BOK}}$ check routine could be structured.

CLOCK OPERATIONS

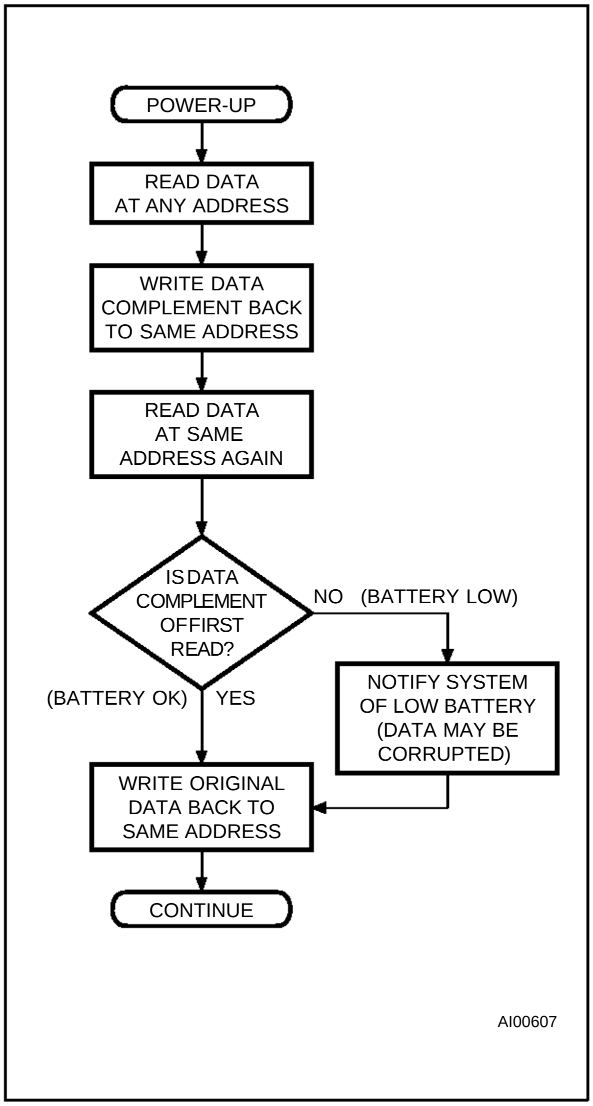
Reading the Clock

Updates to the TIMEKEEPER registers should be halted before clock data is read to prevent reading data in transition. Because the BiPORT TIMEKEEPER cells in the RAM array are only data registers, and not the actual clock counters, updating the registers can be halted without disturbing the clock itself.

Updating is halted when a '1' is written to the READ bit, the seventh bit in the control register. As long as a '1' remains in that position, updating is halted. After a halt is issued, the registers reflect the count; that is, the day, date, and the time that were current at the moment the halt command was issued.

All of the TIMEKEEPER registers are updated simultaneously. A halt will not interrupt an update in progress. Updating is within a second after the bit is reset to a '0'.

Figure 9. Checking the $\overline{\text{BOK}}$ Flag Status



Setting the Clock

The eighth bit of the control register is the WRITE bit. Setting the WRITE bit to a '1', like the READ bit, halts updates to the TIMEKEEPER registers. The user can then load them with the correct day, date, and time data in 24 hour BCD format (see Table 10). Resetting the WRITE bit to a '0' then transfers the values of all time registers (7F9h-7FFh) to the actual TIMEKEEPER counters and allows normal operation to resume. The FT bit and the bits marked as '0' in Table 10 must be written to '0' to allow for normal TIMEKEEPER and RAM operation.

Stopping and Starting the Oscillator

The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain on the battery. The STOP bit is the MSB of the seconds register. Setting it to a '1' stops the oscillator. The M48T02,12 is shipped from SGS-THOMSON with the STOP bit set to a '1'. When reset to a '0', the M48T02,12 oscillator starts within 1 second.

Calibrating the Clock

The M48T02,12 is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. A typical M48T02,12 is accurate within ±1 minute per month at 25°C without calibration. The devices are tested not to exceed 35 PPM (parts per million) oscillator frequency error at 25°C, which equates to about ± 1.53 minutes per month. Of course the oscillation rate of any crystal changes with temperature. Most clock chips compensate for crystal frequency and temperature shift error with cumbersome trim capacitors. The M48T02,12 design, however, employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 128 stage, as shown in Figure 10. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five bit Calibration byte found in the Control Register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The Calibration byte occupies the five lower order bits in the Control register. This byte can be set to represent any value between 0 and 31 in binary form. The sixth bit is a sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

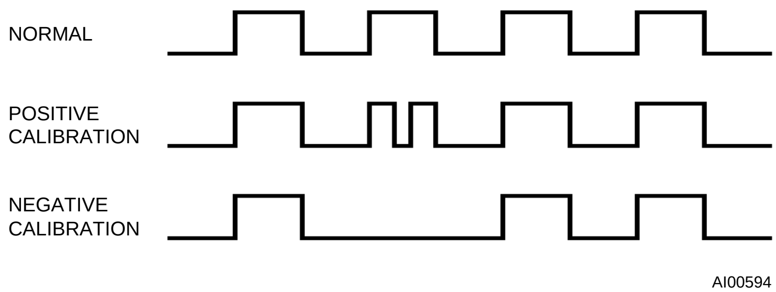
Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or -2.034 PPM of adjustment per calibration step in the calibration register. Assuming that the oscillator is in fact running at exactly 32,768 Hz, each of the 31 increments in the Calibration byte would represent +10.7 or - 5.35 seconds per month which corresponds to a total range of +5.5 or - 2.75 minutes per month.

Table 10. Register Map

Address	Data								Function/Range BCD Format	
	D7	D6	D5	D4	D3	D2	D1	D0		
7FFh	10 Years				Year				Year	00-99
7FEh	0	0	0	10 M.	Month				Month	01-12
7FDh	0	0	10 Date		Date				Date	01-31
7FCh	0	FT	0	0	0	Day			Day	01-07
7FBh	KS	0	10 Hours		Hours				Hour	00-23
7FAh	0	10 Minutes			Minutes				Minutes	00-59
7F9h	ST	10 Seconds			Seconds				Seconds	00-59
7F8h	W	R	S	Calibration					Control	

Keys: **S** = SIGN Bit
FT = FREQUENCY TEST Bit (Set to '0' for normal clock operation)
KS = KICK START Bit
R = READ Bit
W = WRITE Bit
ST = STOP Bit
0 = Must be set to '0'

Figure 10. Clock Calibration



Two methods are available for ascertaining how much calibration a given M48T02,12 may require. The first involves simply setting the clock, letting it run for a month and comparing it to a known accurate reference (like WWV broadcasts). While that may seem crude, it allows the designer to give the end user the ability to calibrate his clock as his environment may require, even after the final product is packaged in a non-user serviceable enclosure. All the designer has to do is provide a simple utility that accesses the Calibration byte. The utility could even be menu driven and made foolproof.

The second approach is better suited to a manufacturing environment, and involves the use of some test equipment. When the Frequency Test (FT) bit, the seventh-most significant bit in the Day Register, is set to a '1', and the oscillator is running at 32,768 Hz, the LSB (DQ0) of the Seconds Register will toggle at 512 Hz. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.01024 Hz would indicate a +20 PPM oscillator frequency error, requiring a -10(001010) to be loaded into the Calibration Byte for correction. Note that setting or changing the Calibration Byte does not affect the Frequency test output frequency. The device must be selected and addresses must stable at Address 7F9h when reading the 512 Hz on DQ0.

The FT bit must be set using the same method used to set the clock, using the Write bit. The LSB of the Seconds Register is monitored by holding the M48T02,12 in an extended read of the Seconds Register, without having the Read bit set. The FT bit MUST be reset to '0' for normal clock operations to resume.

ORDERING INFORMATION SCHEME

Example: M48T02 -120 PC 1

Supply Voltage and Write Protect Voltage		Speed		Package		Temp. Range	
02	V_{CC} = 4.75V to 5.5V V_{PFD} = 4.5V to 4.75V	-120	120ns	PC	PCDIP24	1	0 to 70 °C
		-150	150ns				
12	V_{CC} = 4.5V to 5.5V V_{PFD} = 4.2V to 4.5V	-200	200ns				

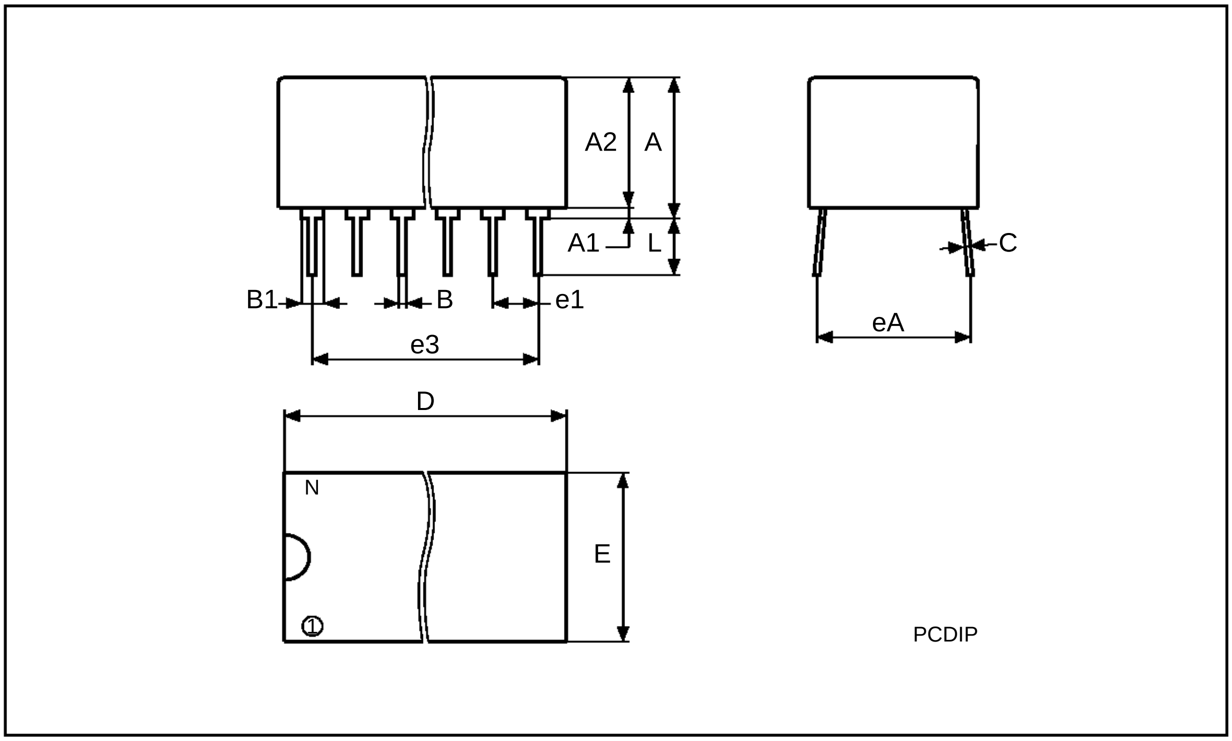
For a list of available options (Supply Voltage, Speed, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

PCDIP24 - 24 pin Plastic DIP, battery CAPHAT

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		8.89	9.65		0.350	0.380
A1		0.38	0.76		0.015	0.030
A2		8.36	8.89		0.329	0.350
B		0.38	0.53		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.31		0.008	0.012
D		34.29	34.80		1.350	1.370
E		17.83	18.34		0.702	0.722
e1		2.29	2.79		0.090	0.110
e3		25.15	30.73		0.990	1.210
eA		15.24	16.00		0.600	0.630
L		3.05	3.81		0.120	0.150
N	24			24		

PCDIP24



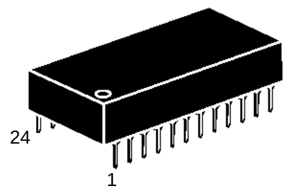
Drawing is not to scale

SGS-THOMSON MICROELECTRONICS

M48Z02
M48Z12

CMOS 2K x 8 ZEROPOWER SRAM

- INTEGRATED ULTRA LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT and BATTERY
- UNLIMITED WRITE CYCLES
- READ CYCLE TIME EQUALS WRITE CYCLE TIME
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- CHOICE of TWO WRITE PROTECT VOLTAGES:
  - M48Z02: 4.5V ≤ V_{PFD} ≤ 4.75V
  - M48Z12: 4.2V ≤ V_{PFD} ≤ 4.5V
- SELF CONTAINED BATTERY in the CAPHAT DIP PACKAGE
- 10 YEARS of DATA RETENTION in the ABSENCE of POWER
- PIN and FUNCTION COMPATIBLE with JEDEC STANDARD 2K x 8 SRAMs



PCDIP24 (PC)
Battery CAPHAT

DESCRIPTION

The M48Z02,12 ZEROPOWER® RAM is a 2K x 8 non-volatile static RAM which is pin and functional compatible with the MK48Z02,12.

A special 24 pin 600mil DIP CAPHAT™ package houses the M48Z02,12 silicon with a long life lithium button cell to form a highly integrated battery backed-up memory solution.

Table 1. Signal Names

A0-A10	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

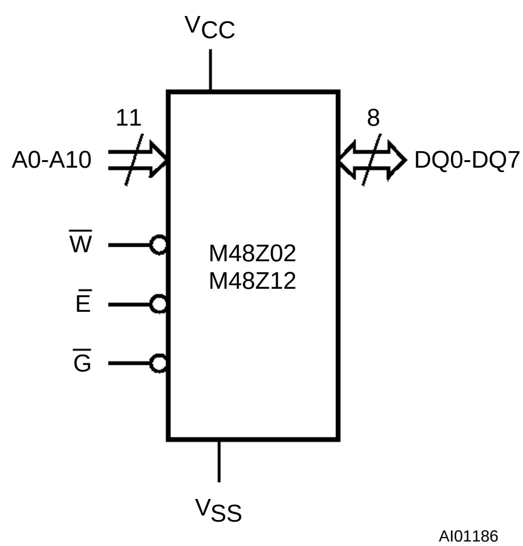


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature grade 1 grade 6	0 to 70 –40 to 85	°C
T_{STG}	Storage Temperature (V_{CC} Off)	–40 to 85	°C
V_{IO}	Input or Output Voltages	–0.3 to 7	V
V_{CC}	Supply Voltage	–0.3 to 7	V
I_O	Output Current	20	mA
P_D	Power Dissipation	1	W

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

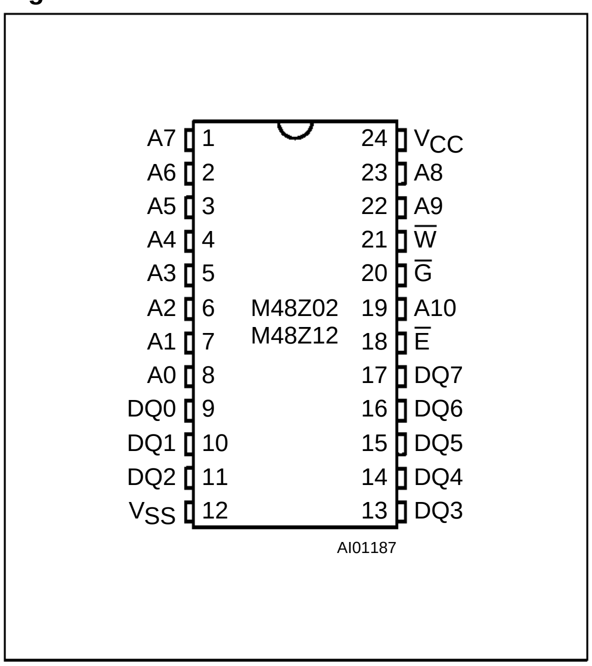
CAUTION: *Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

Table 3. Operating Modes

Mode	V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.75V to 5.5V or 4.5V to 5.5V	V_{IH}	X	X	High Z	Standby
Write		V_{IL}	X	V_{IL}	D_{IN}	Active
Read		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Read		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min)	X	X	X	High Z	CMOS Standby
Deselect	$\leq V_{SO}$	X	X	X	High Z	Battery Back-up Mode

Note: X = V_{IH} or V_{IL}

Figure 2. DIP Pin Connections



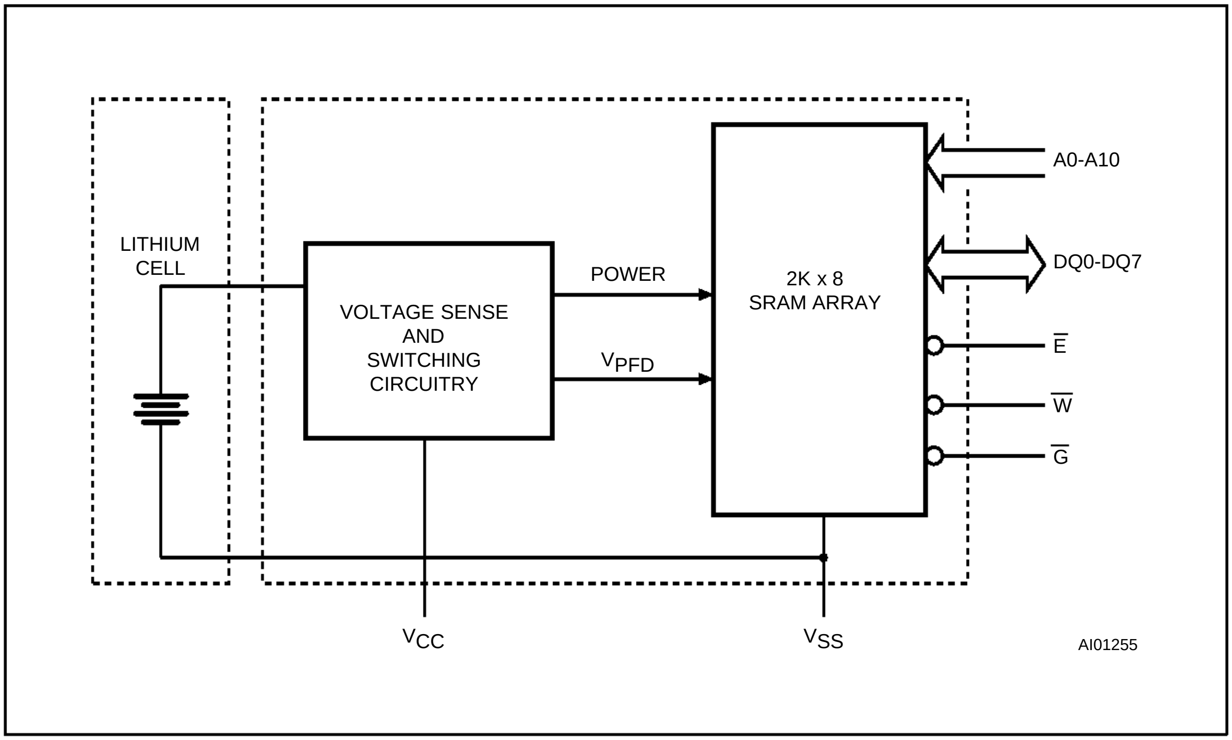
DESCRIPTION (cont'd)

The M48Z02,12 button cell has sufficient capacity and storage life to maintain data and clock functionality for an accumulated time period of at least 10 years in the absence of power over the operating temperature range.

The M48Z02,12 is a non-volatile pin and function equivalent to any JEDEC standard 2K x 8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The M48Z02,12 also has its own Power-fail Detect circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the battery which maintains data and clock operation until valid power returns.

Figure 3. Block Diagram



READ MODE

The M48Z02,12 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low. The device architecture allows ripple-through access of data from eight of 16,384 locations in the static storage array. Thus, the unique address specified by the 11 Address Inputs defines which one of the 2,048 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} (Address Access Time) after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the latter of the Chip Enable Access Time (t_{ELQV}) or Output Enable Access Time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain active, output data will remain valid for t_{AXQX} (Output Data Hold Time) but will go indeterminate until the next Address Access.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0.6V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.2V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

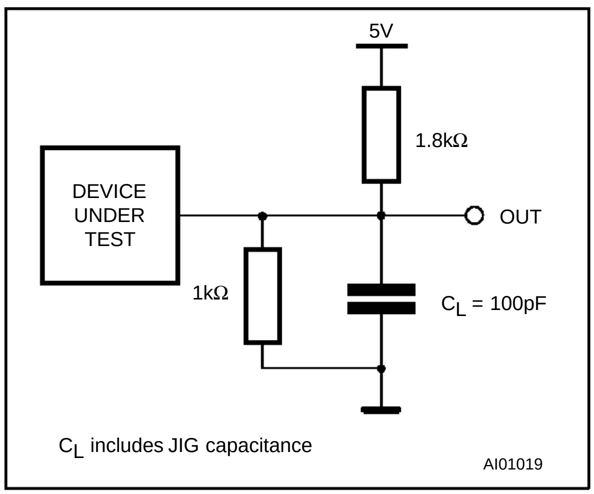


Table 4. Capacitance (1) (T_A = 25 °C)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		10	pF
C_{IO} (2)	Input / Output Capacitance	V_{OUT} = 0V		10	pF

Notes: 1. Effective capacitance calculated from the equation C = IΔt/ΔV with ΔV = 3V and power supply at 5V.
2. Outputs deselected

Table 5. DC Characteristics (T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI} (1)	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±1	µA
I_{LO} (1)	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±5	µA
I_{CC}	Supply Current	Outputs open		80	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		3	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ = V_{CC} – 0.2V		3	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4		V

Note: 1. Outputs Deselected.

Table 6. Power Down/Up Trip Points DC Characteristics (1) (T_A = 0 to 70°C or –40 to 85°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage (M48Z02)	4.5	4.6	4.75	V
V_{PFD}	Power-fail Deselect Voltage (M48Z12)	4.2	4.3	4.5	V
V_{SO}	Battery Back-up Switchover Voltage		3.0		V
t_{DR}	Expected Data Retention Time	10			YEARS

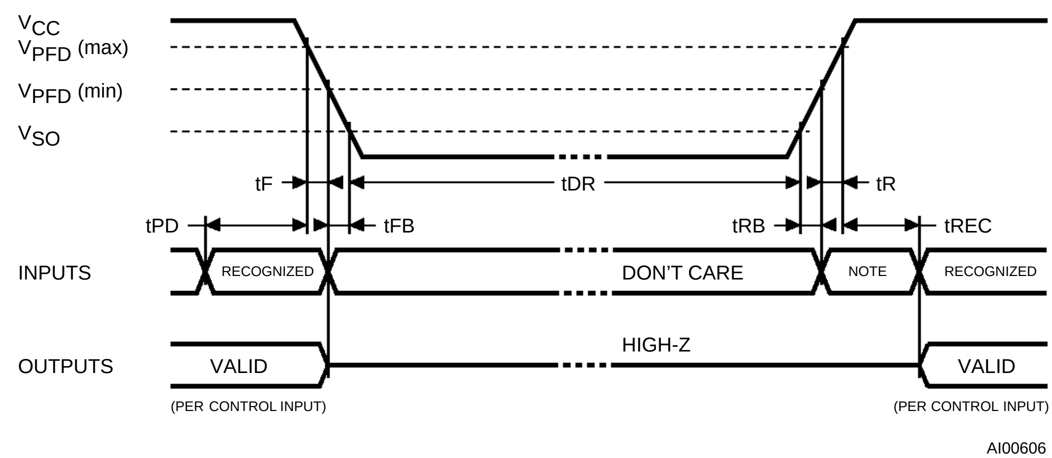
Note: 1. All voltages referenced to V_{SS}.

Table 7. Power Down/Up Mode AC Characteristics (T_A = 0 to 70°C or –40 to 85°C)

Symbol	Parameter	Min	Max	Unit
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0		µs
t_F (1)	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs
t_{FB} (2)	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs
t_R	V_{PFD}(min) to V_{PFD} (max) V_{CC} Rise Time	0		µs
t_{RB}	V_{SO} to V_{PFD} (min) V_{CC} Rise Time	1		µs
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} after Power Up	2		ms

Notes: 1. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 50 µs after V_{CC} passes V_{PFD} (min).
2. V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.

Figure 5. Power Down/Up Mode AC Waveforms



Note: Inputs may or may not be recognized at this time. Caution should be taken to keep $\overline{E}$ high as V_{CC} rises past V_{PFD}(min). Some systems may performs inadvertent write cycles after V_{CC} rises above V_{PFD}(min) but before normal system operations begins. Even though a power on reset is being applied to the processor a reset condition may not occur until after the system clock is running.

Table 8. Read Mode AC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48Z02 / 12						Unit
		-120		-150		-200		
		Min	Max	Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	120		150		200		ns
t_{AVQV}	Address Valid to Output Valid		120		150		200	ns
t_{ELQV}	Chip Enable Low to Output Valid		120		150		200	ns
t_{GLQV}	Output Enable Low to Output Valid		75		75		80	ns
t_{ELQX}	Chip Enable Low to Output Transition	10		10		10		ns
t_{GLQX}	Output Enable Low to Output Transition	5		5		5		ns
t_{EHQZ}	Chip Enable High to Output Hi-Z		30		35		40	ns
t_{GHQZ}	Output Enable High to Output Hi-Z		30		35		40	ns
t_{AXQX}	Address Transition to Output Transition	5		5		5		ns

Figure 6. Read Mode AC Waveforms

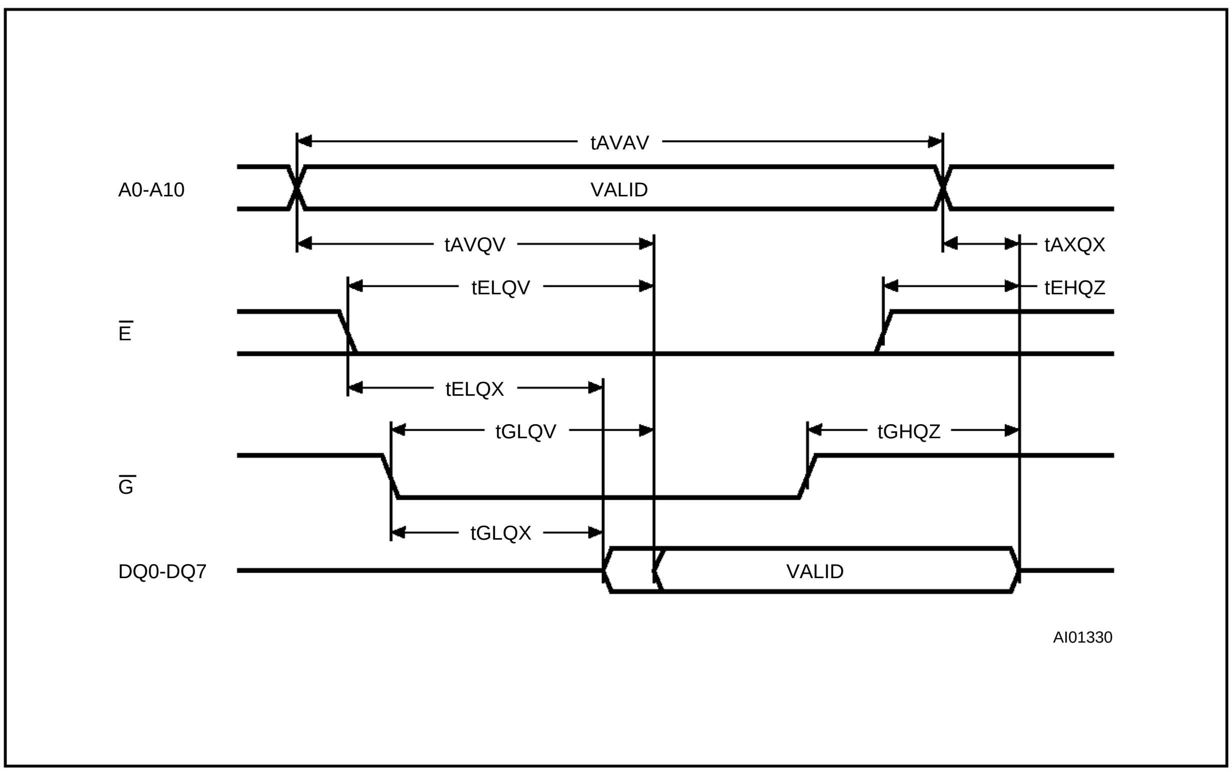


Table 9. Write Mode AC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48Z02 / 12						Unit
		-120		-150		-200		
		Min	Max	Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	120		150		200		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		0		ns
t_{AVEL}	Address Valid to Chip Enable Low	0		0		0		ns
t_{WLWH}	Write Enable Pulse Width	75		90		120		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	75		90		120		ns
t_{WHAX}	Write Enable High to Address Transition	10		10		10		ns
t_{EHAX}	Chip Enable High to Address Transition	10		10		10		ns
t_{DVWH}	Input Valid to Write Enable High	35		40		60		ns
t_{DVEH}	Input Valid to Chip Enable High	35		40		60		ns
t_{WHDX}	Write Enable High to Input Transition	5		5		5		ns
t_{EHDX}	Chip Enable High to Input Transition	5		5		5		ns
t_{WLQZ}	Write Enable Low to Output Hi-Z		40		50		60	ns
t_{AVWH}	Address Valid to Write Enable High	90		120		140		ns
t_{AVEH}	Address Valid to Chip Enable High	90		120		140		ns
t_{WHQX}	Write Enable High to Output Transition	10		10		10		ns

WRITE MODE

The M48Z02,12 is in the Write Mode whenever $\overline{W}$ and $\overline{E}$ are active. The start of a write is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for minimum of t_{EHAX} from Chip Enable or t_{WHAX} from Write Enable prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} afterward. $\overline{G}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

Figure 7. Write Enable Controlled, Write AC Waveforms

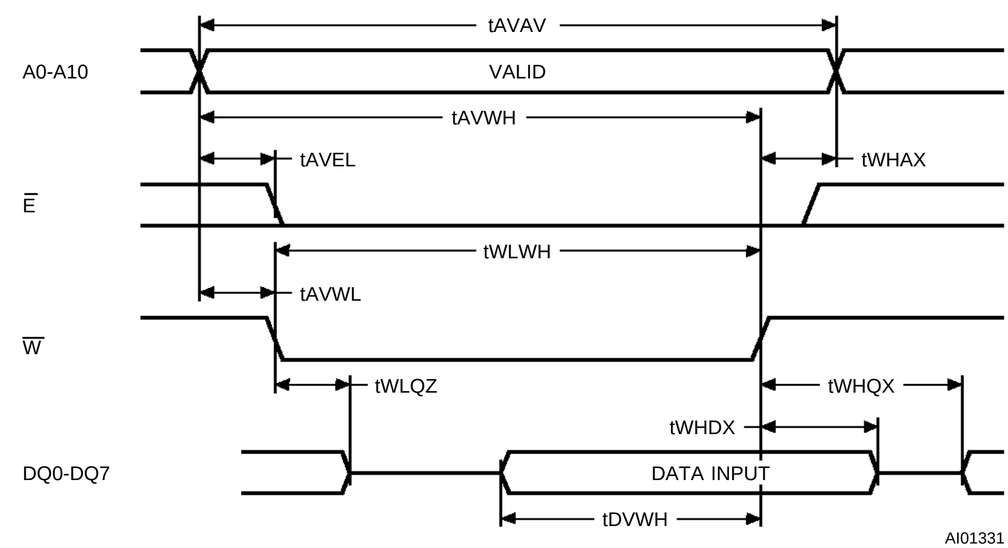
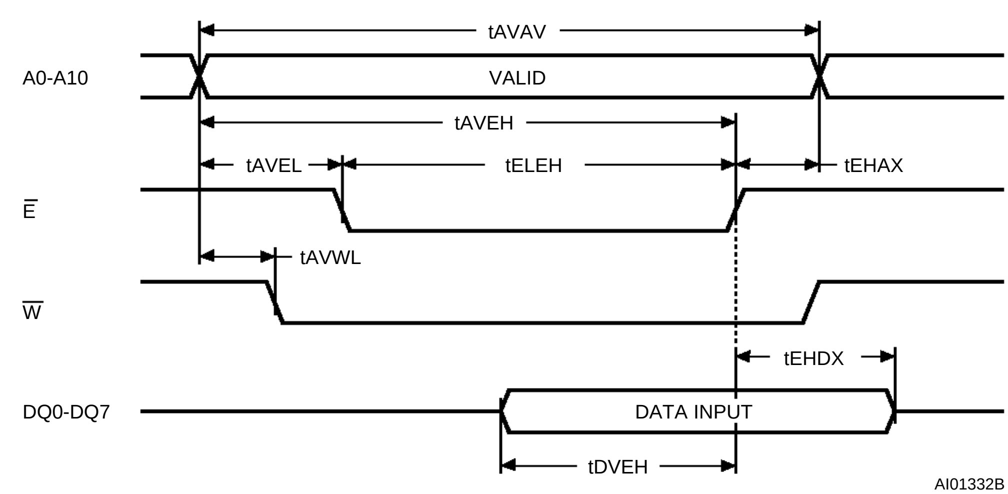


Figure 8. Chip Enable Controlled, Write AC Waveforms



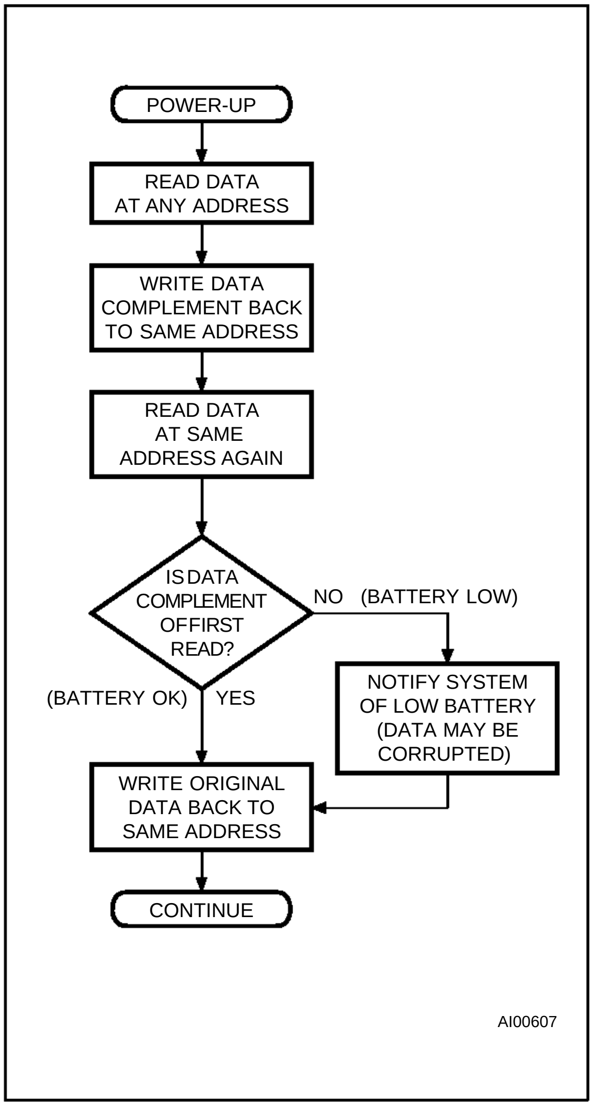
DATA RETENTION MODE

With valid V_{CC} applied, the M48Z02,12 operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD}(max), V_{PFD}(min) window. All outputs become high impedance, and all inputs are treated as "don't care."

Note: A power failure during a write cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD}(min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The M48Z02,12 may respond to transient noise spikes on V_{CC} that reach into the deselect window during the time the device is sampling V_{CC}. Therefore, decoupling of the power supply lines is recommended.

The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above V_{SO}. As V_{CC} rises, the battery voltage is checked. If the voltage is too low, an internal Battery Not OK ($\overline{BOK}$) flag will be set. The $\overline{BOK}$ flag can be checked after power up. If the $\overline{BOK}$ flag is set, the first write attempted will be blocked. The flag is automatically cleared after the first write, and normal RAM operation resumes. Figure 9 illustrates how a $\overline{BOK}$ check routine could be structured.

Figure 9. Checking the $\overline{BOK}$ Flag Status



ORDERING INFORMATION SCHEME

Example: M48Z02 -120 PC 1

Supply Voltage and Write Protect Voltage		Speed		Package		Temp. Range	
02	V_{CC} = 4.75V to 5.5V V_{PFD} = 4.5V to 4.75V	-120	120ns	PC	PCDIP24	1	0 to 70 °C
12	V_{CC} = 4.5V to 5.5V V_{PFD} = 4.2V to 4.5V	-150	150ns			6	–40 to 85 °C
		-200	200ns				

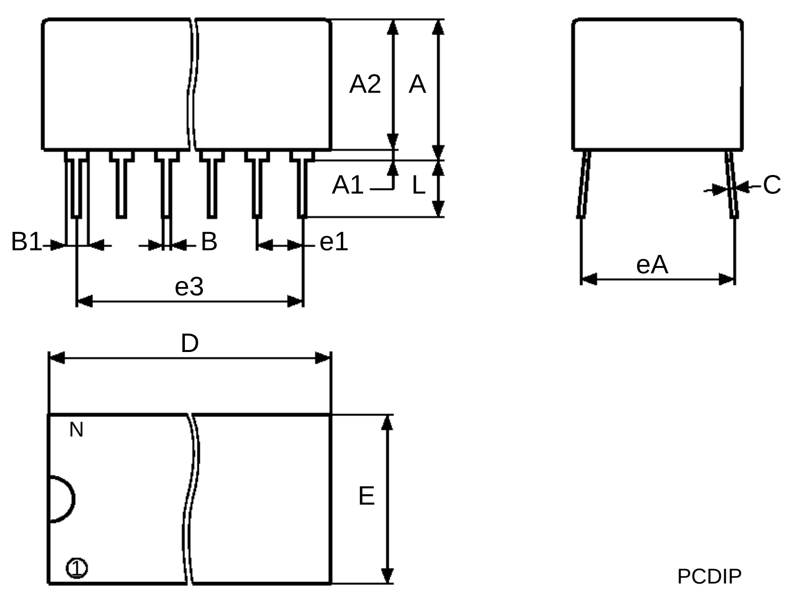
For a list of available options (Supply Voltage, Speed, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

PCDIP24 - 24 pin Plastic DIP, battery CAPHAT

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		8.89	9.65		0.350	0.380
A1		0.38	0.76		0.015	0.030
A2		8.36	8.89		0.329	0.350
B		0.38	0.53		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.31		0.008	0.012
D		34.29	34.80		1.350	1.370
E		17.83	18.34		0.702	0.722
e1		2.29	2.79		0.090	0.110
e3		25.15	30.73		0.990	1.210
eA		15.24	16.00		0.600	0.630
L		3.05	3.81		0.120	0.150
N	24			24		

PCDIP24



Drawing is not to scale

CMOS 64 x 8 SERIAL ACCESS TIMEKEEPER SRAM

- COUNTERS for SECONDS, MINUTES, HOURS, DAY, DATE, MONTH and YEARS
- SOFTWARE CLOCK CALIBRATION
- AUTOMATIC POWER FAIL DETECT and SWITCH CIRCUITRY
- I^2C BUS COMPATIBLE
- 56 BYTES of GENERAL PURPOSE RAM
- ULTRA-LOW BATTERY SUPPLY CURRENT of 500nA
- AVAILABLE with an OPERATING TEMPERATURE of –40 to 85°C
- AUTOMATIC LEAP YEAR COMPENSATION

PSDIP8 (N)
0.4mm Frame

SO8 (S)
0.15mm Frame

DESCRIPTION

The MK41T56 TIMEKEEPER™ RAM is a low power 512 bit static CMOS RAM organized as 64 words by 8 bits. A built-in 32.768 kHz oscillator (external crystal controlled) and the first 8 bytes of the RAM are used for the clock/calendar function and are configured in BCD format. Addresses and data are transferred serially via a two-line bi-directional bus. The built-in address register is incremented automatically after each write or read data byte. The MK41T56 clock has a built-in power sense circuit which detects power failures and automatically switches to the battery supply during power failures. The energy needed to sustain the RAM and clock operations can be supplied from a small lithium button cell.

Figure 1. Logic Diagram

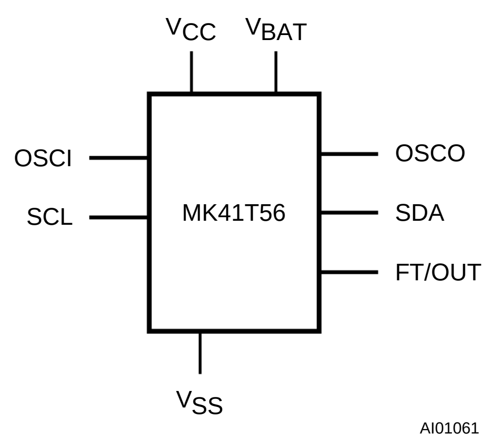


Table 1. Signal Names

OSCI	Oscillator Input
OCSO	Oscillator Output
FT/OUT	Frequency Test / Output Driver
SDA	Serial Data Address Input / Output
SCL	Serial Clock
V_{BAT}	Battery Supply Voltage
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

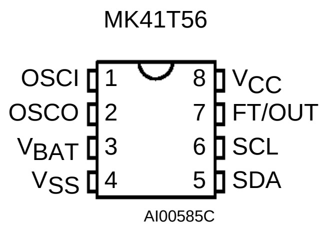


Figure 2B. SO Pin Connections

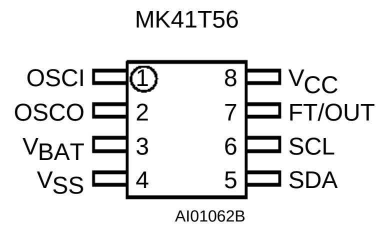


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70 –40 to 85	°C
T_{STG}	Storage Temperature (V_{CC} Off, Oscillator Off)	–55 to 125	°C
V_{IO}	Input or Output Voltages	–0.3 to 7	V
V_{CC}	Supply Voltage	–0.3 to 7	V
I_O	Output Current	20	mA
P_D	Power Dissipation	0.25	W

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

***CAUTION:** Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

Table 3. Register Map

Address	Data								Function/Range BCD Format	
	D7	D6	D5	D4	D3	D2	D1	D0		
0	ST	10 Seconds			Seconds				Seconds	00-59
1	X	10 Minutes			Minutes				Minutes	00-59
2	X	X	10 Hours		Hours				Hour	00-23
3	X	X	X	X	X	Day			Day	01-07
4	X	X	10 Date		Date				Date	01-31
5	X	X	X	10 M.	Month				Month	01-12
6	10 Years				Years				Year	00-99
7	OUT	FT	S	Calibration					Control	

Keys: **S** = SIGN Bit; **FT** = FREQUENCY TEST Bit; **ST** = STOP Bit; **OUT** = Output level; **X** = Don't care.