

MC74VHCT125A

Quad Bus Buffer with 3-State Control Inputs

The MC74VHCT125A is a high speed CMOS quad bus buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74VHCT125A requires the 3-state control input (\overline{OE}) to be set High to place the output into the high impedance state.

The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3V to 5.0V, because it has full 5V CMOS level output swings.

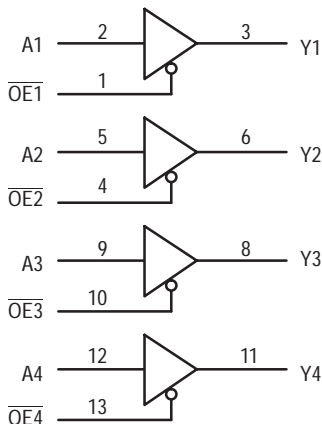
The VHCT125A input structures provide protection when voltages between 0V and 5.5V are applied, regardless of the supply voltage. The output structures also provide protection when $V_{CC} = 0V$. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

- High Speed: $t_{PD} = 3.8ns$ (Typ) at $V_{CC} = 5V$
- Low Power Dissipation: $I_{CC} = 4\mu A$ (Max) at $T_A = 25^\circ C$
- TTL-Compatible Inputs: $V_{IL} = 0.8V$; $V_{IH} = 2.0V$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2V to 5.5V Operating Range
- Low Noise: $V_{OLP} = 0.8V$ (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 72 FETs or 18 Equivalent Gates

LOGIC DIAGRAM

Active-Low Output Enables



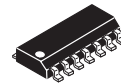
FUNCTION TABLE

| VHCT125A | | |
|----------|-----------------|--------|
| Inputs | | Output |
| A | \overline{OE} | Y |
| H | L | H |
| L | L | L |
| X | H | Z |

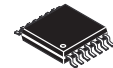


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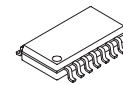
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14-LEAD SOIC
D SUFFIX
CASE 751A

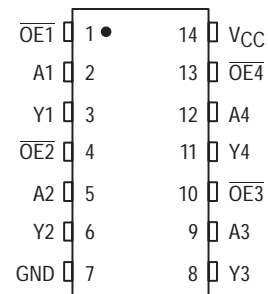


14-LEAD TSSOP
DT SUFFIX
CASE 948G



14-LEAD SOIC EIAJ
M SUFFIX
CASE 965

PIN CONNECTION AND MARKING DIAGRAM (Top View)



For detailed package marking information, see the Marking Diagram section on page 4 of this data sheet.

ORDERING INFORMATION

| Device | Package | Shipping |
|----------------|-----------|---------------|
| MC74VHCT125AD | SOIC | 55 Units/Rail |
| MC74VHCT125ADT | TSSOP | 96 Units/Rail |
| MC74VHCT125AM | SOIC EIAJ | 50 Units/Rail |

MC74VHCT125A

MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|------------------|---------------------------------------------------------------|--------------------------------|------|
| V _{CC} | DC Supply Voltage | - 0.5 to + 7.0 | V |
| V _{in} | DC Input Voltage | - 0.5 to + 7.0 | V |
| V _{out} | DC Output Voltage | - 0.5 to V _{CC} + 0.5 | V |
| I _{IK} | Input Diode Current | - 20 | mA |
| I _{OK} | Output Diode Current | ± 20 | mA |
| I _{out} | DC Output Current, per Pin | ± 25 | mA |
| I _{CC} | DC Supply Current, V _{CC} and GND Pins | ± 50 | mA |
| P _D | Power Dissipation in Still Air, SOIC Packages† TSSOP Package† | 500 450 | mW |
| T _{stg} | Storage Temperature | - 65 to + 150 | °C |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

† Derating — SOIC Packages: - 7 mW/°C from 65° to 125°C
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|---------------------------------|--------------------------------------------------------|------|-----------------|------|
| V _{CC} | DC Supply Voltage | 4.5 | 5.5 | V |
| V _{in} | DC Input Voltage | 0 | 5.5 | V |
| V _{out} | DC Output Voltage | 0 | V _{CC} | V |
| T _A | Operating Temperature, All Package Types | - 40 | + 85 | °C |
| t _r , t _f | Input Rise and Fall Time V _{CC} = 5.0V ± 0.5V | 0 | 20 | ns/V |

DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Conditions | V _{CC} (V) | T _A = 25°C | | | T _A ≤ 85°C | | T _A ≤ 125°C | | Unit |
|------------------|-------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------|---------------------|-----------------------|-----|-------|-----------------------|-------|------------------------|------|------|
| | | | | Min | Typ | Max | Min | Max | Min | Max | |
| V _{IH} | Minimum High-Level Input Voltage | | 3.0 | 1.2 | | | 1.2 | | 1.2 | | V |
| | | | 4.5 | 2.0 | | 2.0 | | 2.0 | | | |
| | | | 5.5 | 2.0 | | 2.0 | | 2.0 | | | |
| V _{IL} | Maximum Low-Level Input Voltage | | 3.0 | | | 0.53 | | 0.53 | | 0.53 | V |
| | | | 4.5 | | | 0.8 | | 0.8 | | 0.8 | |
| | | | 5.5 | | | 0.8 | | 0.8 | | 0.8 | |
| V _{OH} | Minimum High-Level Output Voltage V _{IN} = V _{IH} or V _{IL} | V _{IN} = V _{IH} or V _{IL} I _{OH} = - 50μA | 3.0 | 2.9 | 3.0 | | 2.9 | | 2.9 | | V |
| | | | 4.5 | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | | V _{IN} = V _{IH} or V _{IL} I _{OH} = - 4mA I _{OH} = - 8mA | 3.0 | 2.58 | | | 2.48 | | 2.34 | | |
| | | | 4.5 | 3.94 | | | 3.80 | | 3.66 | | |
| V _{OL} | Maximum Low-Level Output Voltage V _{IN} = V _{IH} or V _{IL} | V _{IN} = V _{IH} or V _{IL} I _{OL} = 50μA | 3.0 | | 0.0 | 0.1 | | 0.1 | | 0.1 | V |
| | | | 4.5 | | 0.0 | 0.1 | | 0.1 | | 0.1 | |
| | | V _{IN} = V _{IH} or V _{IL} I _{OL} = 4mA I _{OL} = 8mA | 3.0 | | | 0.36 | | 0.44 | | 0.52 | |
| | | | 4.5 | | | 0.36 | | 0.44 | | 0.52 | |
| I _{IN} | Maximum Input Leakage Current | V _{IN} = 5.5 V or GND | 0 to 5.5 | | | ± 0.1 | | ± 1.0 | | μA | |
| I _{CC} | Maximum Quiescent Supply Current | V _{IN} = V _{CC} or GND | 5.5 | | | 2.0 | | 20 | | 40 | μA |
| I _{CCT} | Quiescent Supply Current | Input: V _{IN} = 3.4V | 5.5 | | | 1.35 | | 1.50 | | 1.65 | mA |
| I _{OPD} | Output Leakage Current | V _{OUT} = 5.5V | 0.0 | | | 0.5 | | 5.0 | | 10 | μA |

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AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0\text{ns}$)

| Symbol | Parameter | Test Conditions | $T_A = 25^\circ\text{C}$ | | | $T_A = \leq 85^\circ\text{C}$ | | $T_A \leq 125^\circ\text{C}$ | | Unit |
|----------------------------|-------------------------------------------------------------------------|-----------------------------------------------------------------|--------------------------|-----|------|-------------------------------|------|------------------------------|------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| t_{PLH} , t_{PHL} | Maximum Propagation Delay, A to Y | $V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 15\text{pF}$ | | 5.6 | 8.0 | 1.0 | 9.5 | | 12.0 | ns |
| | | $C_L = 50\text{pF}$ | | 8.1 | 11.5 | 1.0 | 13.0 | | 16.0 | |
| | | $V_{CC} = 5.0 \pm 0.5\text{V}$ $C_L = 15\text{pF}$ | | 3.8 | 5.5 | 1.0 | 6.5 | | 8.5 | |
| | | $C_L = 50\text{pF}$ | | 5.3 | 7.5 | 1.0 | 8.5 | | 10.5 | |
| t_{PZL} , t_{PZH} | Maximum Output Enable Time, \overline{OE} to Y | $V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 15\text{pF}$ | | 5.4 | 8.0 | 1.0 | 9.5 | | 11.5 | ns |
| | | $R_L = 1\text{k}\Omega$ $C_L = 50\text{pF}$ | | 7.9 | 11.5 | 1.0 | 13.0 | | 15.0 | |
| | | $V_{CC} = 5.0 \pm 0.5\text{V}$ $C_L = 15\text{pF}$ | | 3.6 | 5.1 | 1.0 | 6.0 | | 7.5 | |
| | | $R_L = 1\text{k}\Omega$ $C_L = 50\text{pF}$ | | 5.1 | 7.1 | 1.0 | 8.0 | | 9.5 | |
| t_{PLZ} , t_{PHZ} | Maximum Output Disable Time, \overline{OE} to Y | $V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 50\text{pF}$ | | 9.5 | 13.2 | 1.0 | 15.0 | | 18.0 | ns |
| | | $R_L = 1\text{k}\Omega$ | | | | | | | | |
| | | $V_{CC} = 5.0 \pm 0.5\text{V}$ $C_L = 50\text{pF}$ | | 6.1 | 8.8 | 1.0 | 10.0 | | 12.0 | |
| | | $R_L = 1\text{k}\Omega$ | | | | | | | | |
| t_{OSLH} , t_{OSHL} | Output-to-Output Skew | $V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 50\text{pF}$ (Note 1.) | | | 1.5 | | 1.5 | | 2.0 | ns |
| | | $V_{CC} = 5.0 \pm 0.5\text{V}$ $C_L = 50\text{pF}$ (Note 1.) | | | 1.0 | | 1.0 | | 1.5 | |
| C_{in} | Maximum Input Capacitance | | | 4 | 10 | | 10 | | 10 | pF |
| C_{out} | Maximum Three-State Output Capacitance (Output in High Impedance State) | | | 6 | | | | | | pF |

| C_{PD} | Power Dissipation Capacitance (Note 2.) | Typical @ 25°C , $V_{CC} = 5.0\text{V}$ | | Unit |
|----------|-----------------------------------------|-------------------------------------------------------|--|------|
| | | 14 | | |
| | | | | pF |

- Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
- C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}/4$ (per buffer). C_{PD} is used to determine the no-load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0\text{ns}$, $C_L = 50\text{pF}$, $V_{CC} = 5.0\text{V}$)

| Symbol | Characteristic | $T_A = 25^\circ\text{C}$ | | Unit |
|-----------|------------------------------------------|--------------------------|------|------|
| | | Typ | Max | |
| V_{OLP} | Quiet Output Maximum Dynamic V_{OL} | 0.3 | 0.8 | V |
| V_{OLV} | Quiet Output Minimum Dynamic V_{OL} | -0.3 | -0.8 | V |
| V_{IHD} | Minimum High Level Dynamic Input Voltage | | 3.5 | V |
| V_{ILD} | Maximum Low Level Dynamic Input Voltage | | 1.5 | V |

MC74VHCT125A

SWITCHING WAVEFORMS

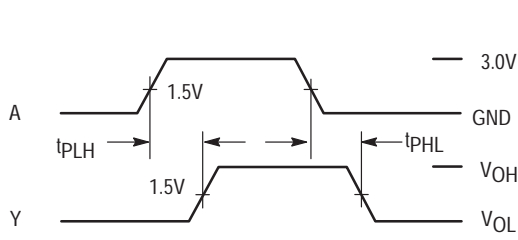


Figure 1.

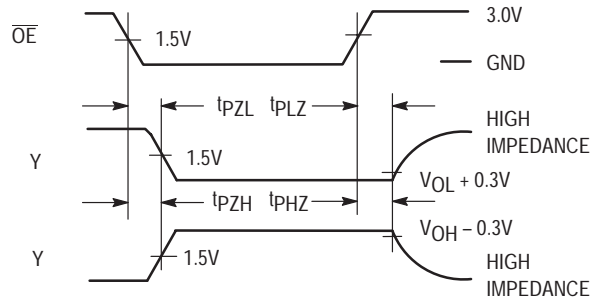
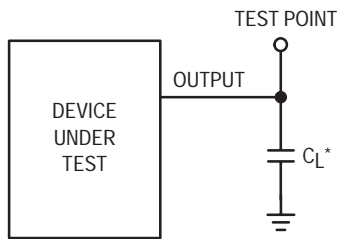
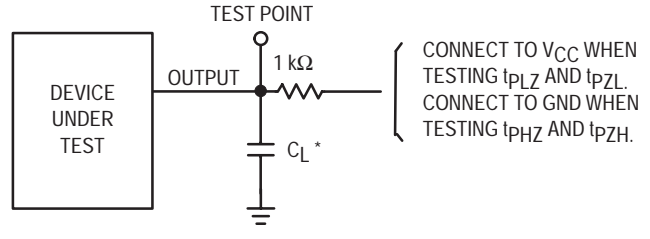


Figure 2.



*Includes all probe and jig capacitance

Figure 3. Test Circuit

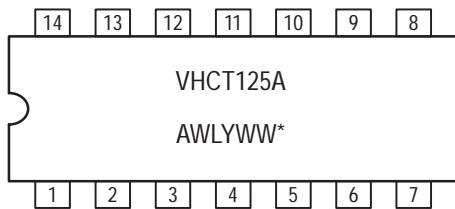


*Includes all probe and jig capacitance

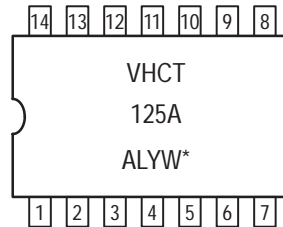
Figure 4. Test Circuit

MARKING DIAGRAMS

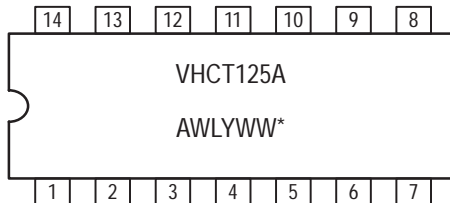
(Top View)



14-LEAD SOIC
D SUFFIX
CASE 751A



14-LEAD TSSOP
DT SUFFIX
CASE 948G



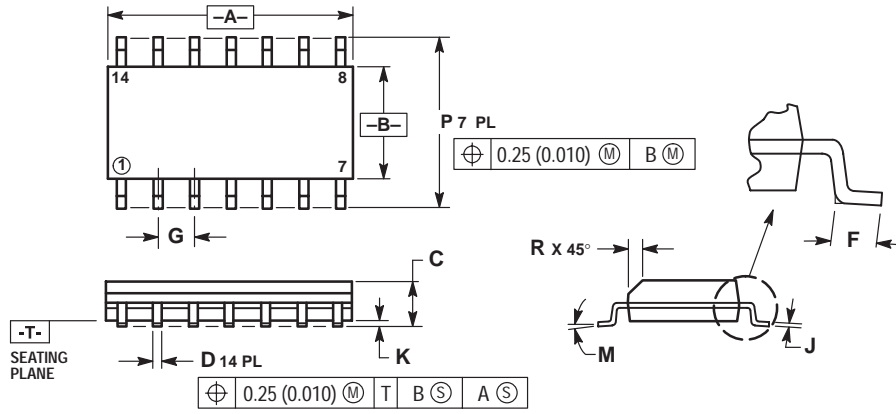
14-LEAD SOIC EIAJ
M SUFFIX
CASE 965

*See Applications Note #AND8004/D for date code and traceability information.

MC74VHCT125A

PACKAGE DIMENSIONS

D SUFFIX
PLASTIC SOIC PACKAGE
 CASE 751A-03
 ISSUE F



NOTES:

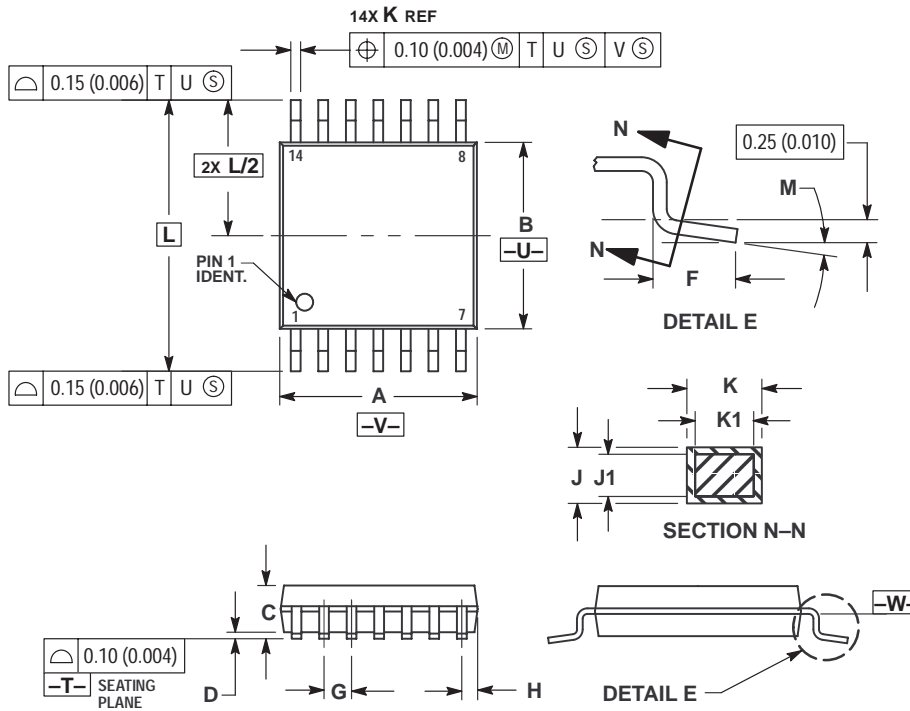
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 8.55 | 8.75 | 0.337 | 0.344 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.228 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

MC74VHCT125A

PACKAGE DIMENSIONS

DT SUFFIX
 PLASTIC TSSOP PACKAGE
 CASE 948G-01
 ISSUE O



NOTES:

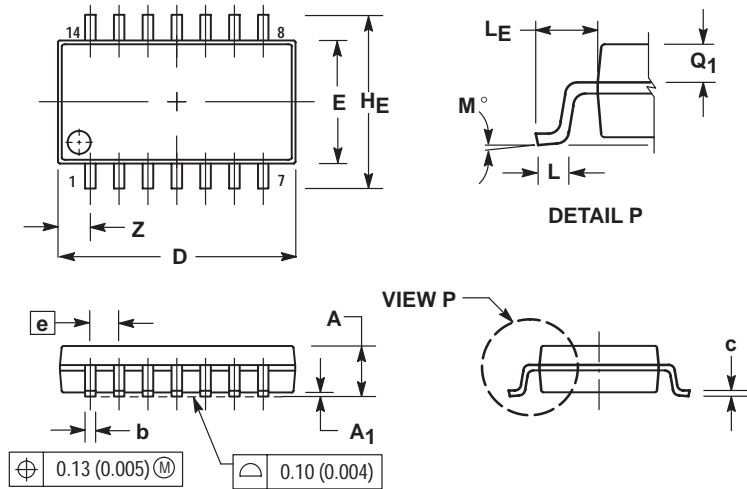
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.50 | 0.60 | 0.020 | 0.024 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

MC74VHCT125A

PACKAGE DIMENSIONS

M SUFFIX
 PLASTIC SOIC EIAJ PACKAGE
 CASE 965-01
 ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

| DIM | MILLIMETERS | | INCHES | |
|----------------|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | --- | 2.05 | --- | 0.081 |
| A ₁ | 0.05 | 0.20 | 0.002 | 0.008 |
| b | 0.35 | 0.50 | 0.014 | 0.020 |
| c | 0.18 | 0.27 | 0.007 | 0.011 |
| D | 9.90 | 10.50 | 0.390 | 0.413 |
| E | 5.10 | 5.45 | 0.201 | 0.215 |
| e | 1.27 BSC | | 0.050 BSC | |
| H _E | 7.40 | 8.20 | 0.291 | 0.323 |
| 0.50 | 0.50 | 0.85 | 0.020 | 0.033 |
| L _E | 1.10 | 1.50 | 0.043 | 0.059 |
| M | 0° | 10° | 0° | 10° |
| Q ₁ | 0.70 | 0.90 | 0.028 | 0.035 |
| Z | --- | 1.42 | --- | 0.056 |

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