

Document Title

**64Kx16 Bit High-Speed CMOS Static RAM(5.0V Operating).  
Operated at Commercial and Industrial Temperature Ranges.**

Revision History

<u>Rev.No.</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>								
Rev. 0.0	Initial release with Preliminary.	June. 8. 2001	Preliminary								
Rev. 0.1	Page 4, DC operation condition modify	June. 16. 2001	Preliminary								
Rev. 0.2	Current modify	September. 9. 2001	Preliminary								
Rev. 0.3	1. Delete 15ns speed bin. 2. Change Icc for Industrial mode.	December. 18.2001	Preliminary								
	<table border="1"> <thead> <tr> <th>Item</th> <th>Previous</th> <th>Current</th> </tr> </thead> <tbody> <tr> <td rowspan="2">Icc(Industrial)</td> <td>10ns</td> <td>85mA</td> </tr> <tr> <td>12ns</td> <td>75mA</td> </tr> </tbody> </table>	Item	Previous	Current	Icc(Industrial)	10ns	85mA	12ns	75mA		
Item	Previous	Current									
Icc(Industrial)	10ns	85mA									
	12ns	75mA									
Rev. 1.0	1. Final datasheet release. 2. Correct read cycle timing diagram(2).	June. 19. 2002	Final								

The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.



**1Mb Async. Fast SRAM Ordering Information**

Org.	Part Number	VDD(V)	Speed ( ns )	PKG	Temp. & Power
256K x4	K6R1004C1D-JC(I) 10/12	5	10/12	J : 32-SOJ	C : Commercial Temperature ,Normal Power Range I : Industrial Temperature ,Normal Power Range
	K6R1004V1D-JC(I) 08/10	3.3	8/10		
128K x8	K6R1008C1D-J(T)C(I) 10/12	5	10/12	J : 32-SOJ	
	K6R1008V1D-J(T)C(I) 08/10	3.3	8/10	T : 32-TSOP2	
64K x16	K6R1016C1D-J(T,E)C(I) 10/12	5	10/12	J : 44-SOJ	
	K6R1016V1D-J(T,E)C(I) 08/10	3.3	8/10	T : 44-TSOP2 E : 48-TBGA	

## 64K x 16 Bit High-Speed CMOS Static RAM

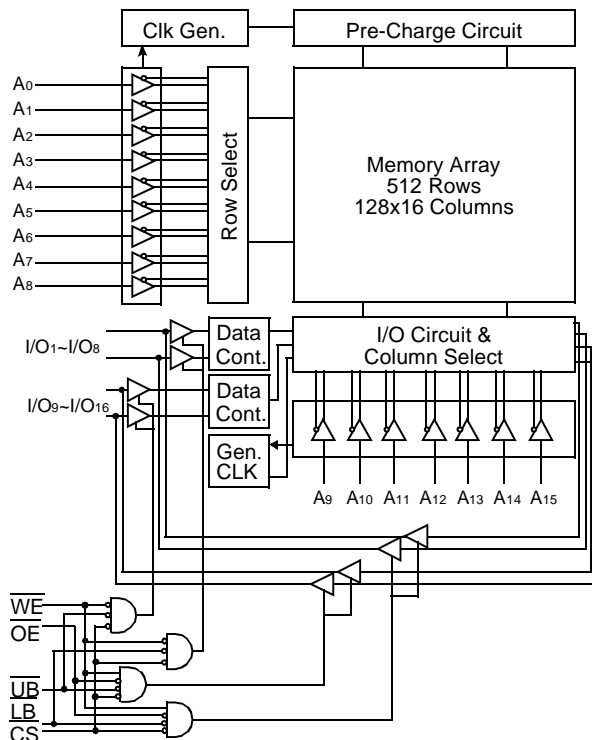
### FEATURES

- Fast Access Time 10,12(Max.)
- Power Dissipation
  - Standby (TTL) : 20mA(Max.)
  - (CMOS) : 5mA(Max.)
  - Operating K6R1016C1D-10 : 65mA(Max.)
  - K6R1016C1D-12 : 55mA(Max.)
- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Data Byte Control:  $\overline{LB}$ : I/O<sub>1</sub>~ I/O<sub>8</sub>,  $\overline{UB}$ : I/O<sub>9</sub>~ I/O<sub>16</sub>
- Standard Pin Configuration:
  - K6R1016C1D-J : 44-SOJ-400
  - K6R1016C1D-T: 44-TSOP2-400BF
  - K6R1016C1D-E: 48-TBGA ( 6.0mm X 7.0mm )  
with 0.75 ball pitch
- Operating in Commercial and Industrial Temperature range.

### GENERAL DESCRIPTION

The K6R1016C1D is a 1,048,576-bit high-speed Static Random Access Memory organized as 65,536 words by 16 bits. The K6R1016C1D uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control ( $\overline{UB}$ ,  $\overline{LB}$ ). The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The K6R1016C1D is packaged in a 400mil 44-pin plastic SOJ or TSOP2 forward or 48-TBGA.

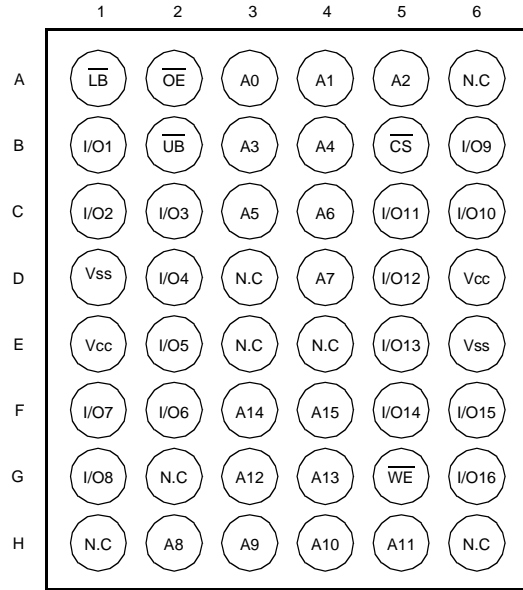
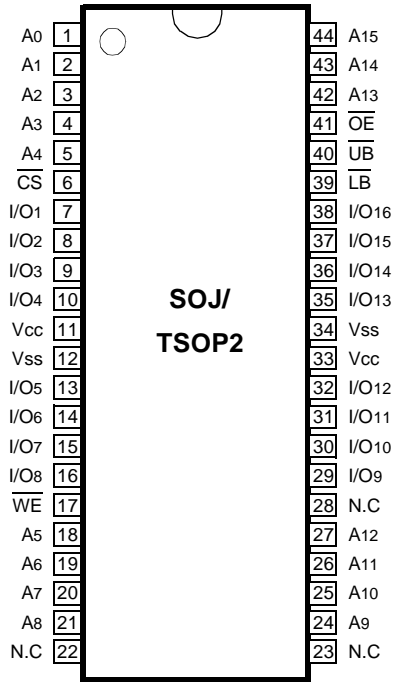
### FUNCTIONAL BLOCK DIAGRAM



### PIN FUNCTION

Pin Name	Pin Function
A <sub>0</sub> - A <sub>15</sub>	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{LB}$	Lower-byte Control(I/O <sub>1</sub> ~I/O <sub>8</sub> )
$\overline{UB}$	Upper-byte Control(I/O <sub>9</sub> ~I/O <sub>16</sub> )
I/O <sub>1</sub> ~ I/O <sub>16</sub>	Data Inputs/Outputs
V <sub>cc</sub>	Power(+5.0V)
V <sub>ss</sub>	Ground
N.C	No Connection

PIN CONFIGURATION(TOP VIEW)



48-TBGA ( Top View )

ABSOLUTE MAXIMUM RATINGS\*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-0.5 to V <sub>CC</sub> +0.5	V
Voltage on V <sub>CC</sub> Supply Relative to Vss	V <sub>CC</sub>	-0.5 to 7.0	V
Power Dissipation	P <sub>d</sub>	1	W
Storage Temperature	T <sub>STG</sub>	-65 to 150	°C
Operating Temperature	Commercial	T <sub>A</sub>	0 to 70
	Industrial	T <sub>A</sub>	-40 to 85

\* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS\*(T<sub>A</sub>= to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
Ground	V <sub>SS</sub>	0	0	0	V
Input High Voltage	V <sub>IH</sub>	2.2	-	V <sub>CC</sub> +0.5***	V
Input Low Voltage	V <sub>IL</sub>	-0.5**	-	0.8	V

\* The above parameters are also guaranteed at industrial temperature range.

\*\* V<sub>IL</sub>(Min) = -2.0V a.c(Pulse Width ≤ 8ns) for I ≤ 20mA.

\*\*\* V<sub>IH</sub>(Max) = V<sub>CC</sub> + 2.0V a.c(Pulse Width ≤ 8ns) for I ≤ 20mA.

## DC AND OPERATING CHARACTERISTICS\* (TA=0 to 70°C, VCC=5.0V±10%, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Max	Unit		
Input Leakage Current	ILI	VIN=VSS to VCC	-2	2	μA		
Output Leakage Current	ILO	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ VOUT=VSS to VCC	-2	2	μA		
Operating Current	Icc	Min. Cycle, 100% Duty CS=VIL, VIN=VIH or VIL, IOUT=0mA	Com.	10ns	-	65	mA
				12ns	-	55	
			Ind.	10ns	-	75	
				12ns	-	65	
Standby Current	ISB	Min. Cycle, $\overline{CS}=V_{IH}$	-	20	mA		
	ISB1	f=0MHz, $\overline{CS} \geq V_{CC}-0.2V$ , VIN ≥ VCC-0.2V or VIN ≤ 0.2V	-	5			
Output Low Voltage Level	VOL	IOL=8mA	-	0.4	V		
Output High Voltage Level	VOH	IOH=-4mA	2.4	-	V		

\* The above parameters are also guaranteed at industrial temperature range.

## CAPACITANCE\* (TA=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	CIO	VIO=0V	-	8	pF
Input Capacitance	CIN	VIN=0V	-	6	pF

\* Capacitance is sampled and not 100% tested.

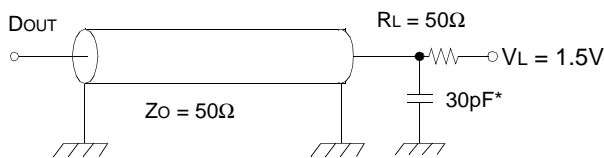
## AC CHARACTERISTICS (TA=0 to 70°C, VCC=5.0V±10%, unless otherwise noted.)

### TEST CONDITIONS\*

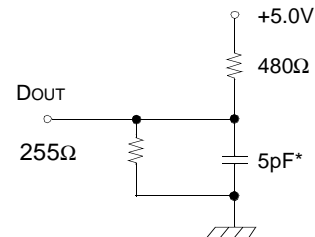
Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

\* The above test conditions are also applied at industrial temperature range.

Output Loads(A)



Output Loads(B)  
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



\* Capacitive Load consists of all components of the test environment.

\* Including Scope and Jig Capacitance

## READ CYCLE\*

Parameter	Symbol	K6R1016C1D-10		K6R1016C1D-12		Unit
		Min	Max	Min	Max	
Read Cycle Time	t <sub>RC</sub>	10	-	12	-	ns
Address Access Time	t <sub>AA</sub>	-	10	-	12	ns
Chip Select to Output	t <sub>CO</sub>	-	10	-	12	ns
Output Enable to Valid Output	t <sub>OE</sub>	-	5	-	6	ns
$\overline{UB}$ , $\overline{LB}$ Access Time	t <sub>BA</sub>	-	5	-	6	ns
Chip Enable to Low-Z Output	t <sub>LZ</sub>	3	-	3	-	ns
Output Enable to Low-Z Output	t <sub>OLZ</sub>	0	-	0	-	ns
$\overline{UB}$ , $\overline{LB}$ Enable to Low-Z Output	t <sub>BLZ</sub>	0	-	0	-	ns
Chip Disable to High-Z Output	t <sub>HZ</sub>	0	5	0	6	ns
Output Disable to High-Z Output	t <sub>OHZ</sub>	0	5	0	6	ns
$\overline{UB}$ , $\overline{LB}$ Disable to High-Z Output	t <sub>BHZ</sub>	0	5	0	6	ns
Output Hold from Address Change	t <sub>OH</sub>	3	-	3	-	ns
Chip Selection to Power Up Time	t <sub>PU</sub>	0	-	0	-	ns
Chip Selection to Power Down Time	t <sub>PD</sub>	-	10	-	12	ns

\* The above parameters are also guaranteed at industrial temperature range.

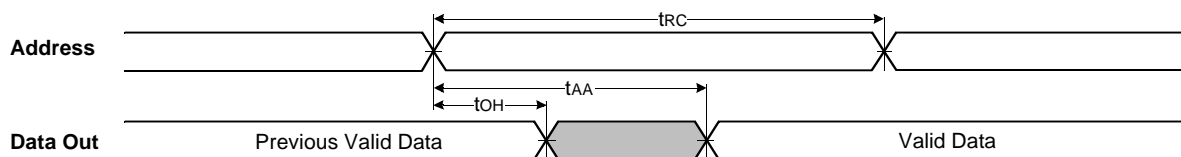
## WRITE CYCLE\*

Parameter	Symbol	K6R1016C1D-10		K6R1016C1D-12		Unit
		Min	Max	Min	Max	
Write Cycle Time	t <sub>WC</sub>	10	-	12	-	ns
Chip Select to End of Write	t <sub>CW</sub>	7	-	8	-	ns
Address Set-up Time	t <sub>AS</sub>	0	-	0	-	ns
Address Valid to End of Write	t <sub>AW</sub>	7	-	8	-	ns
Write Pulse Width( $\overline{OE}$ High)	t <sub>WP</sub>	7	-	8	-	ns
Write Pulse Width( $\overline{OE}$ Low)	t <sub>WP1</sub>	10	-	12	-	ns
$\overline{UB}$ , $\overline{LB}$ Valid to End of Write	t <sub>BW</sub>	7	-	8	-	ns
Write Recovery Time	t <sub>WR</sub>	0	-	0	-	ns
Write to Output High-Z	t <sub>WHZ</sub>	0	5	0	6	ns
Data to Write Time Overlap	t <sub>DW</sub>	5	-	6	-	ns
Data Hold from Write Time	t <sub>DH</sub>	0	-	0	-	ns
End of Write to Output Low-Z	t <sub>OW</sub>	3	-	3	-	ns

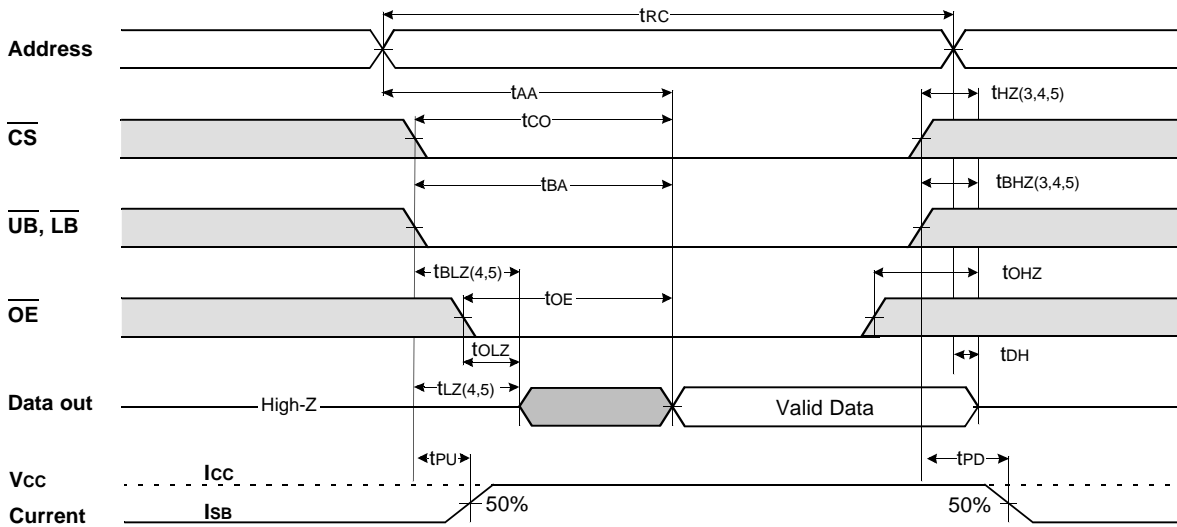
\* The above parameters are also guaranteed at industrial temperature range.

## TIMING DIAGRAMS

**TIMING WAVEFORM OF READ CYCLE(1)** (Address Controlled,  $\overline{CS}=\overline{OE}=V_{IL}$ ,  $\overline{WE}=V_{IH}$ ,  $\overline{UB}$ ,  $\overline{LB}=V_{IL}$ )



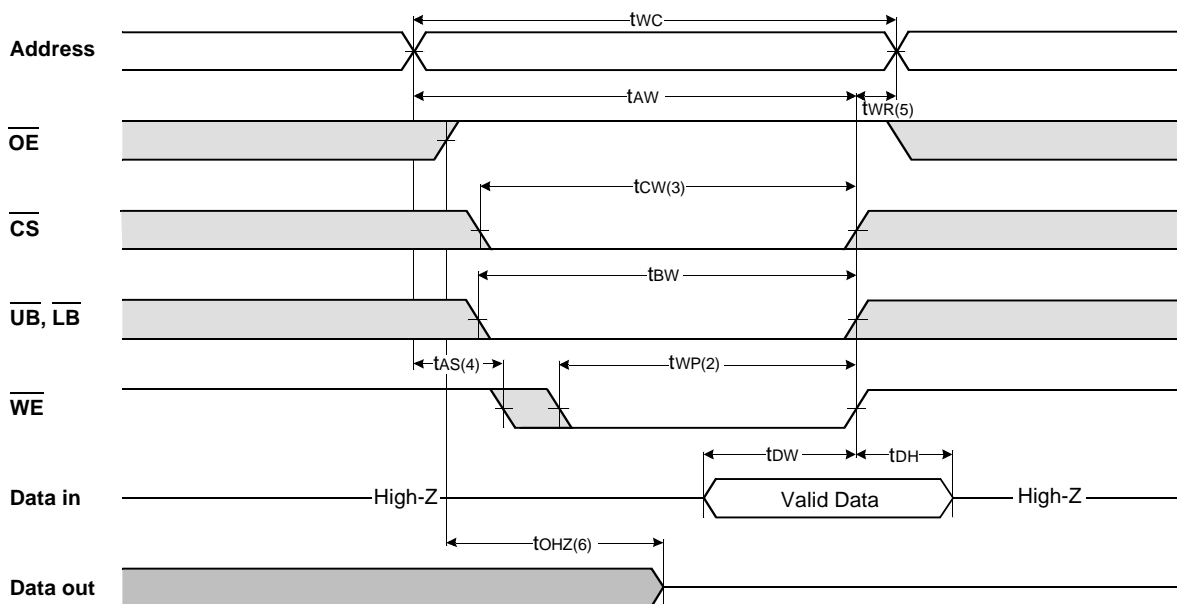
**TIMING WAVEFORM OF READ CYCLE(2) ( $\overline{WE}=V_{IH}$ )**



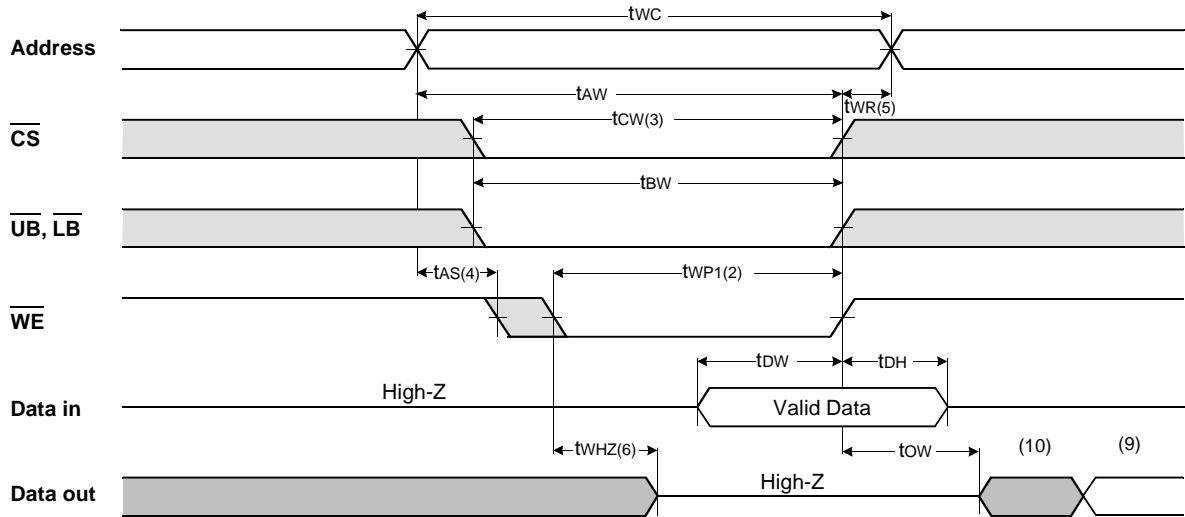
**NOTES(READ CYCLE)**

1.  $\overline{WE}$  is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit condition and are not referenced to  $V_{OH}$  or  $V_{OL}$  levels.
4. At any given temperature and voltage condition,  $t_{HZ}(\text{Max.})$  is less than  $t_{LZ}(\text{Min.})$  both for a given device and from device to device.
5. Transition is measured  $\pm 200\text{mV}$  from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with  $\text{CS}=\text{V}_{IL}$ .
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

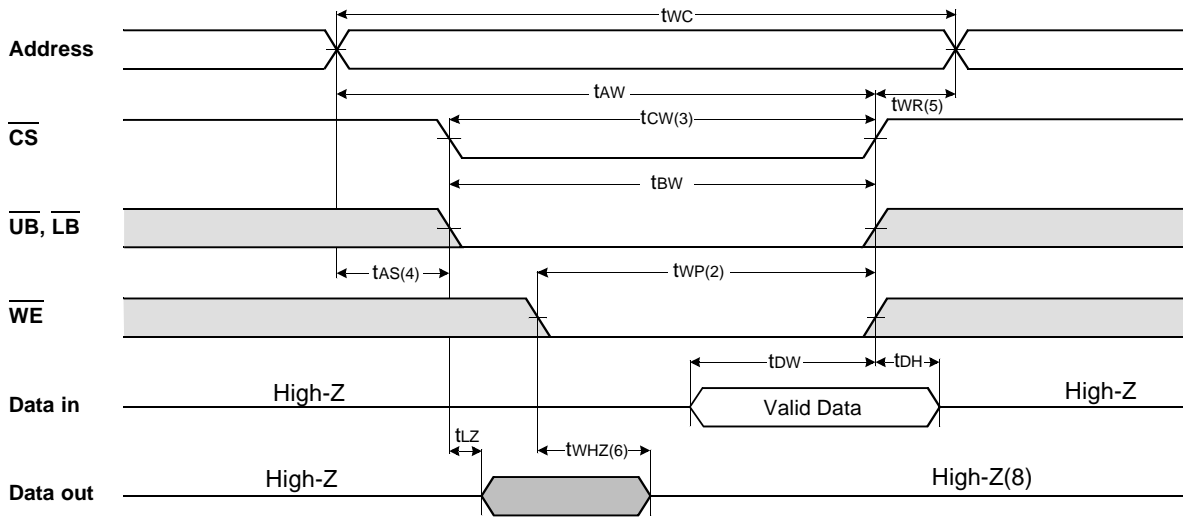
**TIMING WAVEFORM OF WRITE CYCLE(1) ( $\overline{OE}=\text{Clock}$ )**



TIMING WAVEFORM OF WRITE CYCLE(2) ( $\overline{OE}$  =Low fixed)

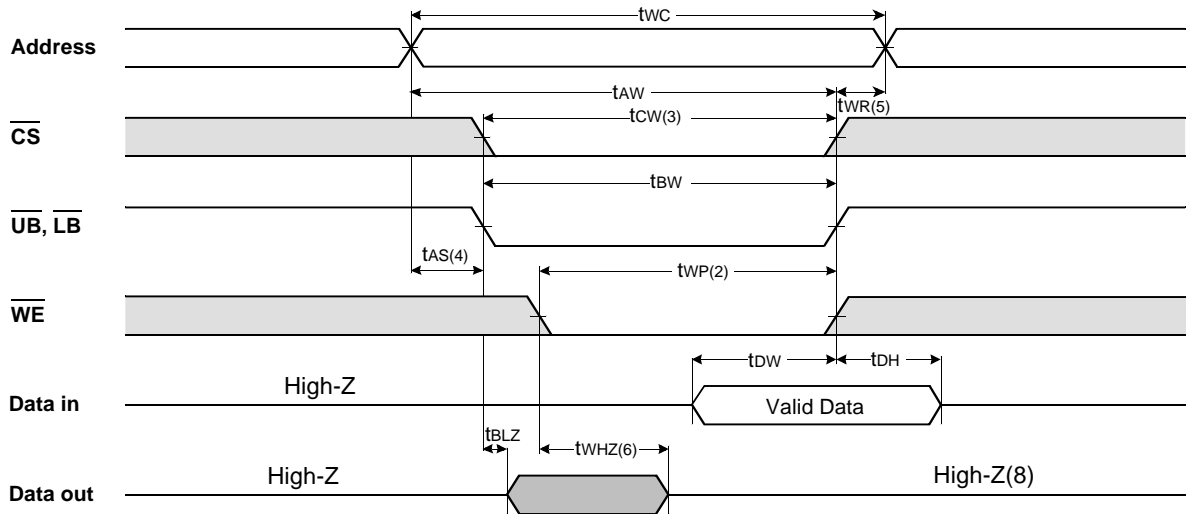


TIMING WAVEFORM OF WRITE CYCLE(3) ( $\overline{CS}$ =Controlled)





TIMING WAVEFORM OF WRITE CYCLE(4) ( $\overline{UB}$ ,  $\overline{LB}$  Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low CS, WE, LB and UB. A write begins at the latest transition CS going low and WE going low; A write ends at the earliest transition CS going high or WE going high. tWP is measured from the beginning of write to the end of write.
3. tcw is measured from the later of CS going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS or WE going high.
6. If OE, CS and WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If CS goes low simultaneously with WE going or after WE going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When CS is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O Pin		Supply Current
						I/O1~I/O8	I/O9~I/O16	
H	X	X*	X	X	Not Select	High-Z	High-Z	ISB, ISB1
L	H	H	X	X	Output Disable	High-Z	High-Z	Icc
L	X	X	H	H	Read	DOUT	High-Z	Icc
L	H	L	L	H		High-Z	DOUT	
L	H	L	L	L		DOUT	DOUT	
L	L	X	L	H	Write	DIN	High-Z	Icc
L	L	X	H	L		High-Z	DIN	
L	L	X	L	L		DIN	DIN	

\* X means Don't Care.

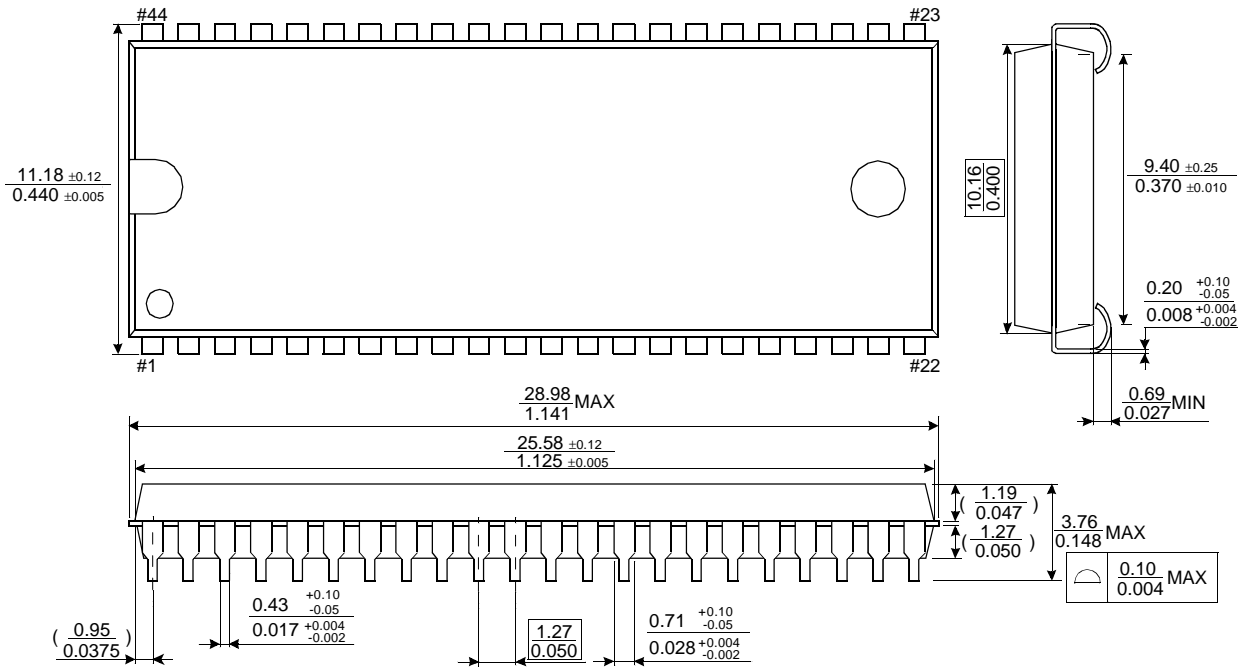
# K6R1016C1D

# CMOS SRAM

## PACKAGE DIMENSIONS

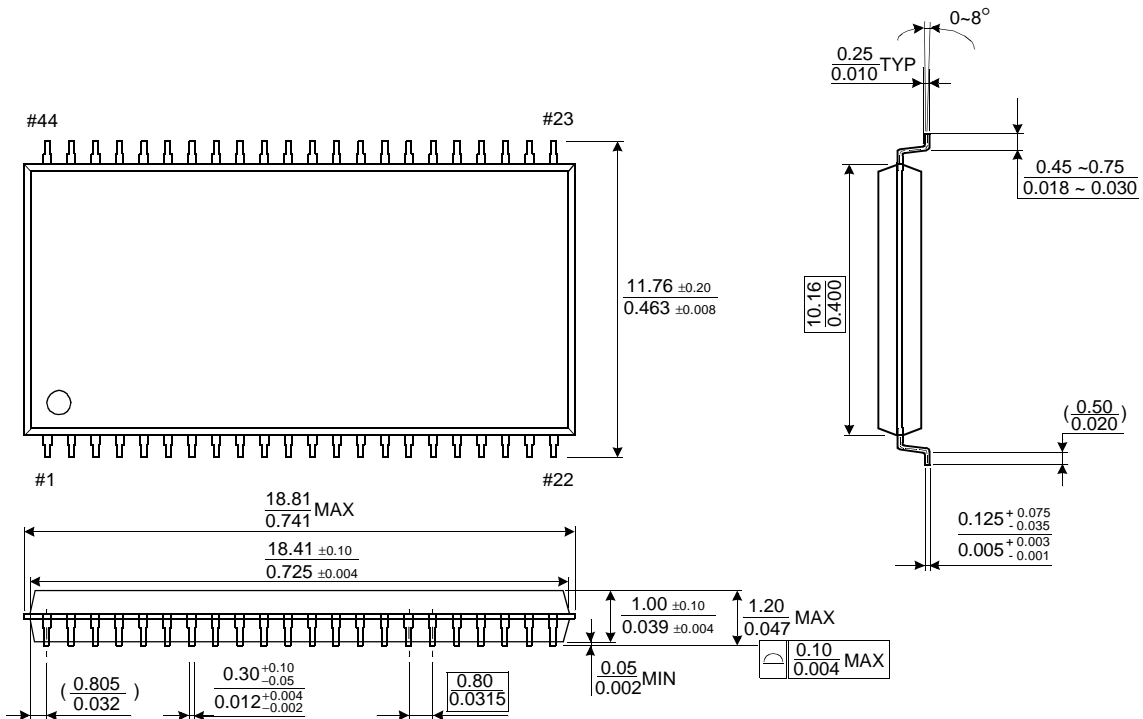
Units: millimeters/Inches

### 44-SOJ-400



### 44-TSOP2-400BF

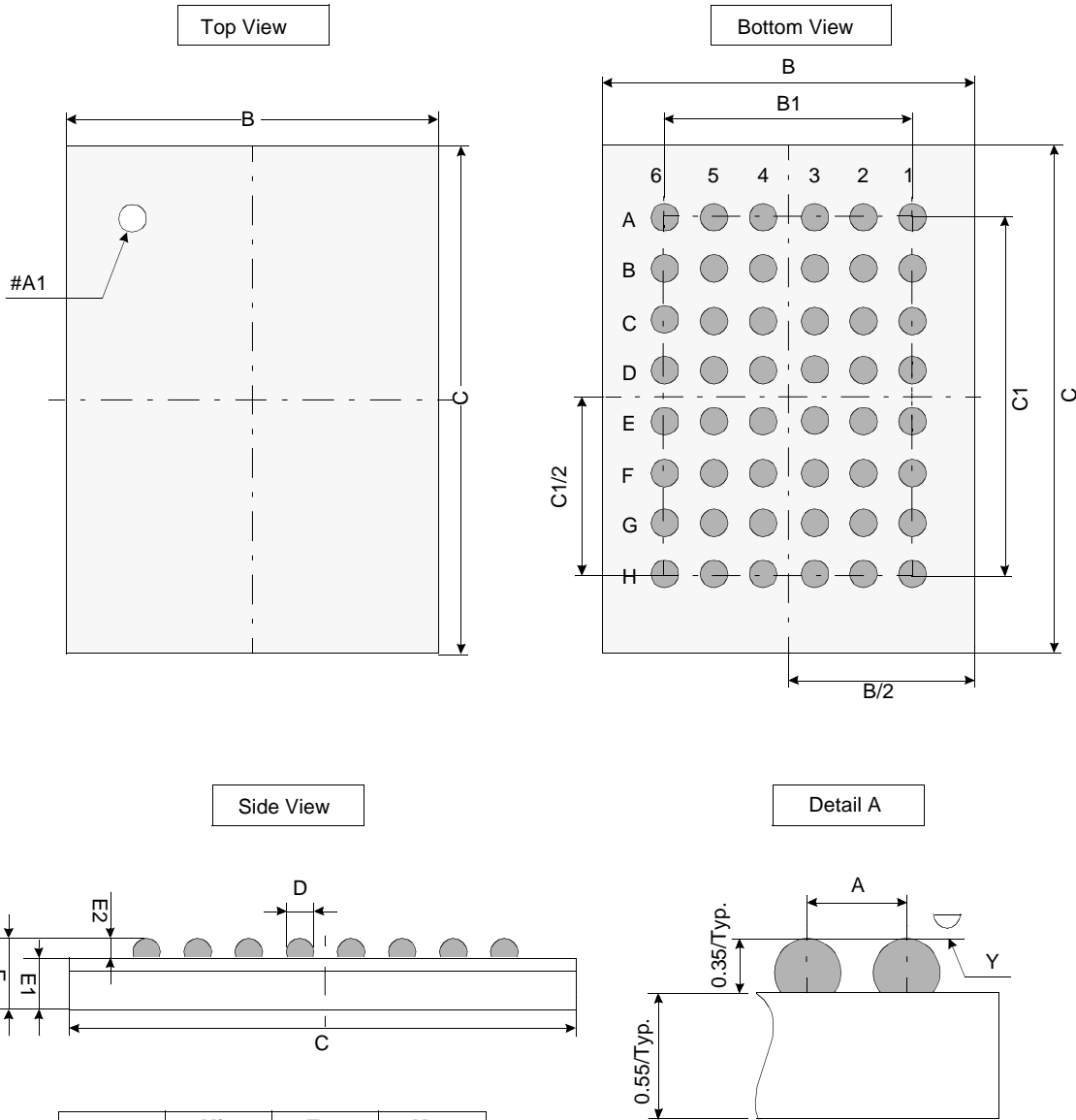
Units: millimeters/Inches



## PACKAGE DIMENSION

Unit: millimeters

48 TAPE BALL GRID ARRAY(0.75mm ball pitch)



	Min	Typ	Max
A	-	0.75	-
B	5.90	6.00	6.10
B1	-	3.75	-
C	6.90	7.00	7.10
C1	-	5.25	-
D	0.40	0.45	0.50
E	0.80	0.90	1.00
E1	-	0.55	-
E2	0.30	0.35	0.40
Y	-	-	0.08

### Notes.

1. Bump counts: 48(8 row x 6 column)
2. Bump pitch: (x,y)=(0.75 x 0.75)(typ.)
3. All tolerance are +/-0.050 unless otherwise specified.
4. Typ: Typical
5. Y is coplanarity: 0.08(Max)