500 MHz, Variable Gain Amplifier with Automatic Gain Control Detector

AD8367S

1.0. SCOPE

This specification documents the detail requirements for space qualified product manufactured on Analog Devices, Inc.'s QML certified line per MIL-PRF-38535 Level V except as modified herein.

The manufacturing flow described in the STANDARD SPACE LEVEL PRODUCTS PROGRAM brochure is to be considered a part of this specification. http://www.analog.com/aeroinfo

This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete data sheet for commercial product grades can be found at www.analog.com/AD8367.

2.0. Part Number: The complete part number(s) of this specification follows:

Part Number	Description
AD8367R703F	HDR Radiation tested for 100Krads, 500 MHz, Variable Gain Amplifier with Automatic Gain Control Detector
AD8367L703F	LDR Radiation tested for 50Krads, 500 MHz, Variable Gain Amplifier with Automatic Gain Control Detector

3.0. Case Outline

The case outline(s) are as designated in MIL-STD-1835 with package dimensions listed as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CDFP4-F16	16 lead	Bottom Brazed Flat Pack

Package: F			
Pin Number	Terminal Symbol	Pin Type	Pin Description
1	ICOM	Power	Signal Common. Connect to low impedance ground.
2	ICOM	Power	Signal Common. Connect to low impedance ground.
3	ENBL	Digital Input	A high activates the device.
4	INPT	Signal Input	200 Ω to ground.
5	MODE	Digital Input	Gain direction control. High for positive slope, low for negative slope. Must be low for AGC mode operation.
6	GAIN	Analog Input	Gain control voltage.
7	DETO	Analog Output	Detector output. Provides output current for RSSI function and AGC control.
8	ICOM	Power	Signal Common. Connect to low impedance ground.
9	OCOM	Power	Power Common. Connect to low impedance ground.
10	DECL	Analog Input	Output centering loop decoupling pin.
11	VOUT	Signal Output	To be externally ac-coupled to load.
12	VPSO	Power	Positive supply voltage. 3.0V to 5.25V. VPSI and VPSO are tied together internally with back to back PN junctions. They should be tied together externally and properly bypassed.
13	VPSI	Digital Output	Positive supply voltage. 3.0V to 5.25V.
14	HPFL	Analog Input	High pass filter connection. A capacitor to ground sets the corner frequency of the output offset control loop.
15	ICOM	Power	Signal Common. Connect to low impedance ground.
16	ICOM	Power	Signal Common. Connect to low impedance ground.
Lid	LID	NC	Not Connected, but can be externally connected to ground.

Figure 1 - Terminal connections.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.326.8703

AD8367S* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Data Sheet

- AD8367S: 500 MHz, Variable Gain Amplifier with Automatic Gain Control Detector Data Sheet

DESIGN RESOURCES

- AD8367S Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD8367S EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

4.0. Specifications

4.1. Absolute maximum ratings 1/

V_{PS} Supply Voltage (VPSO=VPSI=VPS) .....5.5 V
Enable (ENBL) pin voltage .....VPS + 200 mV
MODE select voltage (MODE) ..... VPS + 200 mV
V_{GAIN} control voltage (GAIN).....1.2 V
Input voltage (INPT) ..... ± 600 mV
Internal power dissipation .....200 mW
Storage Temperature Range..... – 65 °C to +150 °C
Lead Temperature (Soldering 10 Sec).....+300 °C
Maximum Junction Temperature (T_J).....125 °C
Thermal resistance, junction-to-case (θ_{JC}).....74 °C/W 2/
Thermal resistance, junction-to-ambient (θ_{JA}).....92 °C/W 2/

4.2. Recommended operating conditions

VPS Supply Voltage (VPSO=VPSI=VPS) .....3.0 V to 5.25 V
Ambient operating temperature range (T_A).....-55°C to +110°C

4.3. Nominal operating performance characteristics (T_A = 25°C, unless otherwise noted)

Minimum Frequency..... 10 MHz
Maximum Frequency..... 500 MHz

Input Stage (From INPT to ICOM)
Maximum Input to avoid input overload..... 700 mVpp
Input Resistance ..... 200 Ω

Output Stage (VOUT)
Output Centering DC Bias Voltage 3/ ..... VPSO/2 V
Output Source Resistance ..... 50 Ω
Maximum Output Voltage Swing R_L = 1 kΩ ..... 4.3 V_{p-p}
Maximum Output Voltage Swing R_L = 200 Ω ..... 3.5 V_{p-p}

Square Law Detector (DETO, CAGC = 100pF)
AGC Small Signal Response Time (6 dBm INPT step) ..... 1 us
AGC Step Response Time (INPT step down to <-36dBm from -16dBm, -55C<T_A<110C) ..... 6 us
AGC Step Response Time (INPT step up to -16dBm from <-36dBm, -55C<T_A<110C, VPS=5V) ..... 2 us
AGC Step Response Time (INPT step up to -16dBm from <-36dBm, -55C<T_A<110C, VPS=3V) ..... 5 us

Enable Interface (ENBL)
Enable Turn On Time (-55C<T_A<110C)
(Time delay following ENBL LO to HI transition until VOUT settled to <10% final value)..... 3 us
Enable Turn Off Time (-55C<T_A<110C)
(Time delay following ENBL HI to LO transition until I_S <2mA)..... 15 us

Gain Control Interface (GAIN)

10 MHz

Gain Range	45 dB
Maximum Gain (GAIN = 950 mV)	+42.5 dB
Minimum Gain (GAIN = 50 mV)	-2.5 dB
Scaling Factor (MODE = HI, 50 mV < GAIN < 950 mV)	+20 mV/dB
Scaling Factor (MODE = LO, 50 mV < GAIN < 950 mV)	-20 mV/dB
Gain Law Conformance	±0.2 dB
GAIN Step Response from 0 dB to 30 dB	300 ns
GAIN Step Response from 30 dB to 0 dB	300 ns

140 MHz

Maximum Gain	+43.5 dB
Minimum Gain	-3.6 dB
Gain Scaling Factor	19.7 mV/dB
Gain Intercept	-5.3 dB
Noise Figure (Maximum Gain)	7.4 dB
Output IP3 (f1 = 140 MHz, f2 = 141 MHz, V_{GAIN} = 0.5 V)	32.7 dBm
Output 1 dB Compression Point (V_{GAIN} = 0.5 V)	14.4 dBm

190 MHz

Maximum Gain	+43.5 dB
Minimum Gain	-3.8 dB
Gain Scaling Factor	19.6 mV/dB
Gain Intercept	-5.3 dB
Noise Figure (Maximum Gain)	7.5 dB
Output IP3 (f1 = 190 MHz, f2 = 191 MHz, V_{GAIN} = 0.5 V)	30.9 dBm
Output 1 dB Compression Point (V_{GAIN} = 0.5 V)	14.4 dBm

NOTES

1/ Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

2/ Measurement taken under absolute worst case condition and represents data taken with a thermal camera for highest power density location. See MIL-STD-1835 for average package Theta JC numbers.

3/ The output dc centering voltage is normally set at $V_{PS}/2$ and can be adjusted by applying a voltage to DECL.

TABLE I – ELECTRICAL PERFORMANCE CHARACTERISTICS

Parameter See notes at end of table	Symbol	Conditions 1/ Unless Otherwise Specified	Sub-Group	Limit Min	Limit Max	Units
POWER and CONTROL INTERFACE 2/						
Total Supply Current	I_S	V_{PS} = 3 V, V_{PS} = 5 V, V_{PS} = 5.25 V	1,3		30	mA
			2		39	
		M,D,P,L,R	1		30	
Disable Supply Current	I_{DIS}	V_{ENBL} = 0.8 V	1,3		1.6	mA
			2		1.8	
		M,D,P,L,R	1		1.6	
ENBL input logic low	$V_{IL\ ENBL}$		1,2,3		0.8	V
		M,D,P,L,R	1		0.8	
ENBL input logic high	$V_{IH\ ENBL}$		1,2,3	2.8		V
		M,D,P,L,R	1	2.8		
ENBL input low current	$I_{IL\ ENBL}$	V_{ENBL} = 0 V	1,2,3		2	µA
		M,D,P,L,R	1		2	
ENBL input low current	$I_{IL\ ENBL}$	V_{ENBL} = 0.8 V	1,2,3		5	µA
		M,D,P,L,R	1		5	
ENBL input high current	$I_{IH\ ENBL}$	V_{ENBL} = 2.8 V	1,2,3		20	µA
		M,D,P,L,R	1		20	
ENBL input high current	$I_{IH\ ENBL}$	V_{ENBL} = V_{PS} = 3 V	1,2,3		20	µA
		M,D,P,L,R	1		20	
ENBL input high current	$I_{IH\ ENBL}$	V_{ENBL} = V_{PS} = 5 V	1,2,3		40	µA
		M,D,P,L,R	1		40	
MODE input logic low	$V_{IL\ MODE}$		1,2,3		0.4	V
		M,D,P,L,R	1		0.4	
MODE input logic high	$V_{IH\ MODE}$		1,2,3	2.4		V
		M,D,P,L,R	1	2.4		
MODE input low current	$I_{IL\ MODE}$	V_{MODE} = 0 V	1,2,3		2	µA
		M,D,P,L,R	1		2	
MODE input low current	$I_{IL\ MODE}$	V_{MODE} = 0.4 V	1,2,3		2	µA
		M,D,P,L,R	1		2	
MODE input high current	$I_{IH\ MODE}$	V_{MODE} = 2.4 V	1,2,3		10	µA
		M,D,P,L,R	1		10	
MODE input high current	$I_{IH\ MODE}$	V_{MODE} = V_{PS} = 3 V	1,2,3		15	µA
		M,D,P,L,R	1		15	
MODE input high current	$I_{IH\ MODE}$	V_{MODE} = V_{PS} = 5 V	1,2,3		30	µA
		M,D,P,L,R	1		30	
GAIN input low current	I_{GAINL}	V_{GAIN} = 0 V	1,2,3		2	µA
		M,D,P,L,R	1		2	
GAIN input high current	I_{GAINH}	V_{GAIN} = 1.0 V	1,2,3		2	µA
		M,D,P,L,R	1		2	

TABLE I – ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Parameter See notes at end of table	Symbol	Conditions 1/ Unless Otherwise Specified	Sub-Group	Limit Min	Limit Max	Units
VGA MODE HIGH						
Midrange Gain 2/	$G_{midVGAH}$	P_{INPT} = -25dBm	4, 5, 6	18.5	22.5	dB
		M,D,P,L,R	4	18.5	22.5	
Gain Scaling Factor 3/	Slope $_{VGAH}$	f = 70MHz or 240 MHz	4, 5, 6	19	21	mV/dB
Gain Intercept 3/	Intrcp $_{VGAH70}$		4,5,6	-6.5	-3.5	dB
	Intrcp $_{VGAH5V240}$	V_{PS} = 5 V, f = 240 MHz	4,5,6	-6	-3	dB
	Intrcp $_{VGAH3V240}$	V_{PS} = 3 V, f = 240 MHz	4,6	-6	-3	dB
			5	-8	-5	
Gain Law Conformance 3/	Lin $_{VGAH70}$		4, 5, 6	-0.5	0.5	dB
	Lin $_{VGAH240}$	f = 240 MHz	4,5,6	-2.0	1.5	dB
1dB Output Compression Point 2/ 3/	P1dB $_{VGAH5V70}$	V_{PS} = 5 V	4,5,6	12		dBm
	P1dB $_{VGAH3V70}$	V_{PS} = 3 V	4	6		dBm
			5	4		
			6	5		
	P1dB $_{VGAH5V240}$	V_{PS} = 5 V, f = 240 MHz	4	12		dBm
			5,6	11		
	P1dB $_{VGAH3V240}$	V_{PS} = 3 V, f = 240 MHz	4,6	5		dBm
			5	2		
Output Third Order Intercept 2/ 3/	OIP3 $_{VGAH5V70}$	V_{PS} = 5 V	4,6	33		dBm
			5	25		
	OIP3 $_{VGAH3V70}$	V_{PS} = 3 V	4	23		dBm
			5	12		
			6	26		
	OIP3 $_{VGAH5V240}$	V_{PS} = 5 V, f = 240 MHz	4	24		dBm
			5	19		
			6	22		
	OIP3 $_{VGAH3V240}$	V_{PS} = 3 V, f = 240 MHz	4	18		dBm
			5	9		
			6	19		
Noise Figure 3/	NF $_{VGAH70}$	V_{GAIN} = 1V	4		8.5	dB
			5		11	
			6		7	
	NF $_{VGAH5V240}$	V_{PS} = 5 V, V_{GAIN} = 1V, f = 240 MHz	4		10	dB
			5		12.5	
			6		8.5	
	NF $_{VGAH3V240}$	V_{PS} = 3 V, V_{GAIN} = 1V, f = 240 MHz	4		9.5	dB
			5		11.5	
			6		7.5	

TABLE I – ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Parameter See notes at end of table	Symbol	Conditions 1/ Unless Otherwise Specified	Sub-Group	Limit Min	Limit Max	Units
VGA MODE LOW						
Midrange Gain 2/	$G_{midVGAL5}$	P_{INPT} = -25dBm, V_{PS} = 5 V	4,6	19.5	23.0	dB
			5	21.0	24.5	
		M,D,P,L,R	4	19.5	23	
	$G_{midVGAL3}$	P_{INPT} = -25dBm, V_{PS} = 3 V	4,5,6	19.5	23	dB
		M,D,P,L,R	4	19.5	23	
Gain Scaling Factor 3/	$Slope_{VGAL}$	f = 70MHz or 240 MHz	4,5,6	-21	-19	mV/dB
Gain Intercept 3/	$Intrcp_{VGAL5V70}$	V_{PS} = 5 V	4,6	45	48	dB
			5	45.5	48.5	
	$Intrcp_{VGAL3V}$	V_{PS} = 3 V, f = 70MHz or 240 MHz	4,5,6	44.5	47.5	dB
	$Intrcp_{VGAL5V240}$	V_{PS} = 5 V, f = 240 MHz	4,6	45	48	dB
			5	46.5	49.5	
Gain Law Conformance 3/	Lin_{VGAL70}		4,5,6	-0.5	0.5	dB
	$Lin_{VGAL240}$	f = 240 MHz	4,5,6	-2.0	1.5	dB
AGC MODE LOW 4/						
Output Set Point	P_{OUTAGC}	P_{INPT} = -16dBm	4,5,6	3	6	dBm
		M,D,P,L,R	4	3	6	
Gain Scaling Factor 3/ 5/	$Slope_{AGCL}$		4,5,6	-21	-19	mV/dB
Gain Intercept 3/ 5/	$Intrcp_{AGCL5V70}$	V_{PS} = 5 V	4,6	44.5	47.5	dB
			5	45.5	48.5	
	$Intrcp_{AGCL3V70}$	V_{PS} = 3 V	4,5,6	44	47	dB
	$Intrcp_{AGCL5V240}$	V_{PS} = 5 V, f = 240 MHz	4,6	45	48	dB
			5	47.5	50.5	
	$Intrcp_{AGCL3V240}$	V_{PS} = 3 V, f = 240 MHz	4,6	45	48	dB
			5	43.5	46.5	
Gain Law Conformance 3/ 5/	Lin_{AGCL70}		4,5,6	-0.5	0.5	dB
	$Lin_{AGCL5V240}$	V_{PS} = 5 V, f = 240 MHz	4,5,6	-2.0	1.5	dB
	$Lin_{AGCL3V240}$	V_{PS} = 3 V, f = 240 MHz	4,5,6	-1.5	1.5	dB

TABLE I NOTES:

1/ Ta = +25C, Ta max = +110C, Ta min = -55C. Unless otherwise noted, Supply Voltage V_{VPSO} = V_{VPSI} = V_{PS} = 5V or 3V, V_{MODE} = 2.4V, V_{ENBL} = 2.8V, 100mV < V_{GAIN} < 900mV, f = 70MHz, system impedance Z_O = 200 Ω, and dBm values are relative to 50 Ω. AD8367R0703F is tested to the R total dose level while AD8367L0703F is tested to the L total dose level.

2/ V_{GAIN} = 500mV

3/ Parameter is part of device initial characterization which is only repeated after design and process changes or with subsequent wafer lots. Parameter not tested post irradiation.

4/ V_{GAIN} = V_{DETO}

5/ -36dBm < P_{INPT} < 2.5dBm, except at Vs =3V, f=240MHz and Ta = 110C then -33.5dBm < P_{INPT} < 2.5dBm.

.

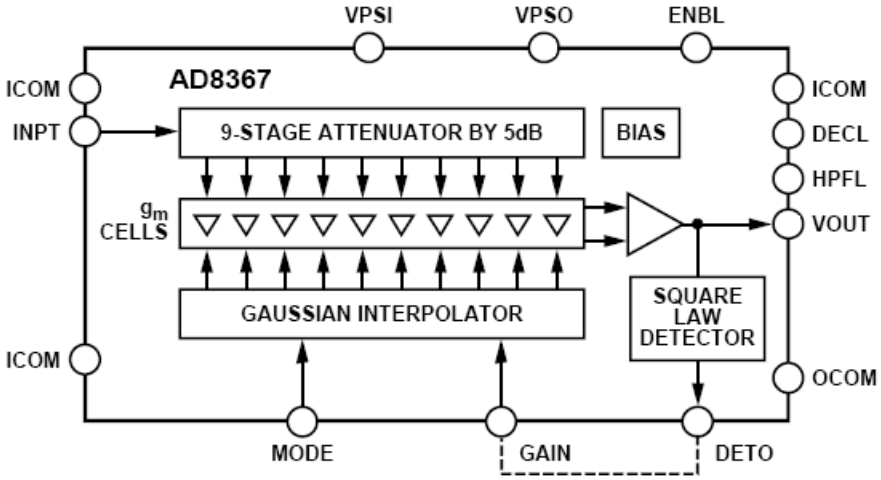

Figure 2 – Block Diagram.

TABLE IIA – ELECTRICAL TEST REQUIREMENTS:

Table IIA	
Test Requirements	Subgroups (in accordance with MIL-PRF-38535, Table III)
Interim Electrical Parameters	1
Final Electrical Parameters	1, 2, 3, 4, 5, 6 1/ 2/
Group A Test Requirements	1, 2, 3, 4, 5, 6
Group C end-point electrical parameters	1, 2, 3, 4, 5, 6 2/
Group D end-point electrical parameters	1, 2, 3, 4, 5, 6
Group E end-point electrical parameters	1, 4

Table IIA Notes:
1/ PDA applies to Table I subgroup 1 and Table IIB delta parameters.
2/ See Table IIB for delta parameters.
3/ Parameters marked with note 3/ in Table I are part of device initial characterization which is only repeated after design and process changes or with subsequent wafer lots.

TABLE IIB – BURN-IN/GROUP C DELTA LIMITS 1/

Parameters	Symbol	Condition	Delta limits	Units
Total Supply Current	I_S	V_{PS} = 3 V, V_{PS} = 5 V, V_{PS} = 5.25 V	±1.0	mA
Disable Current	I_{DIS}	V_{ENBL} = 0.8 V	±0.12	mA
ENBL input low current	$I_{IL\ ENBL}$	V_{ENBL} = 0 V, V_{ENBL} = 0.8 V	±0.4	µA
ENBL input high current	$I_{IH\ ENBL}$	V_{ENBL} = 2.8 V, V_{ENBL} = V_{PS}	±1.0	µA
MODE input low current	$I_{IL\ MODE}$	V_{MODE} = 0 V, V_{MODE} = 0.4 V	±0.4	µA
MODE input high current	$I_{IH\ MODE}$	V_{MODE} = 2.4 V, V_{MODE} = V_{PS}	±1.0	µA
GAIN input low current	I_{GAINL}	V_{GAIN} = 0 V	±0.4	µA
GAIN input high current	I_{GAINH}	V_{GAIN} = 1.0 V	±0.4	µA

1/ Ta = +25C, Unless otherwise noted, Supply Voltage V_{VPSO} = V_{VPSI} = V_{PS} = 3V or 5V, V_{MODE} = 2.4V, V_{ENBL} = 2.8V, V_{GAIN} = 0.5V.

5.0. BURN-IN, LIFE TEST, AND RADIATION

5.1. Burn-in test circuit, Life Test circuit

The test conditions and circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 test condition D of MIL-STD-883. Burn-in is performed at $T_J \geq +125°C$.

HTRB is not applicable for this drawing.

5.2. Radiation exposure circuit.

The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request. For the AD8367R703F, total dose irradiation testing to 100Krads (R level) shall be performed in accordance with MIL-STD-883 method 1019, condition A. For the AD8367L703F, total dose irradiation testing to 50Krads (L level with 50% for 75Krads total) shall be performed in accordance with MIL-STD-883 method 1019, condition D.

6.0. MIL-PRF-38535 QMLV EXCEPTIONS

6.1 Final test temperature range is -55°C to 110°C. No testing at +125°C.

6.2 240 hour Burn-in and 1000 hour Group C Life test performed at $T_J \geq 125°C$ ($T_A = +110°C$).

7.0. Application Notes

GENERAL DESCRIPTION

The AD8367S is a high performance 45 dB variable gain amplifier with linear-in-dB gain control for use from low frequencies up to several hundred megahertz. The range, flatness, and accuracy of the gain response are achieved using Analog Devices' X-AMP architecture, a powerful proprietary concept for variable gain applications that far surpasses what can be achieved using competing techniques.

The input is applied to a 9-stage, 200 Ω resistive ladder network. Each stage has 5 dB of loss, giving a total attenuation of 45 dB. At maximum gain, the first tap is selected; at progressively lower gains, the tap moves smoothly and continuously toward higher attenuation values. The attenuator is followed by a 42.5 dB fixed gain feedback amplifier – essentially an operational amplifier with a gain bandwidth product of 100 GHz – and is very linear, even at high frequencies. The output third order intercept is +20 dBV minimum at 70 MHz (+27 dBm, re 200 Ω), measured at an output level of 1 V p-p with VPS = 5 V.

The analog gain-control input is scaled at 20 mV/dB and runs from 50 mV to 950 mV. This corresponds to a gain of -2.5 dB to +42.5 dB, respectively, when the gain up mode is selected and +42.5 dB to -2.5 dB, respectively, when the gain down mode is selected. The gain down, or inverse mode, must be selected when operating in AGC mode in which an integrated square-law detector with an internal setpoint is used to level the output to 354 mV rms, regardless of the crest factor of the output signal. A single external capacitor sets up the AGC loop averaging time.

The AD8367S can be powered on or off by a voltage applied to the ENBL pin. When this voltage is logic LO, the total power dissipation drops into the single digit milliwatt range. For logic HI, the chip powers up rapidly to its normal quiescent current of 26 mA at 25C.

THEORY OF OPERATION

The AD8367S is a variable gain, single-ended, IF amplifier based on Analog Devices' patented X-AMP architecture. It offers accurate gain control with a 45dB span and a 3 dB bandwidth of 500MHz. It can be configured as a traditional VGA with 50 dB/V gain scaling or as an AGC amplifier by using the built in rms detector. Figure 3 is a simplified block

diagram of the amplifier. The main signal path consists of a voltage controlled 0 dB to 45 dB variable attenuator followed by a 42.5 dB fixed gain amplifier. The AD8367S is designed to operate optimally in a 200 Ω impedance system.

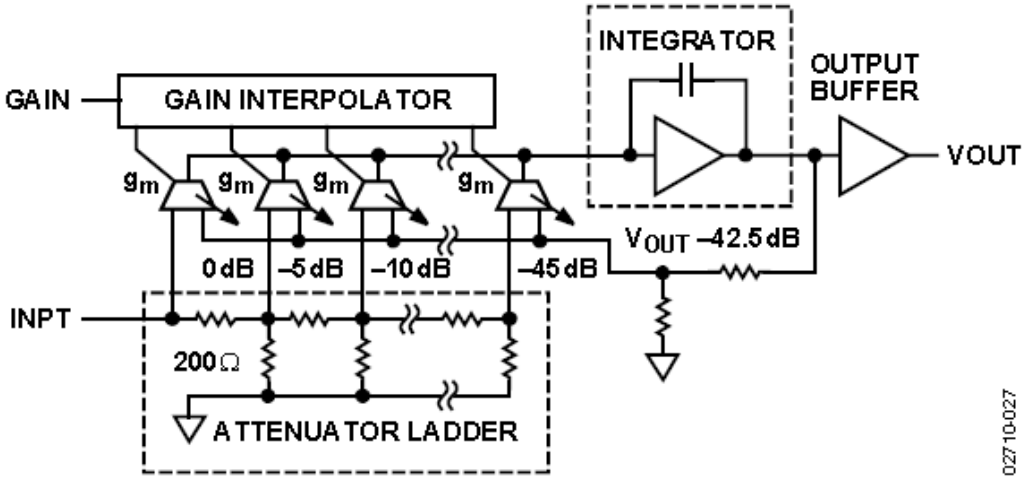

Figure 3 Simplified Architecture

INPUT ATTENUATOR AND GAIN CONTROL

The variable attenuator consists of a 200 Ω single-ended resistive ladder that is comprised of nine 5 dB sections and an interpolator that selects the attenuation factor. Each tap point down the ladder network further attenuates the input signal by a fixed decibel factor. Gain control is achieved by sensing different tap points with variable transconductance stages. Based on the gain control voltage, an interpolator selects which stages are active. For example, if only the first stage is active, the 0 dB tap point is sensed; if the last stage is active, the 45 dB tap point is sensed. Attenuation levels that fall between tap points are achieved by having neighboring g_m stages active simultaneously, creating a weighted average of the discrete tap point attenuations. In this way, a smooth monotonic attenuation function is synthesized, that is, linear-in-dB with a very precise scaling.

The gain of the AD8367S can be an increasing or decreasing function of the control voltage, V_{GAIN}, depending on whether the MODE pin is pulled HI or LO. When the MODE pin is pulled HI, the gain increases with V_{GAIN}, as shown in Figure 4.

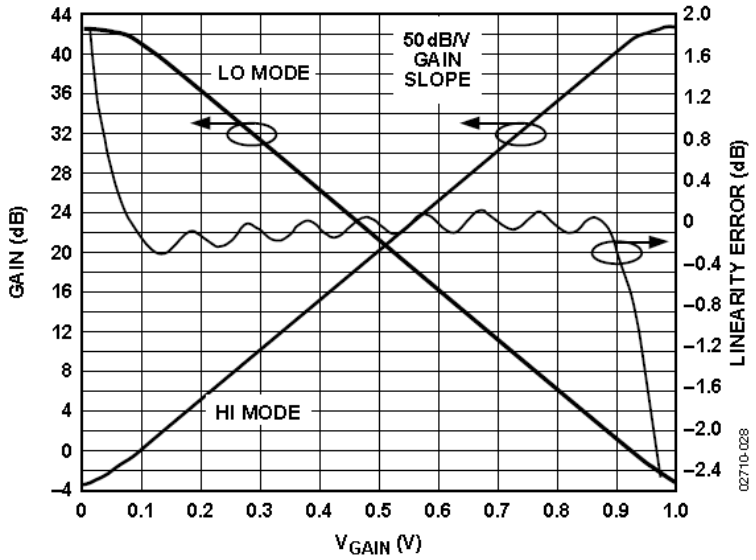

Figure 4. The gain function can be either an increasing or decreasing function of V_{GAIN}, depending on the MODE pin.

The ideal linear-in-dB scaled transfer function is given by

Equation 1 $Gain\ (dB) = 50 \times V_{GAIN} - 5$

where V_{GAIN} is expressed in volts.

Equation 1 contains the gain scaling factor of 50 dB/V (20 mV/dB) and the gain intercept of -5 dB, which represents the extrapolated gain for V_{GAIN} = 0 V. The gain ranges from -2.5 dB to +42.5 dB for V_{GAIN} ranging from 50 mV to 950 mV. The deviation from Equation 1, that is, the gain conformance error, is also illustrated in Figure 4. The ripples in the error are a result of the interpolation action between tap points. The AD8367S provides better than ±0.5 dB of conformance error over a 40 dB gain range at 70 MHz and better than +1.5/-2 dB at 240MHz over the extended ambient temperature range of -55C to 110C.

The gain is a decreasing function of V_{GAIN} when the MODE pin is LO. Figure 4 also illustrates this mode, which is described by

Equation 2 $Gain\ (dB) = 45 - 50 \times V_{GAIN}$

This gain mode is required in AGC applications using the built-in, square-law level detector.

INPUT AND OUTPUT INTERFACES

The AD8367S was designed to operate best in a 200 Ω impedance system. Its gain range, conformance law, and distortion assume that 200 Ω source and load impedances are used. Interfacing the AD8367S to other common impedances (from 50 Ω used at radio frequencies to 1 kΩ presented by data converters) can be accomplished using resistive or reactive passive networks, whose design depends on specific system requirements, such as bandwidth, return loss, noise figure, and absolute gain range.

The input impedance of the AD8367S is nominally 200 Ω, determined by the resistive ladder network. This presents a 200 Ω dc resistance to ground, and in cases where an elevated signal potential is used ac coupling is necessary. The input signal level should not exceed 700mV_{p-p} to avoid overloading the input stage. The output impedance is determined by an internal 50 Ω damping resistor, as shown in figure 5. Despite the fact that the output impedance is 50 Ω, the AD8367S should still be presented with a load of 200 Ω. This implies that the load is mismatched, but doing so preserves the distortion performance of the amplifier.

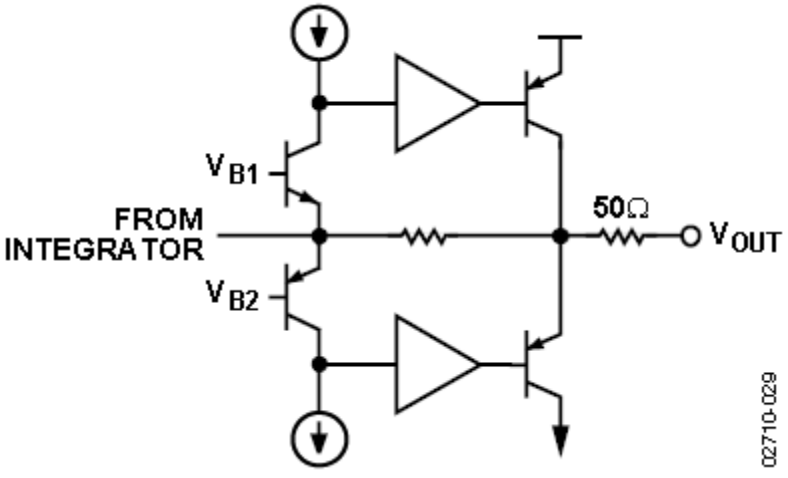

Figure 5. A 50 Ω resistor is added to the output to prevent package resonance.

POWER AND VOLTAGE METRICS

Although power is the traditional metric used in the analysis of cascaded systems, most active circuit blocks fundamentally respond to voltage. The relationship between power and voltage is defined by the impedance level. When input and output impedance levels are the same, power gain and voltage gain are identical. However, when impedance levels change between input and output, they differ. Thus, one must be very careful to use the appropriate gain for system chain analyses. Quantities such as OIP3 are quoted in dBVrms as well as dBm reference to 200 Ω and dBm reference to 50 Ω. The dBVrms unit is defined as decibels relative to 1 Vrms. In a 200 Ω environment, the conversion from dBVrms to dBm referenced to 200 Ω requires the addition of 7dB to the dBVrms value. For example, a 2 dBVrms level corresponds to 9 dBm relative to 200 Ω. The conversion from dBVrms to dBm referenced to 50 Ω requires the addition of 13 dB to the dBVrms value. For example, a 2 dBV_{rms} level corresponds to 15 dBm relative to 50 Ω. Another perhaps simpler way to express the conversion between these different units is given in Equation 3:

Equation 3: dBm re 50 = dBm re 200 + 6 = dBVrms + 13.

NOISE AND DISTORTION

Since the AD8367S consists of a passive variable attenuator followed by a fixed gain amplifier, the noise and distortion characteristics as a function of the gain voltage are easily predicted. The input-referred noise increases in proportion to the attenuation level. Figure 6 shows noise figure, NF, as a function of V_{GAIN}, for the MODE pin pulled HI. The minimum NF of 7.5 dB occurs at maximum gain and increases 1 dB for every 1 dB reduction in gain. In receiver applications, the minimum NF should occur at the maximum gain where the received signal presumably is weakest. At higher signal levels, a lower gain is needed, and the increased NF becomes less important.

The input-referred distortion varies in a similar manner to the noise. Figure 6 illustrates how the third-order intercept point at the input, IIP3, behaves as a function of V_{GAIN}. The highest IIP3 of 20 dBVrms (27 dBm re 200 Ω) occurs at minimum gain. The IIP3 then decreases 1 dB for 1 dB increase in gain. At lower gain levels, a degraded IIP3 is acceptable. Overall, the dynamic range, represented by the difference between IIP3 and NF, remains reasonably constant as a function of gain. The output distortion and compression are essentially independent of the gain. At low gains, when the input level is high, input overload can occur, causing premature distortion.

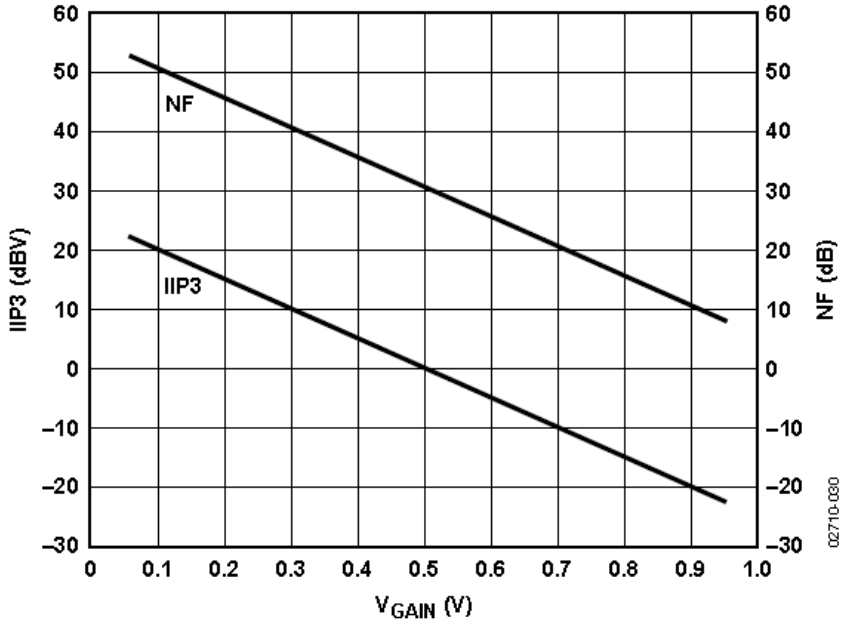

Figure 6. Noise Figure and Input Third-Order Intercept vs. Gain Voltage (R_{SOURCE} = 200 Ω)

OUTPUT CENTERING

To maximize the AC swing at the output of the AD8367S, the output level is centered midway between ground and the supply. This is achieved when the DECL pin is bypassed to ground via a shunt capacitor. The loop acts to suppress deviations from the reference at outputs below its corner frequency while not affecting signals above it, as shown in Figure 7. The maximum corner frequency with no external capacitor is 500 kHz. The corner frequency can be lowered by adding an external capacitor, C_{HP}:

Equation 4: $f_{HP}(kHz) = 10 / (C_{HP}(nF) + 0.02$

A 100 Ω resistor in series with the C_{HP} capacitor is recommended to de-Q the resonant tank that is formed by the bond-wire inductance and C_{HP}. Failure to insert this capacitor can potentially cause oscillations at higher frequencies at high gain settings.

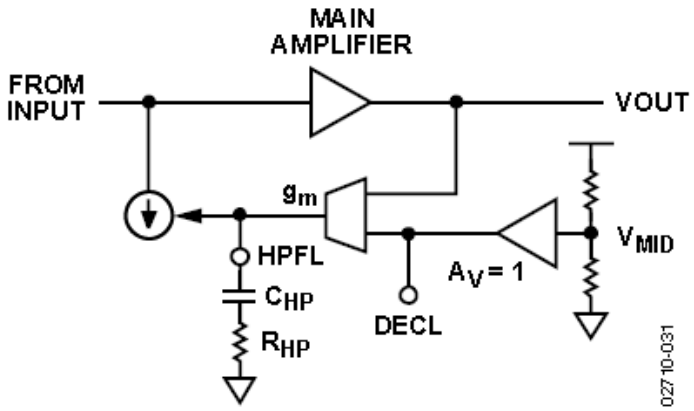

Figure 7. The dc output level is centered to midsupply by a control loop whose corner frequency is determined by C_{HP}.

RMS DETECTION

The AD8367S contains a square-law detector that senses the output signal and compares it to a calibrated setpoint of 354 mVrms, which corresponds to a 1 V_{p-p} sine wave. This set point is internally set and cannot be modified to change the AGC setpoint and the resulting VOUT level without using additional external components.

Any difference between the output and setpoint generates a current that is integrated by an external capacitor, C_{AGC}, connected from the DETO pin to ground, to provide an AGC control voltage. There is also an internal 5 pF capacitor on the DETO pin. The resulting voltage is used as an AGC bias. For this application, the MODE pin is pulled low and the DETO pin is tied to the GAIN pin. The output signal level is then regulated to 354 mVrms. The AGC bias represents a calibrated rms measure of the received signal strength (RSSI). Since in AGC mode the output signal is forced to the 354 mV_{rms} setpoint (-9.02 dBV_{rms}), Equation 2 can be recast to express the strength of the received signal, V_{IN-RMS}, in terms of the AGC bias V_{DETO}.

Equation 5: $V_{IN-RMS}(dBV_{rms}) = -54.02 + 50 \times V_{DETO}$

where -54.02 dBV_{rms} = -45 dB – 9.02 dBV_{rms}.

For small changes in input signal level, V_{DETO} responds with a characteristic single-pole time constant, τ_{AGC}, which is proportional to C_{AGC}.

Equation 6: T_{AGC} (us) = 10 x C_{AGC} (nF)

where the internal 5 pF capacitor is lumped with the external capacitor to give C_{AGC}.

APPLICATIONS

The AD8367S can be configured either as a VGA whose gain is controlled externally through the GAIN pin or as an AGC amplifier, using a supply voltage of 3V to 5.25V. The supply to the VPSO and VPSI pins should be decoupled using a low inductance, 0.1uF surface-mount, ceramic capacitor as close as possible to the device. Additional supply decoupling can be provided by small series resistors. A 10 nF capacitor from the DECL pin to the OCOM pin is recommended to decouple the output reference voltage.

INPUT AND OUTPUT MATCHING

The AD8367S is designed to operate in a 200 Ω impedance system. The output amplifier is a low output impedance voltage buffer with a 50 Ω damping resistor to desensitize it from load reactance and parasitics. The quoted performance includes the voltage division between the 50 Ω resistor and the 200 Ω load. The AD8367S can be reactively matched to an impedance other than 200 Ω by using traditional step-up and step-down matching networks or high quality transformers.

STABILITY AND LAYOUT CONSIDERATIONS

In some applications, the printed circuit board (PCB) parasitics, in combination with the source impedance presented by the driving stage, can present some troublesome impedance at high frequency and can potentially un-stabilize the amplifier under certain extreme conditions, such as high gain at high temperature. To address such scenarios, it is recommended to include a series inductor on the INPT pin as close to the device as possible. This inductor forms a snubbing network to choke out high frequencies from entering the device. A value of 10 nH or higher is recommended to minimize high frequency energy on the INPT pin. This inductor also minimizes the negative impact due to reflective source conditions at high RF frequencies to ensure the amplifier operates unconditionally stable to maintain typical device performance.

It is also recommended that stitching be used to tie ground planes together around input and output signal traces, and under the AD8367S. This stitching forms a low impedance ground plane to ensure specified electrical performance and to reduce thermal resistance.

VGA OPERATION

The AD8367S is a general-purpose VGA suitable for use in a wide variety of applications where voltage control of gain is needed. While having a 500 MHz bandwidth, its use is not limited to high frequency signal processing. Its accurate, temperature- and supply-stable linear-in-dB scaling is valuable wherever it is important to have a more dependable response to the control voltage that is usually offered by VGAs of this sort. For example, there is no preclusion to its use in speech bandwidth systems.

Figure 8 shows the basic connections. The C_{HP} capacitor at the HPFL pin can be used to alter the high-pass corner frequency of the signal path and is associated with the offset control loop that eliminates the inherent variation in the internal dc balance of the signal path as the gain is varied (offset ripple). This frequency should be chosen to be about a decade below the lowest frequency component of the signal. If made much lower than necessary, the offset loop is not able to track the variations that occur when there are rapid changes in V_{GAIN}. The control of offset is important even when the output is ac-coupled because of the potential reduction of the upper and lower voltage range at this pin.

However, in many applications these components are unnecessary because an internal network provides a default high-pass corner frequency of about 500 kHz. For C_{HP} = 1 nF, the modified corner is at about 10 kHz; it scales downward with increasing capacitance. Figure 9 shows representative response curves for the indicated component values.

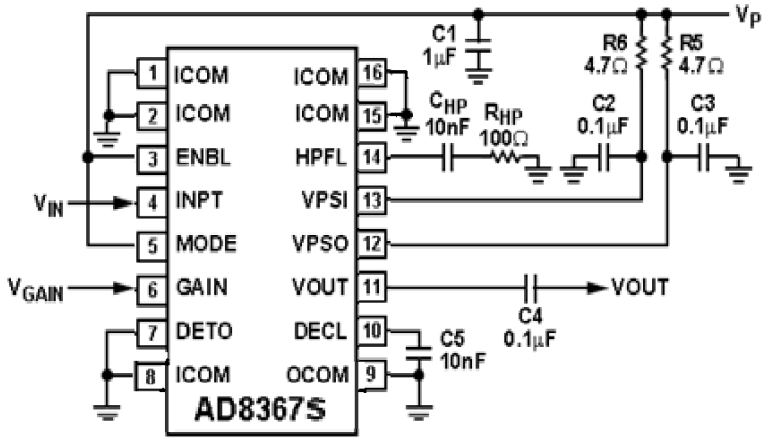

Figure 8. Basic connections for Voltage Controlled Gain mode.

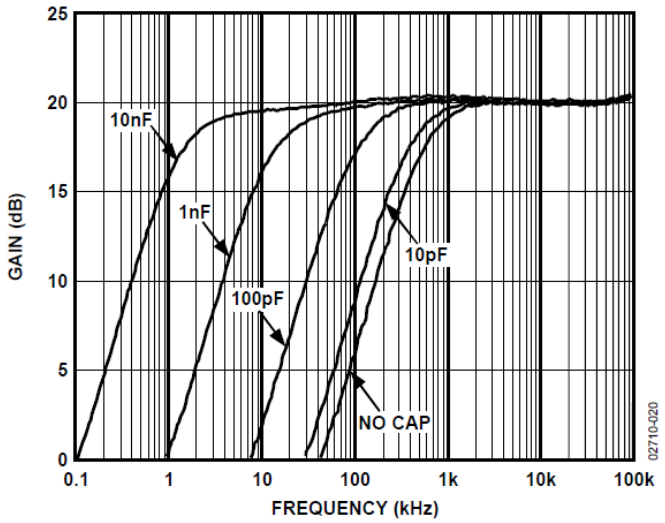

Figure 9. Gain vs. Frequency for Multiple Values of HPFL Capacitor ag V_{GAIN} = 500mV.

AGC OPERATION

The AD8367S can be used as an AGC amplifier, as shown in Figure 10. For this application, the accurate internal, square-law detector is employed. The output of this detector is a current that varies in polarity, depending on whether the rms value of the output is greater to or less than its internally-determined setpoint of 354 mV_{rms}. This is 1 V_{p-p} for sine-wave signals, but the peak amplitude for other signals, such as Gaussian noise, or those carrying complex modulation, is invariably somewhat greater. However, for all waveforms having a crest factor of <5, and when using a supply voltage of 4.5 V to 5.25V, the rms value is correctly measured and delivered at V_{OUT}. When using lower supplies, the rms value of V_{OUT} is unaffected (the setpoint is determined by a band gap reference), but the peak crest factor capacity is reduced.

The GAIN pin is connected to the base of a transistor internally and thus requires less than 2 uA of current drive. The output of the detector is delivered to the DETO pin. The detector can source up to 60uA and can sink up to 11 uA. For a sine-wave output signal, and under conditions where the AGC loop is settled, the detector output also takes the form of a sine-wave, but at twice the frequency and having a mean value of 0. If the input to the amplifier increases, the mean of this current also increases and charges the external loop filter capacitor, C_{AGC}, toward more positive voltages. Conversely, a reduction in V_{OUT} below the setpoint of 354 mV_{rms} causes this voltage to fall toward ground. The capacitor voltage is the AGC bias; this can be used as a received signal strength indicator (RSSI) output and is scaled exactly as V_{GAIN}, that is, 20 mV/dB.

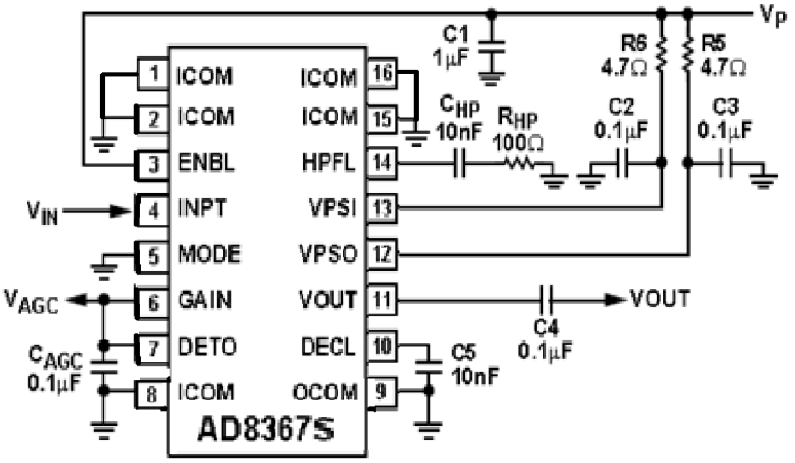

Figure 10. Basic connections for AGC operation.

A valuable feature of using a square law detector is that the RSSI voltage is a true reflection of signal power and can be converted to an absolute power measurement for any given source impedance. The AD8367S can thus be employed as a true-power meter, or decibel-reading ac voltmeter, as distinct from its basic amplifier function.

The AGC mode of operation requires that the correct gain direction is chosen. Specifically, the gain must fall as V_{AGC} increases to restore the needed balance against the setpoint. Therefore, the MODE pin must be pulled LO. This accurate leveling function is shown in Figure 11, where the rms output is held to within 0.1 dB of the setpoint for >35 dB range of input levels.

The dynamics of this loop are controlled by C_{AGC} acting in conjunction with an on-chip equivalent resistance, R_{AGC}, of 10 kΩ which form an effective time-constant $T_{AGC} = R_{AGC} \times C_{AGC}$. The loop thus operates as a single-pole system with a loop bandwidth of $1/(2\pi T_{AGC})$. Because the gain control function is linear in decibels, this bandwidth is independent of the absolute signal level. Figure 12 illustrates the loop dynamics for a 30 dB change in input signal level with C_{AGC} = 100 pF.

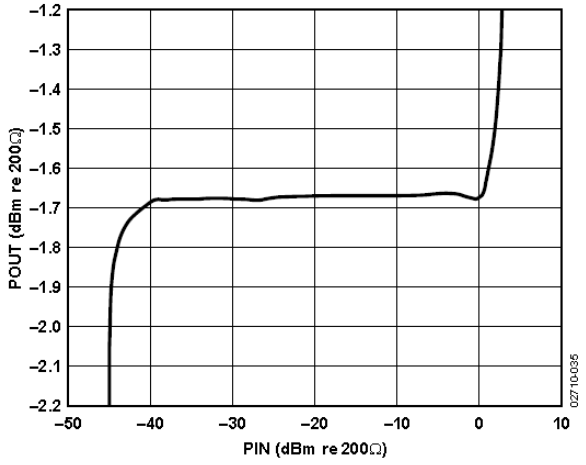

Figure 11: Leveling Accuracy of the AGC function.

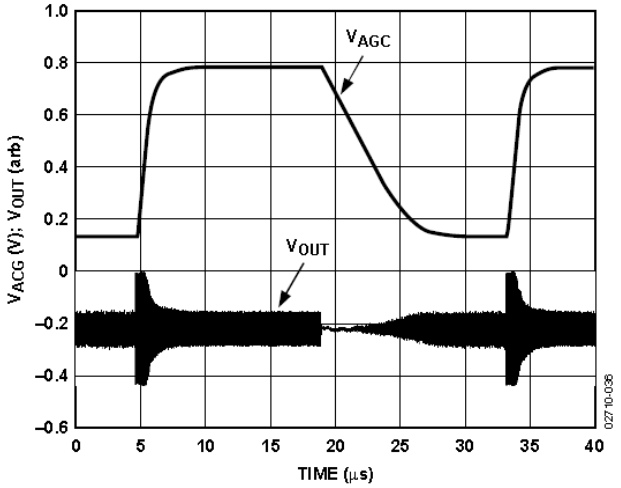

Figure 12: AGC Response to a 32 dB step in input level (f = 50 MHz)

It is important to understand that R_{AGC} does not act as if in shunt with C_{AGC}. Rather, the error-correction process is that of a true integrator, to guarantee an output that is exactly equal in rms amplitude to the specified setpoint. For large changes in input level, the integrating action of this loop is most apparent. The slew rate of V_{AGC} is determined by the peak output current from the detector and the capacitor. Thus, for a representative value of C_{AGC} = 3 nF, this rate is about 20 V_{rms} or 10 dB/us, while the small-signal bandwidth is 1 kHz.

Most AGC loops incorporating a true error-integrating technique have a common weakness. When driven from an increasingly larger signal, the AGC bias increases to reduce the gain. However, eventually the gain falls to its minimum value, for which further increase in this bias has no effect on the gain. That is, the voltage on the loop capacitor is forced progressively higher because the detector output is a current, and the AGC bias is its integral. Consequently, there is always a precipitous increase in this bias voltage when the input to the AD8367S exceeds that value that overdrives the detector, and because the minimum gain is -2.5 dB, that happens for all inputs 2.5 dB greater than the setpoint of about 350 mV_{rms}. If possible, the user should ensure that this limitation is preserved, preferably with a guard-band of 5 dB to 10 dB below overload.

In some cases, if driven into AGC overload, the AD8367S requires unusually long times to recover; that is, the voltage at DETO remains at an abnormally high value and the gain is at its lowest value. To avoid this situation, it is recommended that a clamp be placed on the DETO pin, as shown in Figure 13.

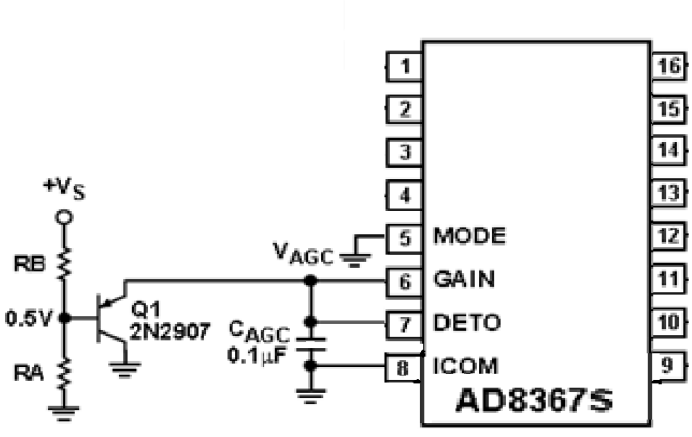

Figure 13. External Clamp to prevent AGC Overload. The resistive divider network, RA and RB, should be designed such that the base of Q1 is driven to 0.5 V.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Radiation Test option
AD8367R703F	−55°C to +110°C	16 Lead Bottom Brazed Flat Pack	X	HDR 100Krads, Method 1019, Condition A
AD8367L703F	−55°C to +110°C	16 Lead Bottom Brazed Flat Pack	X	LDR 50Krads, Method 1019, Condition D

8.0. Revision History

Rev	Description of Change	Date
A	Initial Release	10/10/2012
B	Add LDR radiation tested model	08/05/2013
C	correct typos to reflect actual conditions used	08/04/2014

8/14

ANALOG DEVICES

www.analog.com

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

AD8367R703F AD8367L703F