MCP6141/2/3/4

600 nA, Non-Unity Gain Rail-to-Rail Input/Output Op Amps

Features:

- Low Quiescent Current: 600 nA/amplifier (typ.)
- Gain Bandwidth Product: 100 kHz (typ.)
- Stable for gains of 10 V/V or higher
- Rail-to-Rail Input/Output
- Wide Supply Voltage Range: 1.4V to 5.5V
- Available in Single, Dual, and Quad
- Chip Select ($\overline{CS}$) with MCP6143
- Available in 5-lead and 6-lead SOT-23 Packages
- Temperature Ranges:
  - Industrial: -40°C to +85°C
  - Extended: -40°C to +125°C

Applications:

- Toll Booth Tags
- Wearable Products
- Temperature Measurement
- Battery Powered

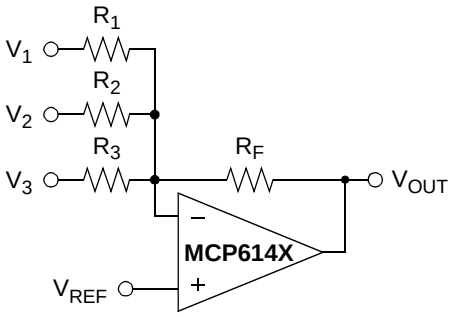
Available Tools:

- SPICE Macro Models (at www.microchip.com)
- FilterLab™ Software (at www.microchip.com)

Related Devices:

- MCP6041/2/3/4: Unity Gain Stable Op Amps

Typical Application



Inverting, Summing Amplifier

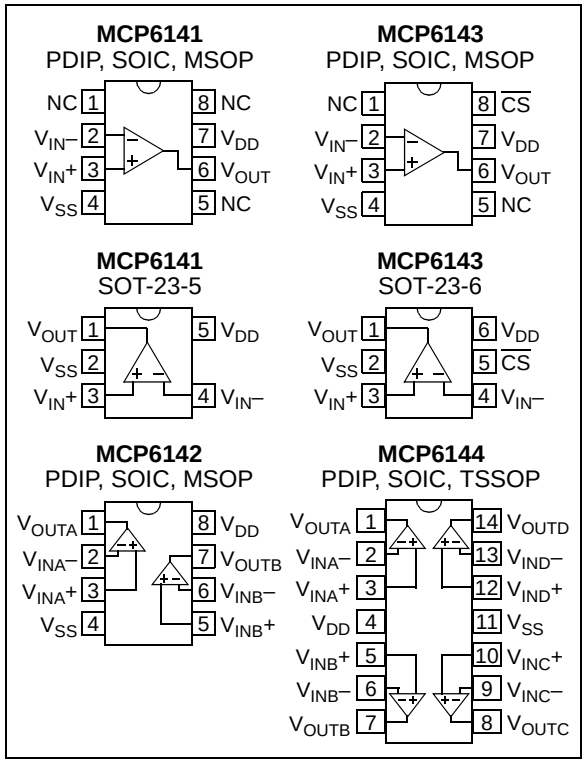
Description:

The MCP6141/2/3/4 family of non-unity gain stable operational amplifiers (op amps) from Microchip Technology Inc. operate with a single supply voltage as low as 1.4V, while drawing less than 1 µA (max.) of quiescent current per amplifier. These devices are also designed to support rail-to-rail input and output operation. This combination of features supports battery-powered and portable applications.

The MCP6141/2/3/4 amplifiers have a gain bandwidth product of 100 kHz (typ.) and are stable for gains of 10 V/V or higher. These specifications make these op amps appropriate for battery powered applications where a higher frequency response from the amplifier is required.

The MCP6141/2/3/4 family operational amplifiers are offered in single (MCP6141), single with Chip Select ($\overline{CS}$) (MCP6143), dual (MCP6142) and quad (MCP6144) configurations. The MCP6141 device is available in the 5-lead SOT-23 package, and the MCP6143 device is available in the 6-lead SOT-23 package.

Package Types



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

$V_{DD} - V_{SS}$ 7.0V
All Inputs and Outputs..... $V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Difference Input voltage ..... $|V_{DD} - V_{SS}|$
Output Short Circuit Current .....continuous
Current at Input Pins .....±2 mA
Current at Output and Supply Pins .....±30 mA
Storage Temperature.....–65°C to +150°C
Junction Temperature.....+150°C
ESD protection on all pins (HBM; MM) ..... ≥ 4 kV; 200V

† **Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +1.4V to +5.5V, V_{SS} = GND, T_A = 25°C, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, and R_L = 1 MΩ to $V_{DD}/2$.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input Offset						
Input Offset Voltage	V_{OS}	-3	—	+3	mV	$V_{CM} = V_{SS}$
Drift with Temperature	$\Delta V_{OS}/\Delta T_A$	—	±1.5	—	µV/°C	$V_{CM} = V_{SS}$, T_A = -40°C to +125°C
Power Supply Rejection	PSRR	70	85	—	dB	$V_{CM} = V_{SS}$
Input Bias Current and Impedance						
Input Bias Current	I_B	—	1	—	pA	
Industrial Temperature	I_B	—	20	100	pA	T_A = +85°
Extended Temperature	I_B	—	1200	5000	pA	T_A = +125°
Input Offset Current	I_{OS}	—	1	—	pA	
Common Mode Input Impedance	Z_{CM}	—	10^{13}||6	—	Ω||pF	
Differential Input Impedance	Z_{DIFF}	—	10^{13}||6	—	Ω||pF	
Common Mode						
Common Mode Input Range	V_{CMR}	V_{SS}–0.3	—	V_{DD}+0.3	V	
Common Mode Rejection Ratio	CMRR	62	80	—	dB	V_{DD} = 5V, V_{CM} = -0.3V to 5.3V
	CMRR	60	75	—	dB	V_{DD} = 5V, V_{CM} = 2.5V to 5.3V
	CMRR	60	80	—	dB	V_{DD} = 5V, V_{CM} = -0.3V to 2.5V
Open Loop Gain						
DC Open Loop Gain (large signal)	A_{OL}	95	115	—	dB	R_L = 50 kΩ to $V_{DD}/2$, V_{OUT} = 0.1V to V_{DD}–0.1V
Output						
Maximum Output Voltage Swing	V_{OL}, V_{OH}	V_{SS} + 10	—	V_{DD} – 10	mV	R_L = 50 kΩ to $V_{DD}/2$, 0.5V output overdrive
Linear Region Output Voltage Swing	V_{OVR}	V_{SS} + 100	—	V_{DD} – 100	mV	R_L = 50 kΩ to $V_{DD}/2$, $A_{OL} \geq$ 95 dB
Output Short Circuit Current	I_{SC}	—	2	—	mA	V_{DD} = 1.4V
	I_{SC}	—	20	—	mA	V_{DD} = 5.5V
Power Supply						
Supply Voltage	V_{DD}	1.4	—	5.5	V	
Quiescent Current per amplifier	I_Q	0.3	0.6	1.0	µA	I_O = 0

AC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +1.4V to +5.5V, V_{SS} = GND, T_A = 25°C, V_{CM} = V_{DD}/2, $V_{OUT} \approx V_{DD}/2$, R_L = 1 MΩ to $V_{DD}/2$, and C_L = 60 pF.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
AC Response						
Gain Bandwidth Product	GBWP	—	100	—	kHz	
Slew Rate	SR	—	24	—	V/ms	
Phase Margin	PM	—	60	—	°	G = +10
Noise						
Input Voltage Noise	E_{ni}	—	5.0	—	μV_{P-P}	f = 0.1 Hz to 10 Hz
Input Voltage Noise Density	e_{ni}	—	170	—	nV/√Hz	f = 1 kHz
Input Current Noise Density	i_{ni}	—	0.6	—	fA/√Hz	f = 1 kHz

MCP6143 CHIP SELECT ($\overline{CS}$) ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +1.4V to +5.5V, V_{SS} = GND, T_A = 25°C, V_{CM} = V_{DD}/2, $V_{OUT} \approx V_{DD}/2$, R_L = 1 MΩ to $V_{DD}/2$, and C_L = 60 pF.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
$\overline{CS}$ Low Specifications						
$\overline{CS}$ Logic Threshold, Low	V_{IL}	V_{SS}	—	V_{SS}+0.3	V	
$\overline{CS}$ Input Current, Low	I_{CSL}	—	5	—	pA	$\overline{CS}$ = V_{SS}
$\overline{CS}$ High Specifications						
$\overline{CS}$ Logic Threshold, High	V_{IH}	V_{DD}–0.3	—	V_{DD}	V	
$\overline{CS}$ Input Current, High	I_{CSH}	—	5	—	pA	$\overline{CS}$ = V_{DD}
$\overline{CS}$ Input High, GND Current	I_{SS}	—	-20	—	pA	$\overline{CS}$ = V_{DD}
Amplifier Output Leakage, $\overline{CS}$ High	I_{OLEAK}	—	20	—	pA	$\overline{CS}$ = V_{DD}
Dynamic Specifications						
$\overline{CS}$ Low to Amplifier Output Turn-on Time	t_{ON}	—	2	50	ms	G = +1V/V, $\overline{CS}$ = 0.3V to V_{OUT} = 0.9V_{DD}/2
$\overline{CS}$ High to Amplifier Output High-Z	t_{OFF}	—	10	—	µs	G = +1V/V, $\overline{CS}$ = V_{DD}–0.3V to V_{OUT} = 0.1V_{DD}/2
Hysteresis	V_{HYST}	—	0.6	—	V	V_{DD} = 5.0V

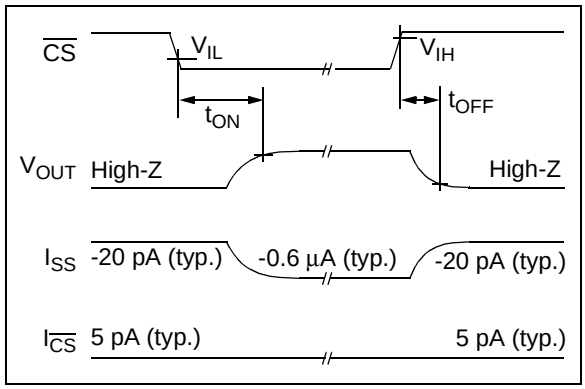


FIGURE 1-1: *Chip Select ($\overline{CS}$) Timing Diagram (MCP6143 only).*

TEMPERATURE CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +1.4V to +5.5V, V_{SS} = GND.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+85	°C	Industrial Temperature parts
	T_A	-40	—	+125	°C	Extended Temperature parts
Operating Temperature Range	T_A	-40	—	+125	°C	**(Note 1)**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5L-SOT-23	θ_{JA}	—	256	—	°C/W	
Thermal Resistance, 6L-SOT-23	θ_{JA}	—	230	—	°C/W	
Thermal Resistance, 8L-PDIP	θ_{JA}	—	85	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	163	—	°C/W	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	206	—	°C/W	
Thermal Resistance, 14L-PDIP	θ_{JA}	—	70	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	120	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	

Note 1: The MCP6141/2/3/4 family of Industrial Temperature op amps operates over this extended range, but with reduced performance. In any case, the internal Junction Temperature (T_J) should not exceed the Absolute Maximum specification of +150°C.

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = 25°C, V_{DD} = +1.4V to +5.5V, V_{SS} = GND, $V_{CM} = V_{DD}/2$, R_L = 1 MΩ to $V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, and C_L = 60 pF.

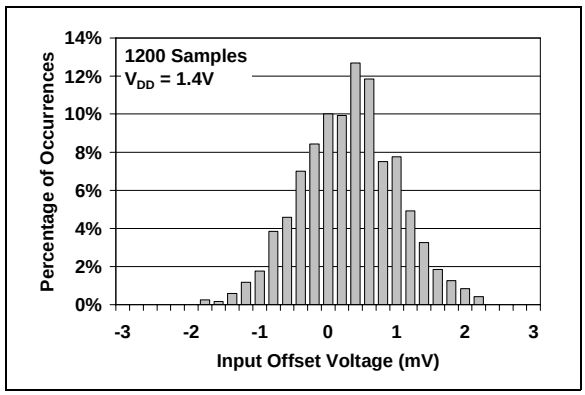


FIGURE 2-1: *Input Offset Voltage at V_{DD} = 1.4V.*

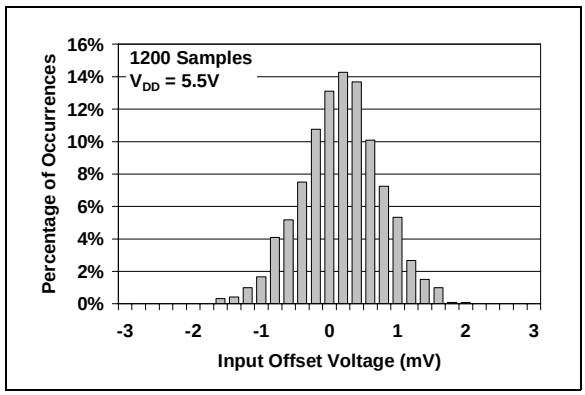


FIGURE 2-4: *Input Offset Voltage at V_{DD} = 5.5V.*

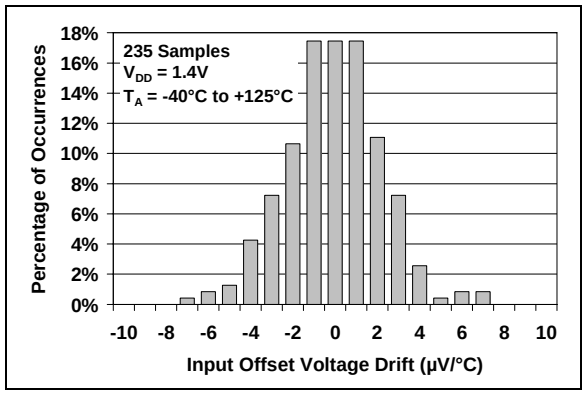


FIGURE 2-2: *Input Offset Voltage Drift at V_{DD} = 1.4V.*

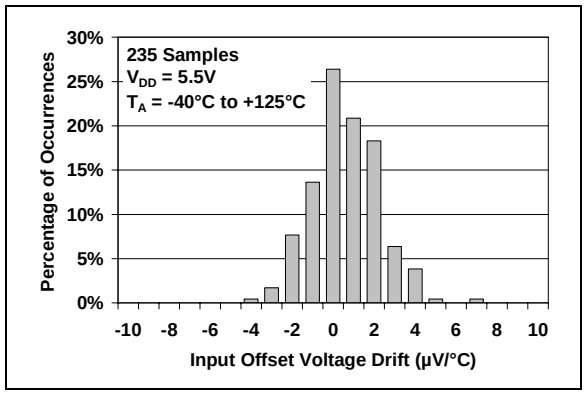


FIGURE 2-5: *Input Offset Voltage Drift at V_{DD} = 5.5V.*

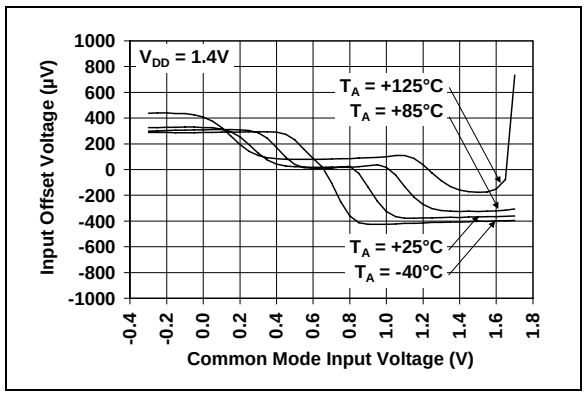


FIGURE 2-3: *Input Offset Voltage vs. Common Mode Input Voltage at V_{DD} = 1.4V.*

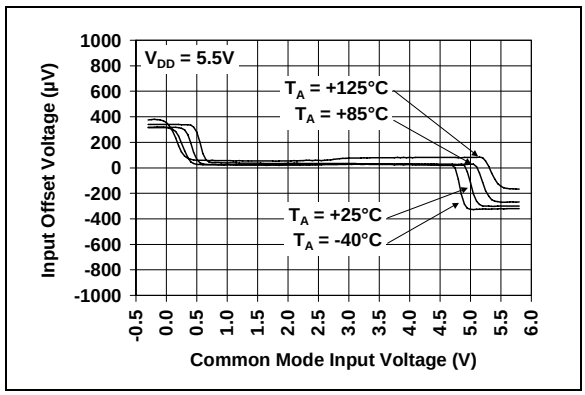


FIGURE 2-6: *Input Offset Voltage vs. Common Mode Input Voltage at V_{DD} = 5.5V.*

Note: Unless otherwise indicated, T_A = 25°C, V_{DD} = +1.4V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, R_L = 1 MΩ to V_{DD}/2, $V_{OUT} \approx V_{DD}/2$, and C_L = 60 pF.

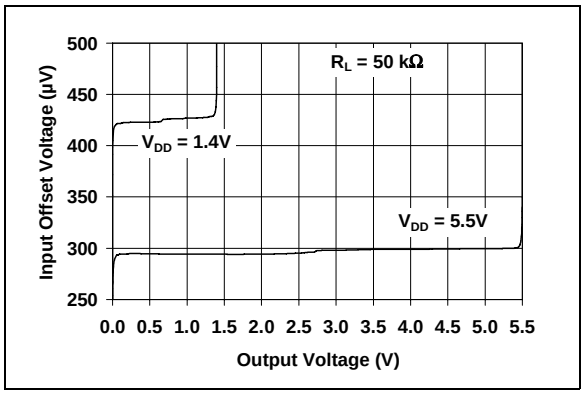


FIGURE 2-7: *Input Offset Voltage vs. Output Voltage.*

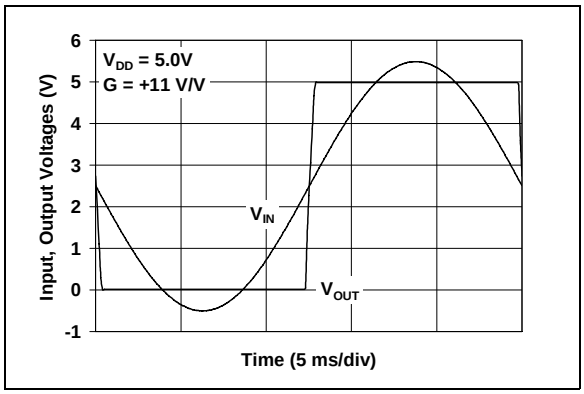


FIGURE 2-10: *The MCP6141/2/3/4 family shows no phase reversal.*

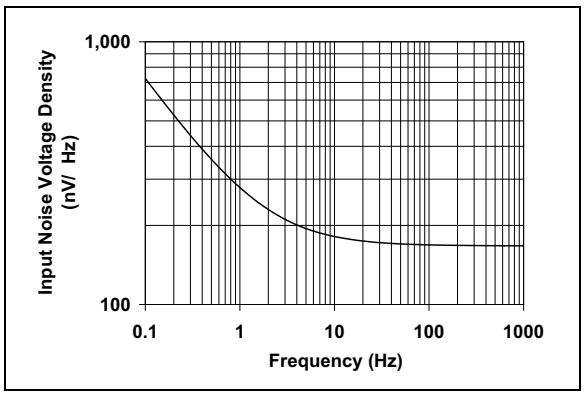


FIGURE 2-8: *Input Noise Voltage Density vs. Frequency.*

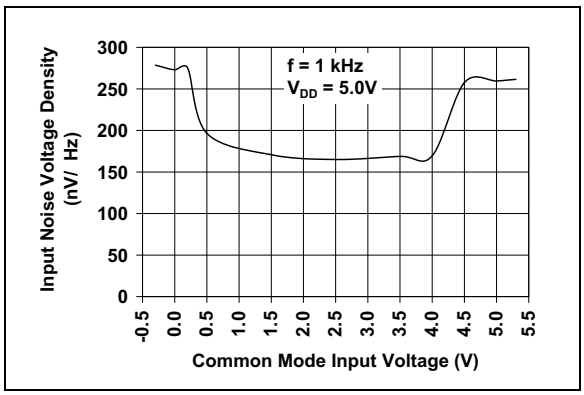


FIGURE 2-11: *Input Noise Voltage Density vs. Common Mode Input Voltage.*

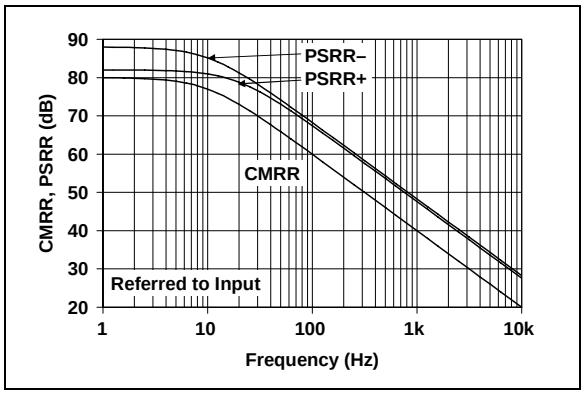


FIGURE 2-9: *CMRR, PSRR vs. Frequency.*

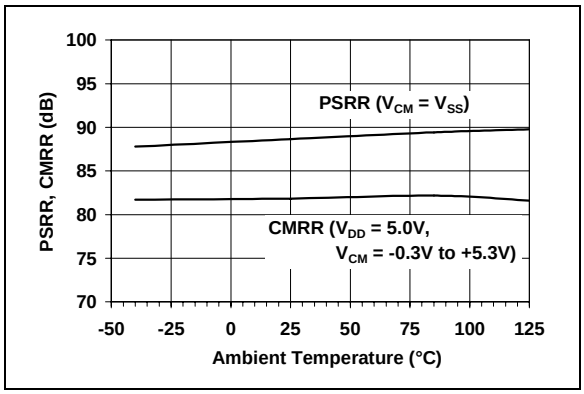


FIGURE 2-12: *CMRR, PSRR vs. Ambient Temperature.*

Note: Unless otherwise indicated, T_A = 25°C, V_{DD} = +1.4V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, R_L = 1 MΩ to V_{DD}/2, V_{OUT} ≈ V_{DD}/2, and C_L = 60 pF.

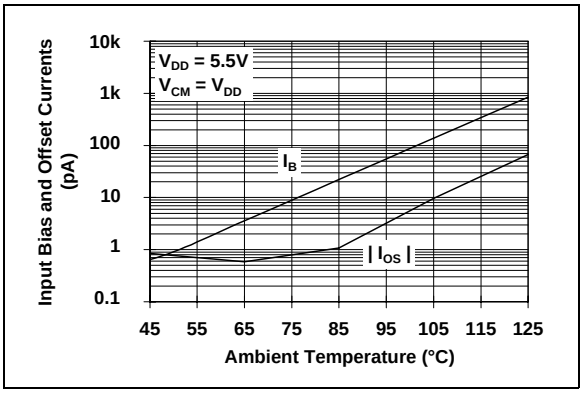


FIGURE 2-13: *Input Bias, Offset Currents vs. Ambient Temperature.*

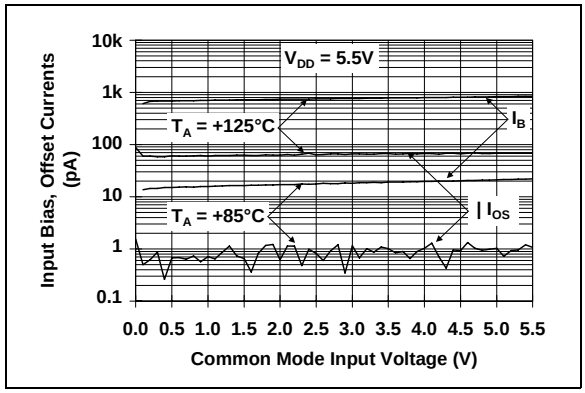


FIGURE 2-16: *Input Bias, Offset Currents vs. Common Mode Input Voltage.*

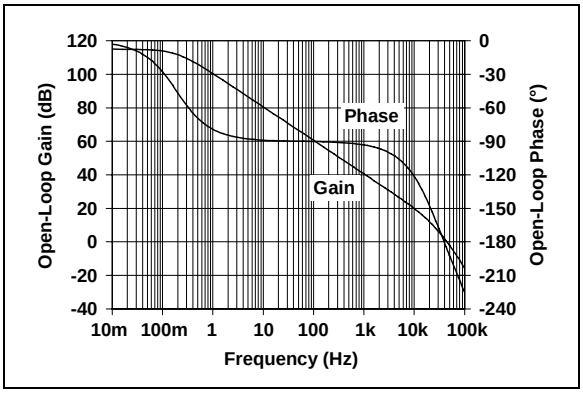


FIGURE 2-14: *Open-Loop Gain, Phase vs. Frequency.*

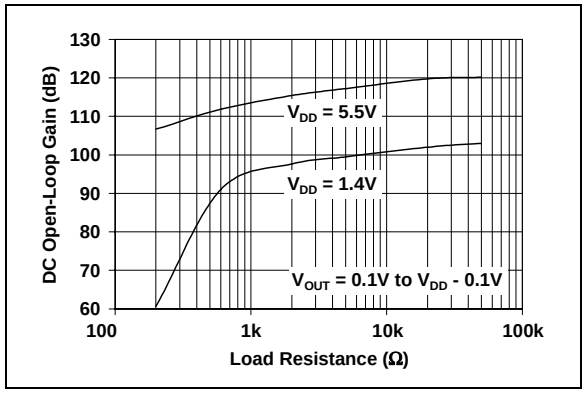


FIGURE 2-17: *DC Open-Loop Gain vs. Load Resistance.*

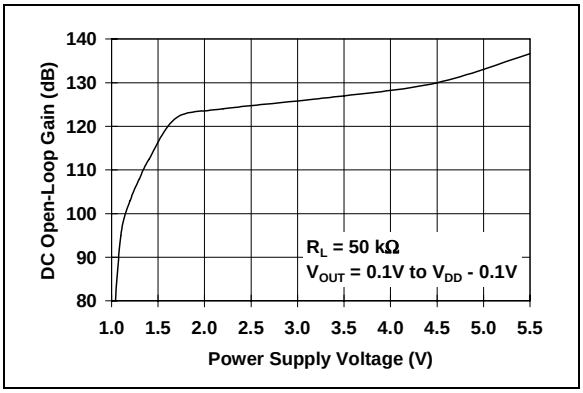


FIGURE 2-15: *DC Open-Loop Gain vs. Power Supply Voltage.*

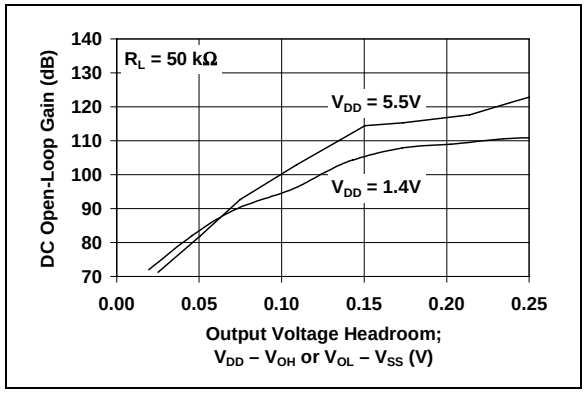


FIGURE 2-18: *DC Open-Loop Gain vs. Output Voltage Headroom.*

Note: Unless otherwise indicated, T_A = 25°C, V_{DD} = +1.4V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, R_L = 1 MΩ to V_{DD}/2, $V_{OUT} \approx V_{DD}/2$, and C_L = 60 pF.

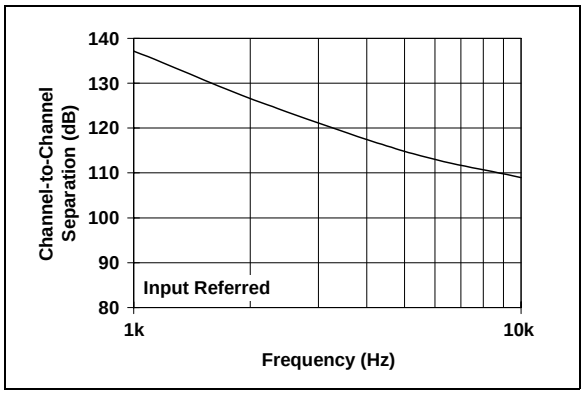


FIGURE 2-19: *Channel-to-Channel Separation vs. Frequency (MCP6142 and MCP6144 only).*

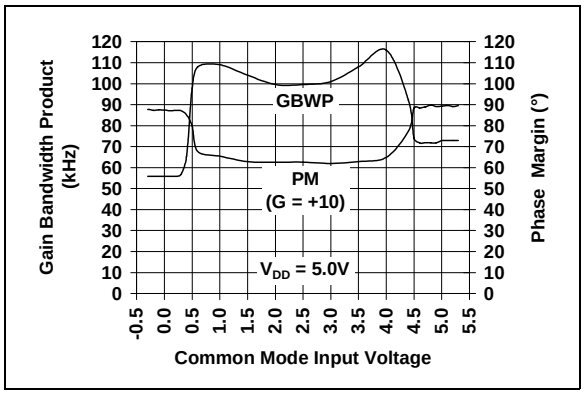


FIGURE 2-22: *Gain Bandwidth Product, Phase Margin vs. Common Mode Input Voltage.*

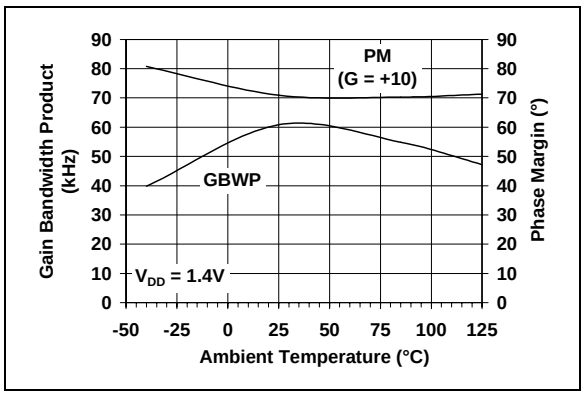


FIGURE 2-20: *Gain Bandwidth Product, Phase Margin vs. Ambient Temperature at V_{DD} = 1.4V.*

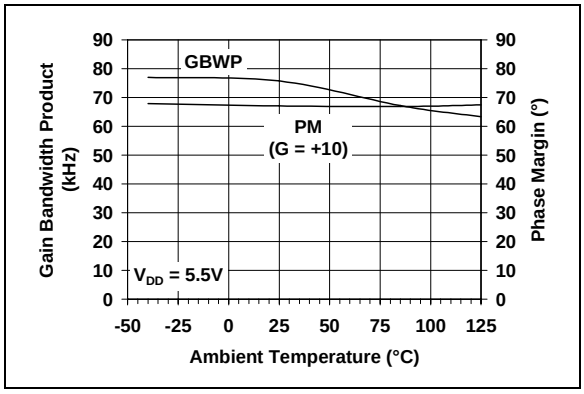


FIGURE 2-23: *Gain Bandwidth Product, Phase Margin vs. Ambient Temperature at V_{DD} = 5.5V.*

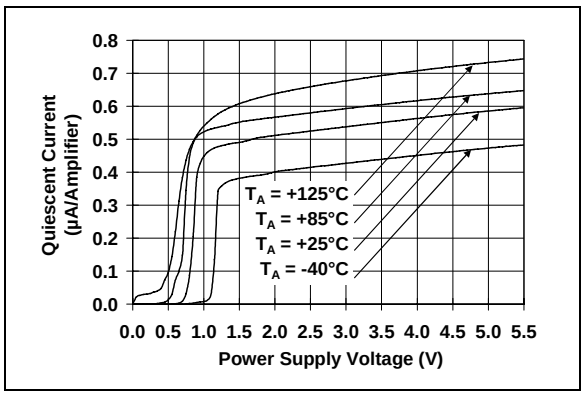


FIGURE 2-21: *Quiescent Current vs. Power Supply Voltage.*

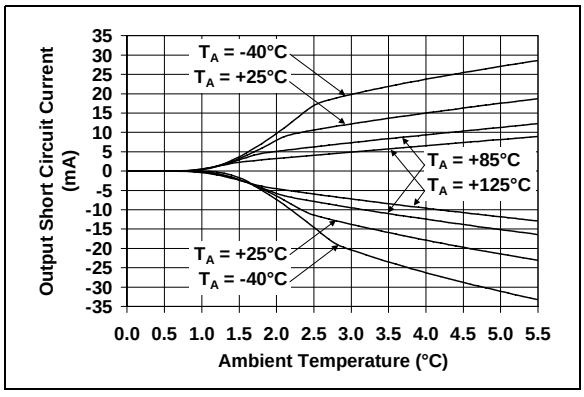


FIGURE 2-24: *Output Short Circuit Current vs. Power Supply Voltage.*

Note: Unless otherwise indicated, T_A = 25°C, V_{DD} = +1.4V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, R_L = 1 MΩ to V_{DD}/2, $V_{OUT} \approx V_{DD}/2$, and C_L = 60 pF.

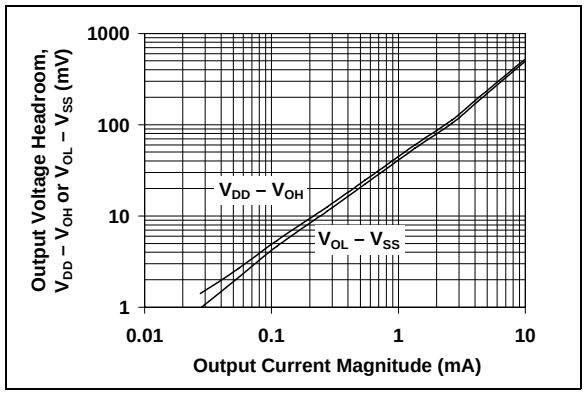


FIGURE 2-25: *Output Voltage Headroom vs. Output Current Magnitude.*

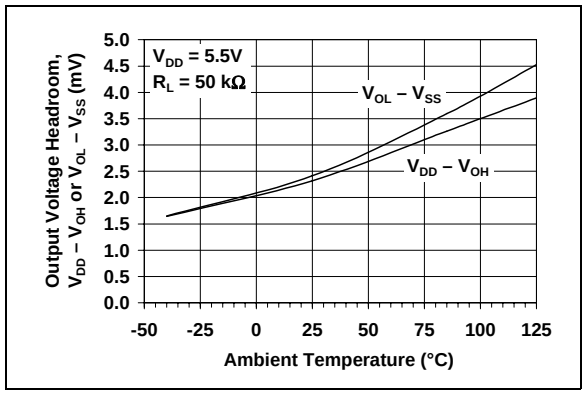


FIGURE 2-28: *Output Voltage Headroom vs. Ambient Temperature.*

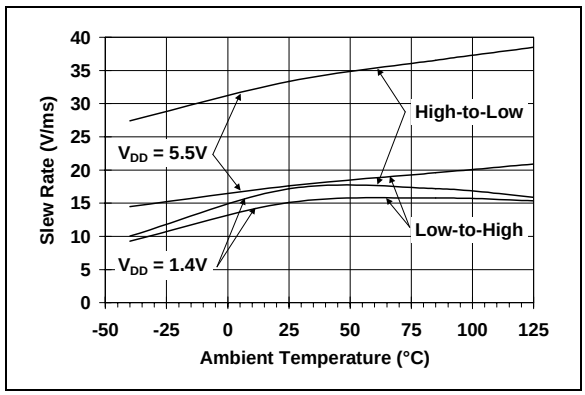


FIGURE 2-26: *Slew Rate vs. Ambient Temperature.*

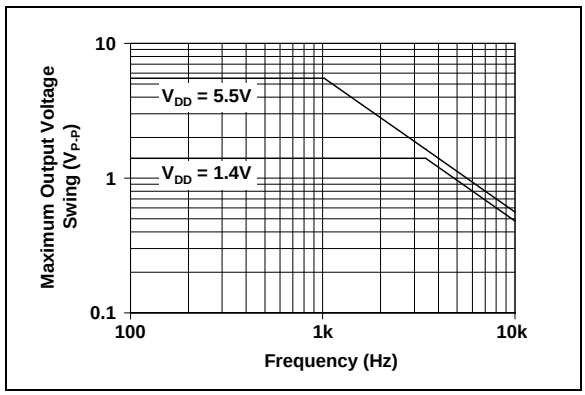


FIGURE 2-29: *Maximum Output Voltage Swing vs. Frequency.*

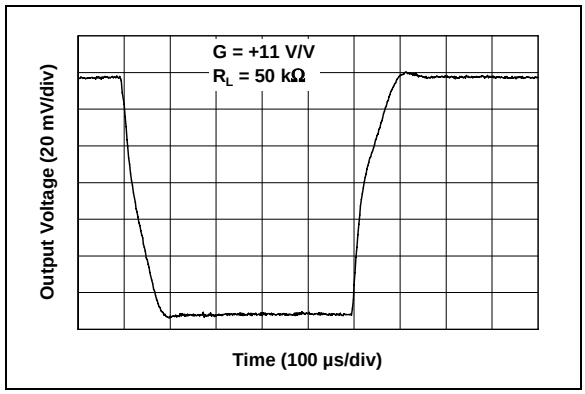


FIGURE 2-27: *Small Signal Non-inverting Pulse Response.*

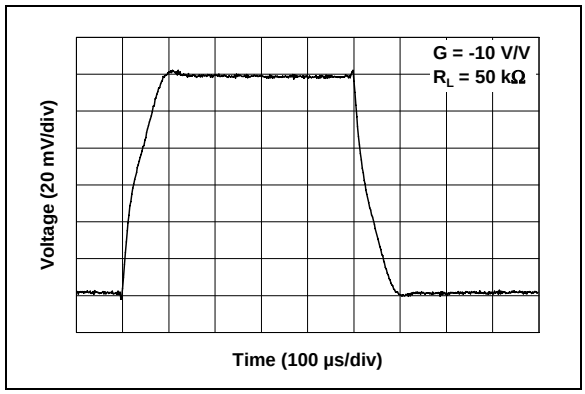


FIGURE 2-30: *Small Signal Inverting Pulse Response.*

Note: Unless otherwise indicated, T_A = 25°C, V_{DD} = +1.4V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, R_L = 1 MΩ to V_{DD}/2, $V_{OUT} \approx V_{DD}/2$, and C_L = 60 pF.

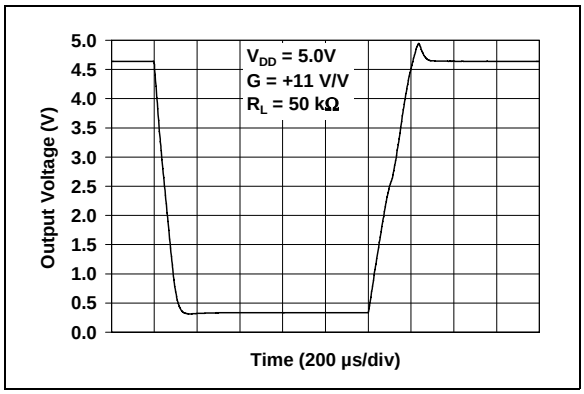


FIGURE 2-31: *Large Signal Non-inverting Pulse Response.*

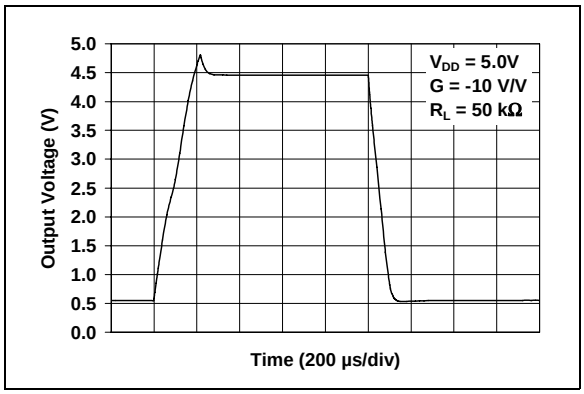


FIGURE 2-33: *Large Signal Inverting Pulse Response.*

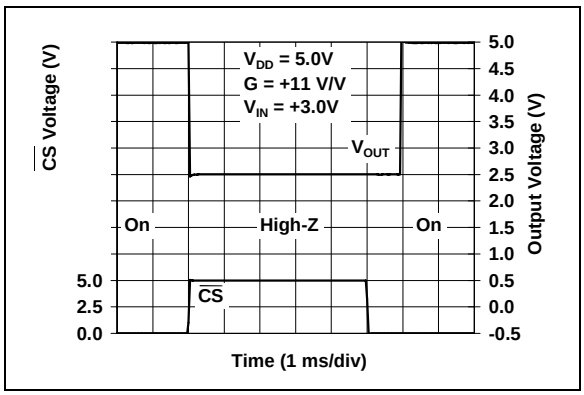


FIGURE 2-32: *Chip Select ($\overline{CS}$) to Amplifier Output Response Time (MCP6143 only).*

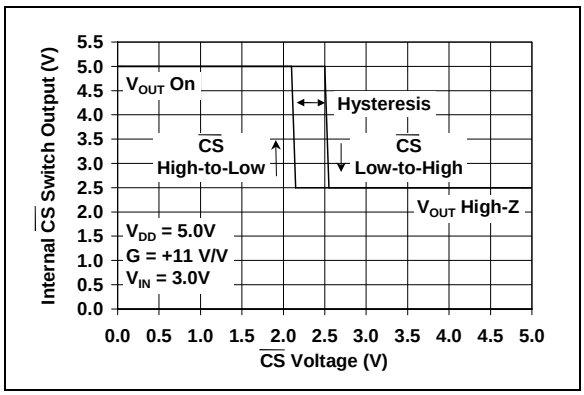


FIGURE 2-34: *Internal Chip Select ($\overline{CS}$) Hysteresis (MCP6143 only).*

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP6141 (PDIP, SOIC, MSOP)	**MCP6141** (SOT-23-5)	**MCP6142**	**MCP6143** (PDIP, SOIC, MSOP)	**MCP6143** (SOT-23-6)	**MCP6144**	**Symbol**	**Description**
6	1	1	6	1	1	V_{OUT}, V_{OUTA}	Analog Output (op amp A)
2	4	2	2	4	2	$V_{IN}-$, $V_{INA}-$	Inverting Input (op amp A)
3	3	3	3	3	3	$V_{IN}+$, $V_{INA}+$	Non-inverting Input (op amp A)
7	5	8	7	6	4	V_{DD}	Positive Power Supply
—	—	5	—	—	5	$V_{INB}+$	Non-inverting Input (op amp B)
—	—	6	—	—	6	$V_{INB}-$	Inverting Input (op amp B)
—	—	7	—	—	7	V_{OUTB}	Analog Output (op amp B)
—	—	—	—	—	8	V_{OUTC}	Analog Output (op amp C)
—	—	—	—	—	9	$V_{INC}-$	Inverting Input (op amp C)
—	—	—	—	—	10	$V_{INC}+$	Non-inverting Input (op amp C)
4	2	4	4	2	11	V_{SS}	Negative Power Supply
—	—	—	—	—	12	$V_{IND}+$	Non-inverting Input (op amp D)
—	—	—	—	—	13	$V_{IND}-$	Inverting Input (op amp D)
—	—	—	—	—	14	V_{OUTD}	Analog Output (op amp D)
—	—	—	8	5	—	$\overline{CS}$	Chip Select
1, 5, 8	—	—	1, 5	—	—	NC	No Internal Connection

3.1 Analog Outputs

The output pins are low-impedance voltage sources.

3.2 Analog Inputs

The non-inverting and inverting inputs are high-impedance CMOS inputs with low bias currents.

3.3 $\overline{CS}$ Digital Input

This is a CMOS, Schmitt-triggered input that places the part into a low-power mode of operation.

3.4 Power Supply (V_{SS} and V_{DD})

The positive power supply pin (V_{DD}) is 1.4V to 5.5V higher than the negative power supply pin (V_{SS}). For normal operation, the other pins are at voltages between V_{SS} and V_{DD}.

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} will need a local bypass capacitor (typically 0.01 µF to 0.1 µF) within 2 mm of the V_{DD} pin. These can share a bulk capacitor with nearby analog parts (within 100 mm), but it is not required.

4.0 APPLICATIONS INFORMATION

The MCP6141/2/3/4 family of op amps is manufactured using Microchip's state-of-the-art CMOS process These op amps are stable for gains of 10 V/V and higher. They are suitable for a wide range of general purpose, low-power applications.

See Microchip's related MCP6041/2/3/4 family of op amps for applications needing unity gain stability.

4.1 Rail-to-Rail Inputs

The MCP6141/2/3/4 op amps are designed to prevent phase reversal when the input pins exceed the supply voltages. Figure 2-10 shows the input voltage exceeding the supply voltage without any phase reversal.

The input stage of the MCP6141/2/3/4 op amps uses two differential CMOS input stages in parallel. One operates at low Common mode input voltage (V_{CM}), while the other operates at high V_{CM}. With this topology, the device operates with V_{CM} tp to 0.3V above V_{DD} and 0.3V below V_{SS}. The input offset voltage (V_{OS}) is measured at $V_{CM} = V_{SS} – 0.3V$ and $V_{DD} + 0.3V$ to ensure proper operation.

Input voltages that exceed the Absolute Maximum Voltage Range ($V_{SS} – 0.3V$ to $V_{DD} + 0.3V$) can cause excessive current to flow into or out of the input pins. Current beyond ±2 mA can cause reliability problems. Applications that exceed this rating must be externally limited with a resistor, as shown in Figure 4-1.

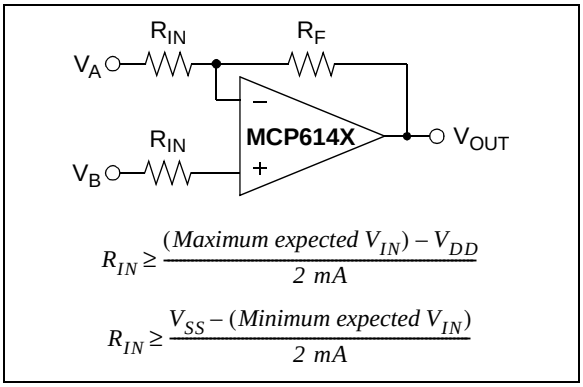


FIGURE 4-1: *Input Current-Limiting Resistor (R_{IN}).*

4.2 Rail-to-Rail Output

There are two specifications that describe the output swing capability of the MCP6141/2/3/4 family of op amps. The first specification (Maximum Output Voltage Swing) defines the absolute maximum swing that can be achieved under the specified load condition. Thus, the output voltage swings to within 10 mV of either supply rail with a 50 kΩ load to $V_{DD}/2$. Figure 2-10 shows how the output voltage is limited when the input goes beyond the linear region of operation.

The second specification that describes the output swing capability of these amplifiers is the Linear Output Voltage Range. This specification defines the maximum output swing that can be achieved while the amplifier still operates in its linear region. To verify linear operation in this range, the large signal DC Open-Loop Gain (A_{OL}) is measured at points inside the supply rails. The measurement must meet the specified A_{OL} condition in the specification table.

4.3 Output Loads and Battery Life

The MCP6141/2/3/4 op amp family has outstanding quiescent current, which supports battery-powered applications. There is minimal quiescent current glitching when Chip Select ($\overline{CS}$) is raised or lowered. This prevents excessive current draw, and reduced battery life, when the part is turned off or on.

Heavy resistive loads at the output can cause excessive battery drain. Driving a DC voltage of 2.5V across a 100 kΩ load resistor will cause the supply current to increase by 25 µA, depleting the battery 43 times as fast as I_Q (0.6 µA, typ.) alone.

High frequency signals (fast edge rate) across capacitive loads will also significantly increase supply current. For instance, a 0.1 µF capacitor at the output presents an AC impedance of 15.9 kΩ ($1/2\pi fC$) to a 100 Hz sinewave. It can be shown that the average power drawn from the battery by a 5.0 V_{p-p} sinewave (1.77 V_{rms}), under these conditions, is

EQUATION 4-1:

$$\begin{aligned} P_{Supply} &= (V_{DD} - V_{SS})\,(I_Q + V_{L(p-p)}\,f\,C_L) \\ &= (5V)(0.6\ \mu A + 5.0V_{p-p} \cdot 100Hz \cdot 0.1\mu F) \\ &= 3.0\ \mu W + 50\ \mu W \end{aligned}$$

This will drain the battery 18 times as fast as I_Q alone.

4.4 Stability

4.4.1 NOISE GAIN

The MCP6141/2/3/4 op amp family is designed to give high bandwidth and slew rate for circuits with high noise gain (G_N) or signal gain. Low gain applications should be realized using the MCP6041/2/3/4 op amp family; this simplifies design and implementation issues.

Noise gain is defined to be the gain from a voltage source at the non-inverting input to the output when all other voltage sources are zeroed (shorted out). Noise gain is independent of signal gain and depends only on components in the feedback loop. The amplifier circuits in Figure 4-2 and Figure 4-3 have their noise gain calculated as follows:

EQUATION 4-2:

$$G_N = 1 + \frac{R_F}{R_G} \geq 10\ V/V$$

In order for the amplifiers to be stable, the noise gain should meet the specified minimum noise gain. Note that a noise gain of G_N = +10 V/V corresponds to a non-inverting signal gain of G = +10 V/V, or to an inverting signal gain of G = -9 V/V.

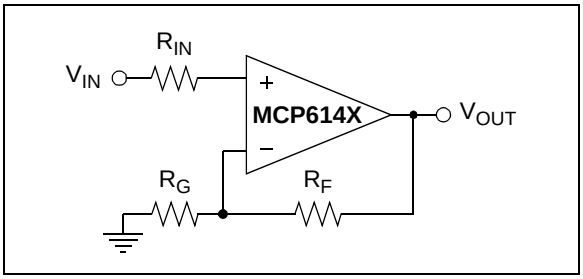


FIGURE 4-2: *Noise Gain for Non-inverting Gain Configuration.*

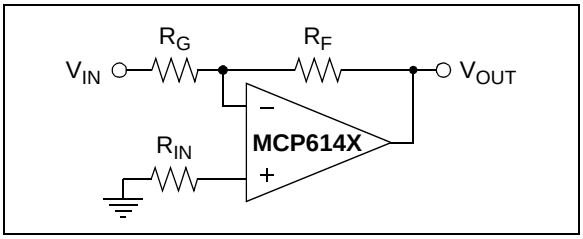


FIGURE 4-3: *Noise Gain for Inverting Gain Configuration.*

Figure 4-4 shows a unity gain buffer and Miller integrator that are unstable when used with the MCP6141/2/3/4 family. Note that the capacitor makes the integrator circuit reach unity gain at high frequencies, which makes these op amps unstable.

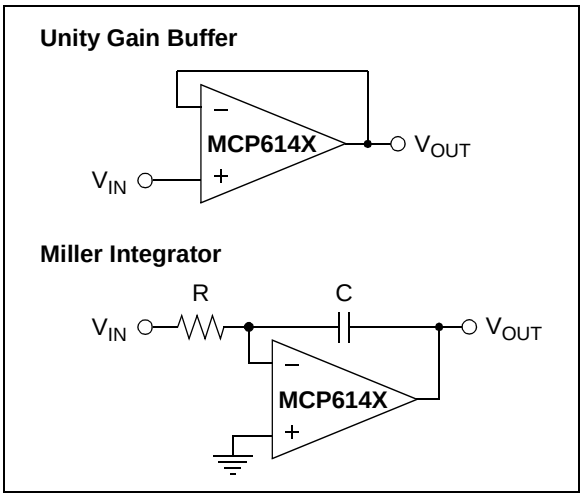


FIGURE 4-4: *Typical Unstable Circuits for the MCP6141/2/3/4 Family.*

4.4.2 CAPACITIVE LOADS

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. A unity gain buffer (G = +1) is the most sensitive to capacitive loads, though all gains show the same general behavior.

When driving large capacitive loads with these op amps (e.g., > 60 pF when G = +10), a small series resistor at the output (R_{ISO} in Figure 4-5) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitive load.

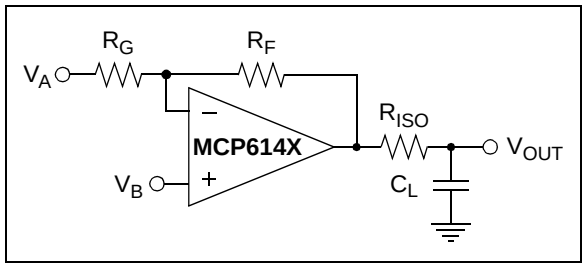


FIGURE 4-5: *Output Resistor, R_{ISO} stabilizes large capacitive loads.*

Figure 4-6 gives recommended R_{ISO} values for different capacitive loads and gains. The x-axis is the normalized load capacitance (C_L/G_N), where G_N is the circuit's noise gain. For non-inverting gains, G_N and the Signal Gain are equal. For inverting gains, G_N is 1+|Signal Gain| (e.g., -9 V/V gives G_N = +10 V/V).

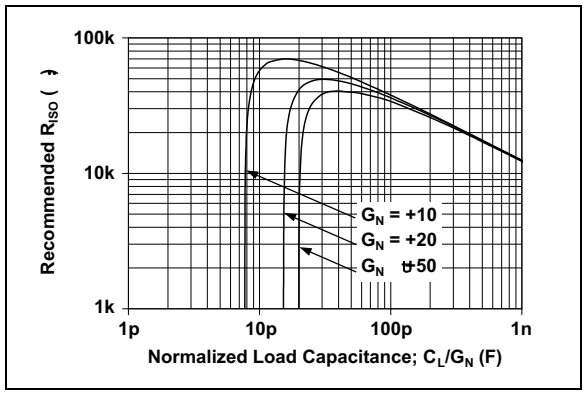


FIGURE 4-6: *Recommended R_{ISO} Values for Capacitive Loads.*

After selecting R_{ISO} for your circuit, double check the resulting frequency response peaking and step response overshoot. Modify R_{ISO}'s value until the response is reasonable. Bench evaluation and simulations with the MCP6141/2/3/4 SPICE macro model are helpful.

4.5 MCP6143 Chip Select ($\overline{CS}$)

The MCP6143 is a single op amp with Chip Select ($\overline{CS}$). When $\overline{CS}$ is pulled high, the supply current drops to 50 nA (typ.) and flows through the $\overline{CS}$ pin to V_{SS}. When this happens, the amplifier output is put into a high impedance state. By pulling $\overline{CS}$ low, the amplifier is enabled. If the $\overline{CS}$ pin is left floating, the amplifier may not operate properly. Figure 1-1 shows the output voltage and supply current response to a $\overline{CS}$ pulse.

4.6 Supply Bypass

With this family of operational amplifiers, the power supply pin (V_{DD} for single supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good high frequency performance. It can use a bulk capacitor (i.e., 1 µF or larger) within 100 mm to provide large, slow currents. This bulk capacitor is not required for most applications and can be shared with other nearby analog parts.

4.7 Unused Op Amps

An unused op amp in a quad package (MCP6144) should be configured as shown in Figure 4-7. These circuits prevent the output from toggling and causing crosstalk. Circuits A and B are set near the minimum noise gain. Circuit A can use any reference voltage between the supplies, provides a buffered DC voltage, and minimizes the supply current draw of the unused op amp. Circuit B may draw a little more supply current for the unused op amp. Circuit C uses the minimum number of components and operates as a comparator; it may draw more current than either Circuit A or B.

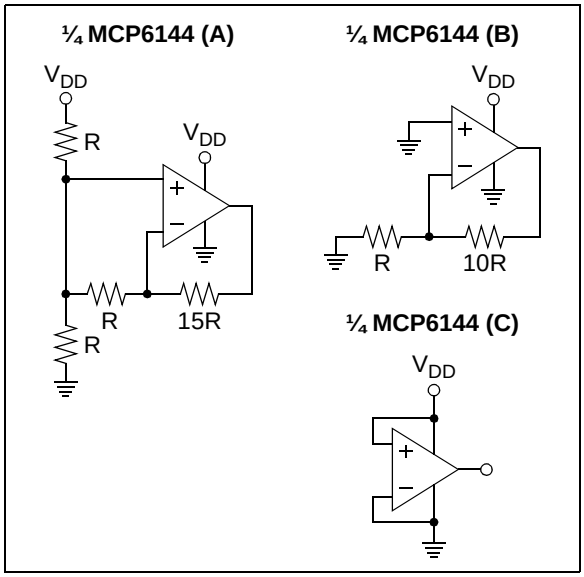


FIGURE 4-7: *Unused Op Amps.*

4.8 PCB Surface Leakage

In applications where low input bias current is critical, printed circuit board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5 pA of current to flow, which is greater than the MCP6141/2/3/4 family's bias current at 25°C (1 pA, typ.).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 4-8.

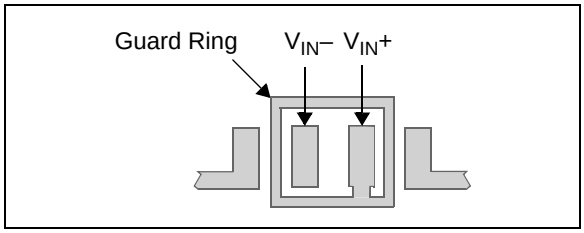


FIGURE 4-8: *Example Guard Ring Layout for Inverting Gain.*

1. Non-inverting Gain and Unity Gain Buffer:
   a) Connect the non-inverting pin (V_{IN}+) to the input with a wire that does not touch the PCB surface.
   b) Connect the guard ring to the inverting input pin (V_{IN}–). This biases the guard ring to the Common mode input voltage.
2. Inverting Gain and Trans-impedance Gain (convert current to voltage, such as photo detectors) amplifiers:
   a) Connect the guard ring to the non-inverting input pin (V_{IN}+). This biases the guard ring to the same reference voltage as the op amp (e.g., $V_{DD}/2$ or ground).
   b) Connect the inverting pin (V_{IN}–) to the input with a wire that does not touch the PCB surface.

4.9 Application Circuits

4.9.1 BATTERY CURRENT SENSING

The MCP6141/2/3/4 op amps' Common Mode Input Range, which goes 0.3V beyond both supply rails, supports their use in high side and low side battery current sensing applications. The very low quiescent current (0.6 µA, typ.) help prolong battery life, and the rail-to-rail output supports detection low currents.

Figure 4-9 shows a high side battery current sensor circuit. The 1 kΩ resistor is sized to minimize power losses. The battery current (I_{DD}) through the 1 kΩ resistor causes its top terminal to be more negative than the bottom terminal. This keeps the Common mode input voltage of the op amp at V_{DD}, which is within its allowed range. When no current is flowing, the output will be at its Maximum Output Voltage Swing (V_{OH}), which is virtually at V_{DD}.

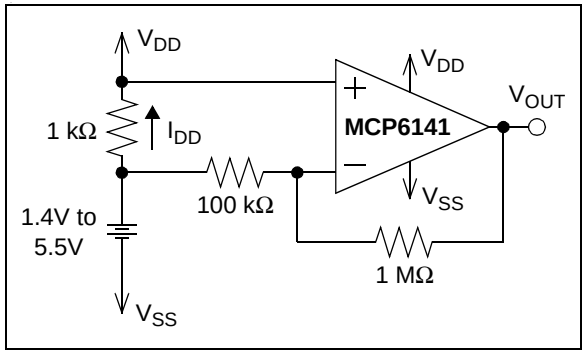


FIGURE 4-9: *High Side Battery Current Sensor.*

4.9.2 INVERTING SUMMING AMPLIFIER

The MCP6141/2/3/4 op amp is well suited for the inverting summing amplifier shown in Figure 4-10 when the resistors at the input (R_1, R_2, and R_3) make the noise gain at least 10 V/V. The output voltage (V_{OUT}) is a weighted sum of the inputs (V_1, V_2, and V_3), and is shifted by the V_{REF} input. The necessary calculations follow in Equation 4-3.

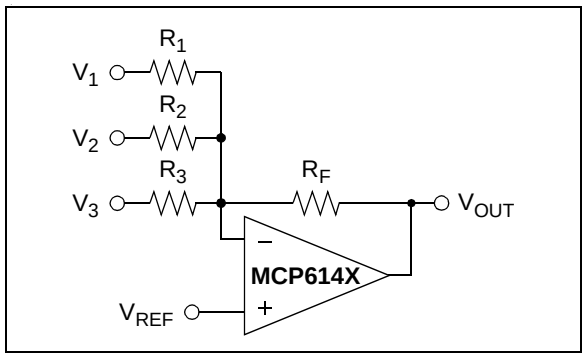


FIGURE 4-10: *Summing Amplifier.*

EQUATION 4-3:

Noise Gain:

$$G_N = 1 + R_F\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right) \geq 10\ V/V$$

Signal Gains:

$$G_1 = -R_F/R_1$$
$$G_2 = -R_F/R_2$$
$$G_3 = -R_F/R_3$$

Output Signal:

$$V_{OUT} = V_1G_1 + V_2G_2 + V_3G_3 + V_{REF}G_N$$

5.0 DESIGN TOOLS

Microchip provides the basic design tools needed for the MCP6141/2/3/4 family of op amps.

5.1 SPICE Macro Model

The latest SPICE macro model for the MCP6141/2/3/4 op amps is available on our web site at www.microchip.com. This model is intended to be an initial design tool that works well in the op amp's linear region of operation at room temperature. See the model file for information on its capabilities.

Bench testing is a very important part of any design and cannot be replaced with simulations. Also, simulation results using this macro model need to be validated by comparing them to the data sheet specifications and characteristic curves.

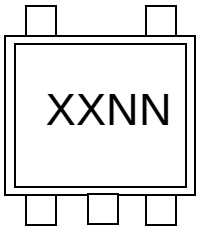
5.2 FilterLab® Software

The FilterLab software is an innovative tool that simplifies analog active filter (using op amps) design. It is available free of charge from our web site at www.microchip.com. The FilterLab software tool provides full schematic diagrams of the filter circuit with component values. It also outputs the filter circuit in SPICE format, which can be used with the macro model to simulate actual filter performance.

6.0 PACKAGING INFORMATION

6.1 Package Marking Information

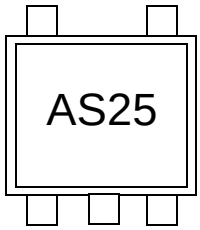
5-Lead SOT-23 (**MCP6141**)



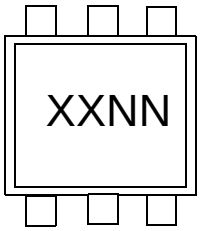
Device	E-Temp Code
MCP6141	ASNN

Note: Applies to 5-Lead SOT-23

Example:



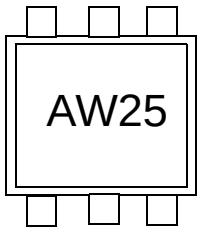
6-Lead SOT-23 (**MCP6143)**



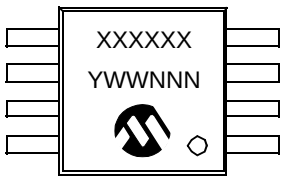
Device	E-Temp Code
MCP6143	AWNN

Note: Applies to 6-Lead SOT-23

Example:



8-Lead MSOP



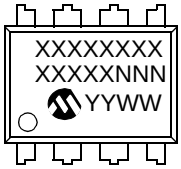
Example:

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

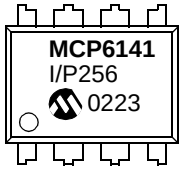
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

Package Marking Information (Continued)

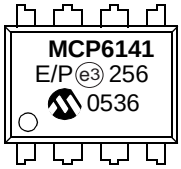
8-Lead PDIP (300 mil)



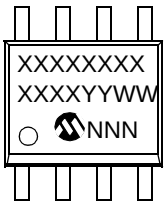
Example:



OR



8-Lead SOIC (150 mil)



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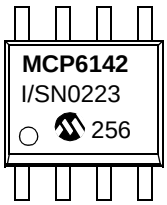
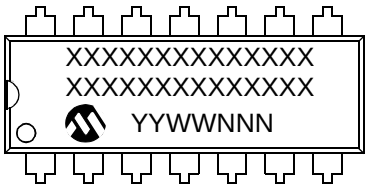


OR

14-Lead PDIP (300 mil) (**MCP6144**)



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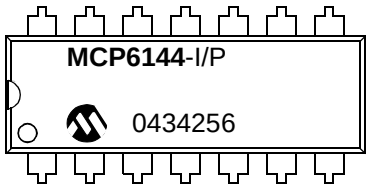
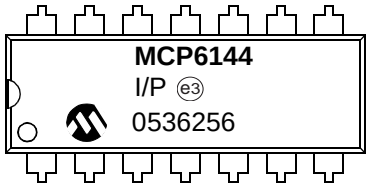
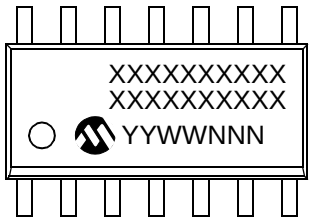


OR

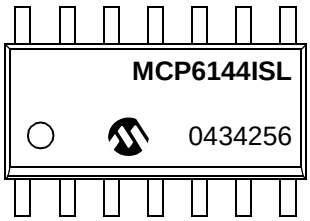


Package Marking Information (Continued)

14-Lead SOIC (150 mil) (**MCP6144**)



Example:



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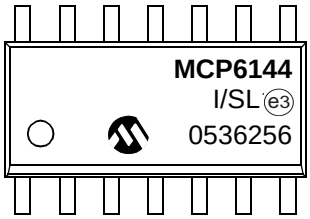
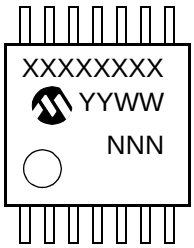
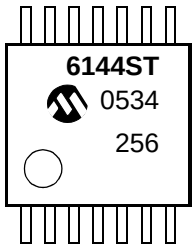


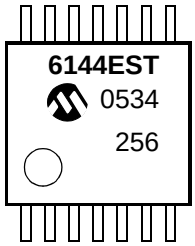
14-Lead TSSOP (**MCP6144**)



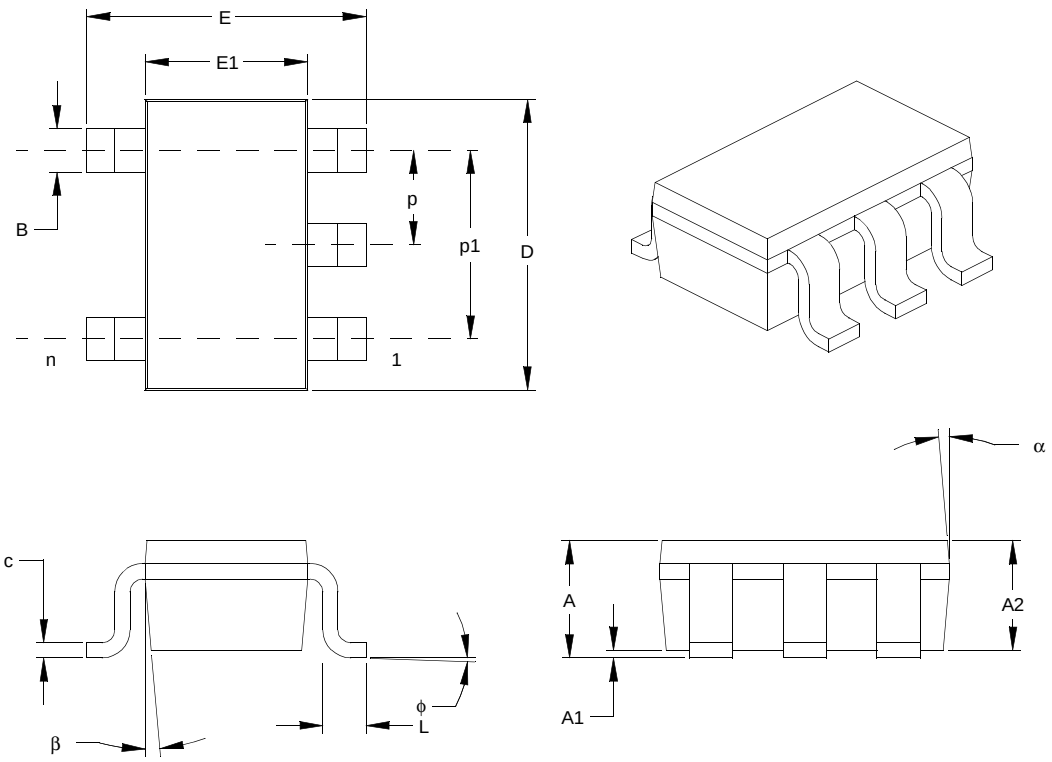
Example:



OR



5-Lead Plastic Small Outline Transistor (OT) (SOT-23)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		5			5	
Pitch	p		.038			0.95	
Outside lead pitch (basic)	p1		.075			1.90	
Overall Height	A	.035	.046	.057	0.90	1.18	1.45
Molded Package Thickness	A2	.035	.043	.051	0.90	1.10	1.30
Standoff	A1	.000	.003	.006	0.00	0.08	0.15
Overall Width	E	.102	.110	.118	2.60	2.80	3.00
Molded Package Width	E1	.059	.064	.069	1.50	1.63	1.75
Overall Length	D	.110	.116	.122	2.80	2.95	3.10
Foot Length	L	.014	.018	.022	0.35	0.45	0.55
Foot Angle	f	0	5	10	0	5	10
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.014	.017	.020	0.35	0.43	0.50
Mold Draft Angle Top	a	0	5	10	0	5	10
Mold Draft Angle Bottom	b	0	5	10	0	5	10

***** Controlling Parameter

Notes:

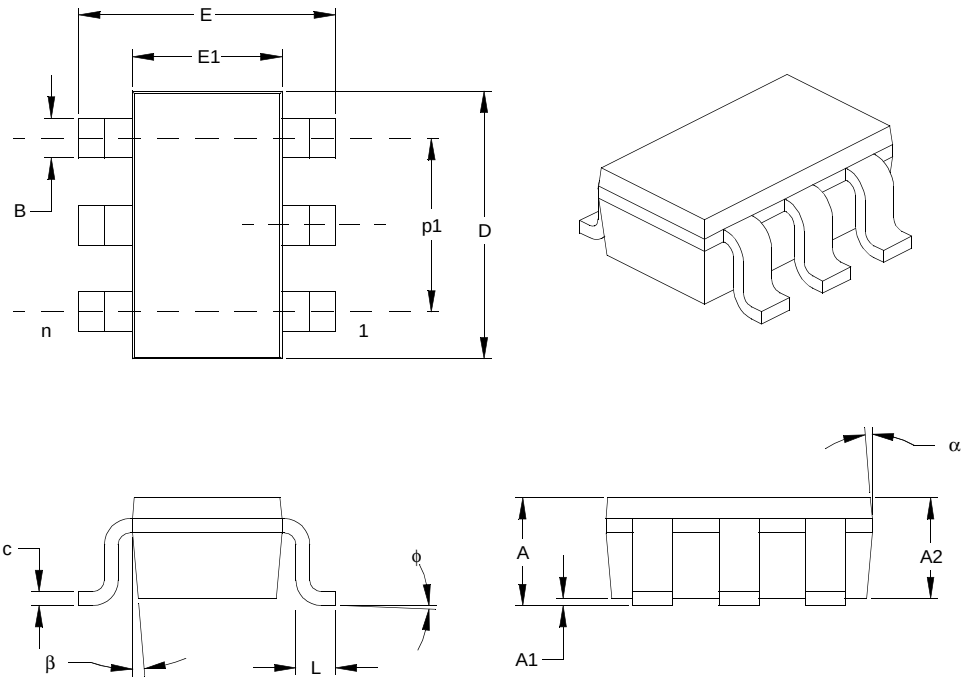
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.

EIAJ Equivalent: SC-74A

Drawing No. C04-091

Revised 09-12-05

6-Lead Plastic Small Outline Transistor (CH) (SOT-23)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		6			6	
Pitch	p		.038 BSC			0.95 BSC	
Outside lead pitch	p1		.075 BSC			1.90 BSC	
Overall Height	A	.035	.046	.057	0.90	1.18	1.45
Molded Package Thickness	A2	.035	.043	.051	0.90	1.10	1.30
Standoff	A1	.000	.003	.006	0.00	0.08	0.15
Overall Width	E	.102	.110	.118	2.60	2.80	3.00
Molded Package Width	E1	.059	.064	.069	1.50	1.63	1.75
Overall Length	D	.110	.116	.122	2.80	2.95	3.10
Foot Length	L	.014	.018	.022	0.35	0.45	0.55
Foot Angle	ϕ	0	5	10	0	5	10
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.014	.017	.020	0.35	0.43	0.50
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

***** Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

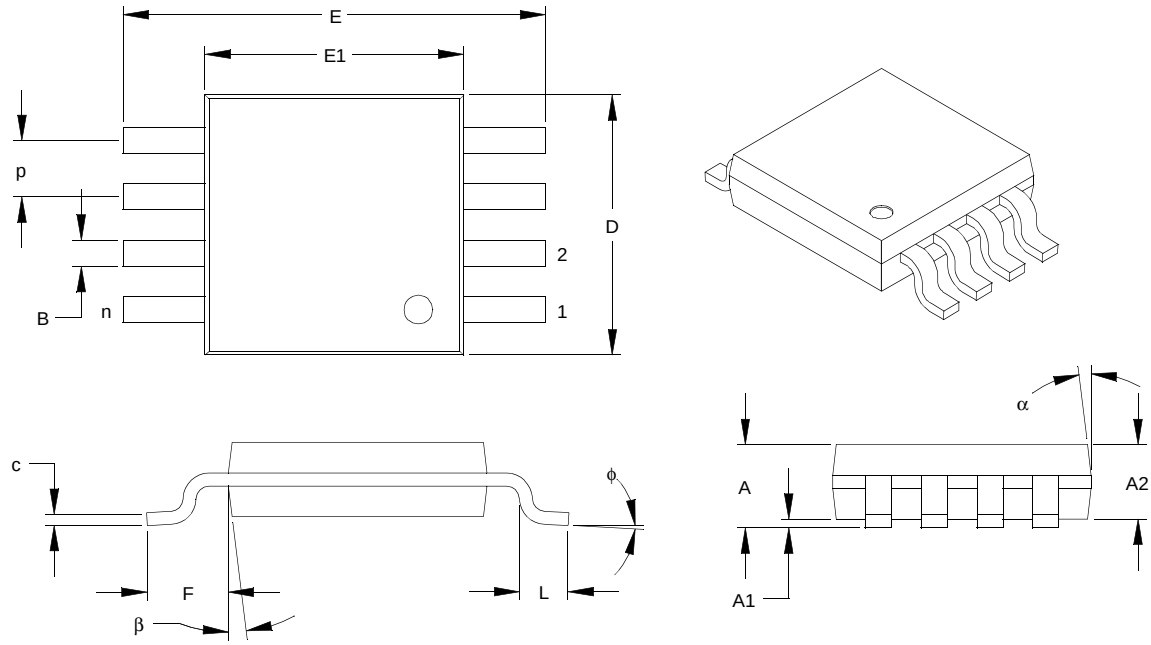
See ASME Y14.5M

JEITA (formerly EIAJ) equivalent: SC-74A

Drawing No. C04-120

Revised 09-12-05

8-Lead Plastic Micro Small Outline Package (MS) (MSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.026 BSC			0.65 BSC	
Overall Height	A	-	-	.043	-	-	1.10
Molded Package Thickness	A2	.030	.033	.037	0.75	0.85	0.95
Standoff	A1	.000	-	.006	0.00	-	0.15
Overall Width	E		.193 BSC			4.90 BSC	
Molded Package Width	E1		.118 BSC			3.00 BSC	
Overall Length	D		.118 BSC			3.00 BSC	
Foot Length	L	.016	.024	.031	0.40	0.60	0.80
Footprint (Reference)	F		.037 REF			0.95 REF	
Foot Angle	ϕ	0°	-	8°	0°	-	8°
Lead Thickness	c	.003	.006	.009	0.08	-	0.23
Lead Width	B	.009	.012	.016	0.22	-	0.40
Mold Draft Angle Top	α	5°	-	15°	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°	5°	-	15°

***** Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

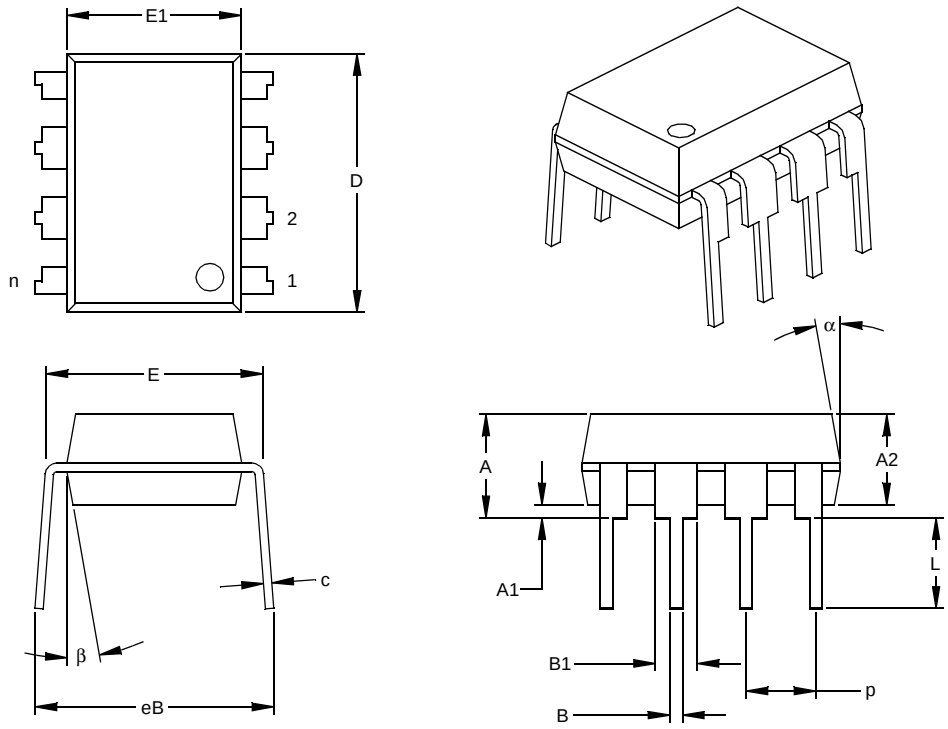
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
See ASME Y14.5M

REF: Reference Dimension, usually without tolerance, for information purposes only.
See ASME Y14.5M

JEDEC Equivalent: MO-187 Revised 07-21-05

Drawing No. C04-111

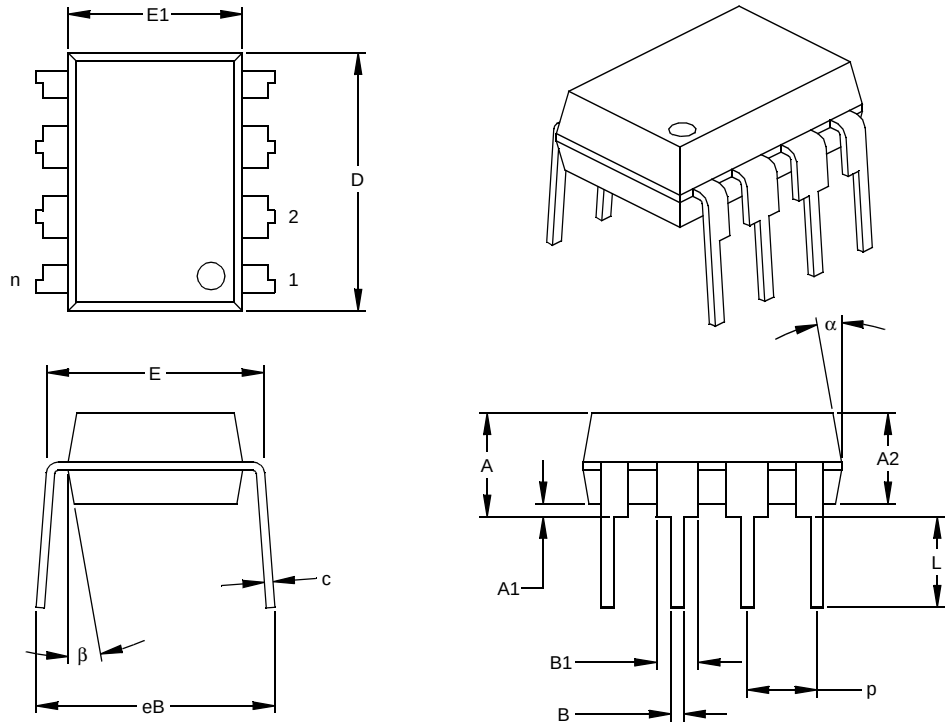
8-Lead Plastic Dual In-line (P) – 300 mil Body (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

***** Controlling Parameter
§ Significant Characteristic
Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

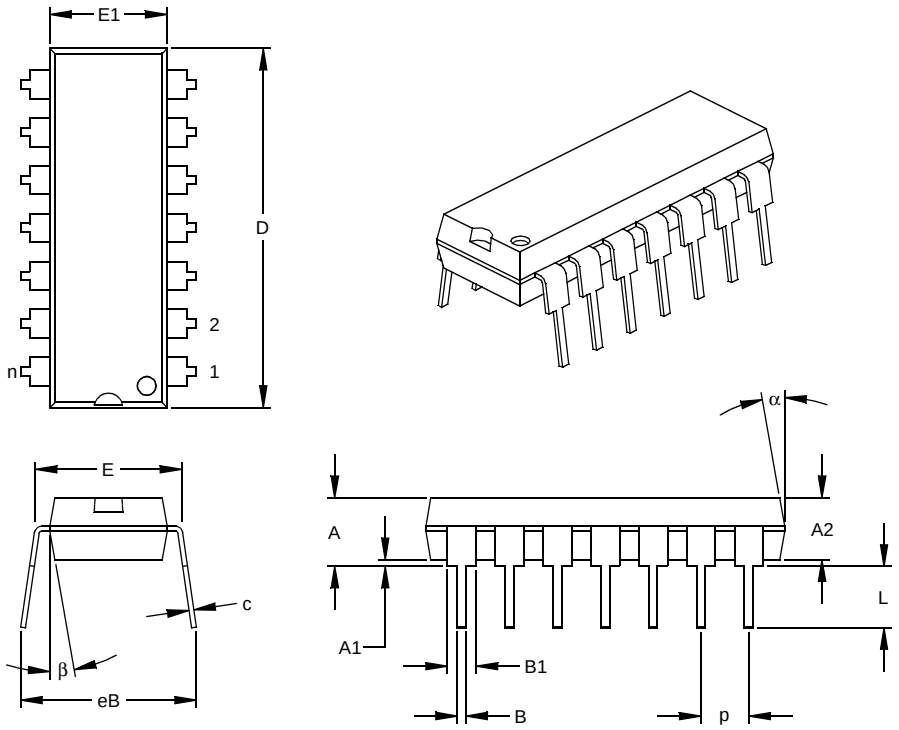
8-Lead Plastic Micro Small Outline Package (MS) (MSOP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

***** Controlling Parameter
§ Significant Characteristic
Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

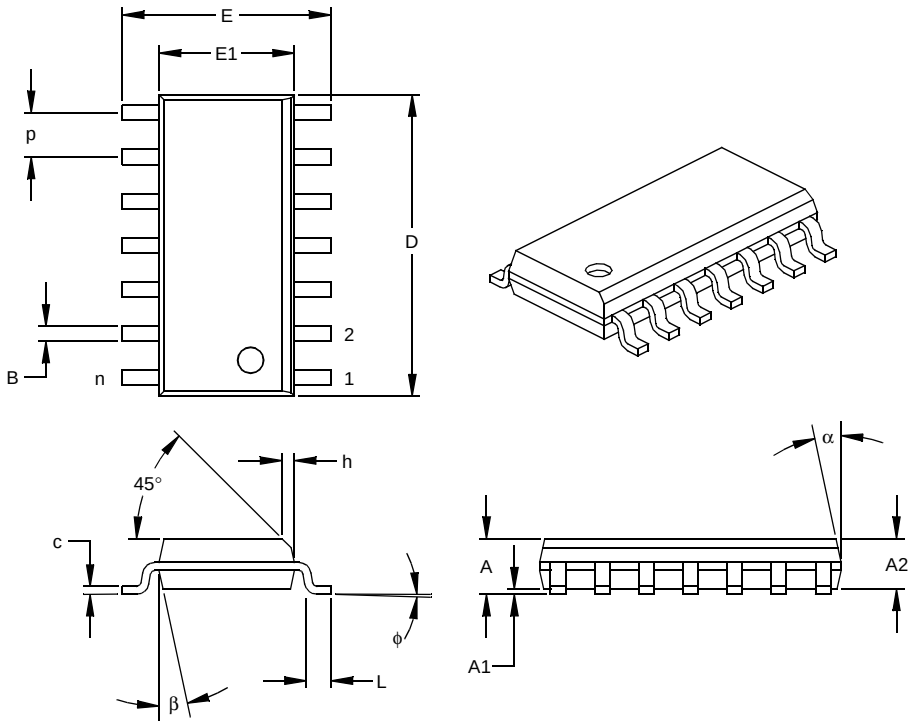
14-Lead Plastic Dual In-line (P) – 300 mil Body (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.740	.750	.760	18.80	19.05	19.30
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

***** Controlling Parameter
§ Significant Characteristic
Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-005

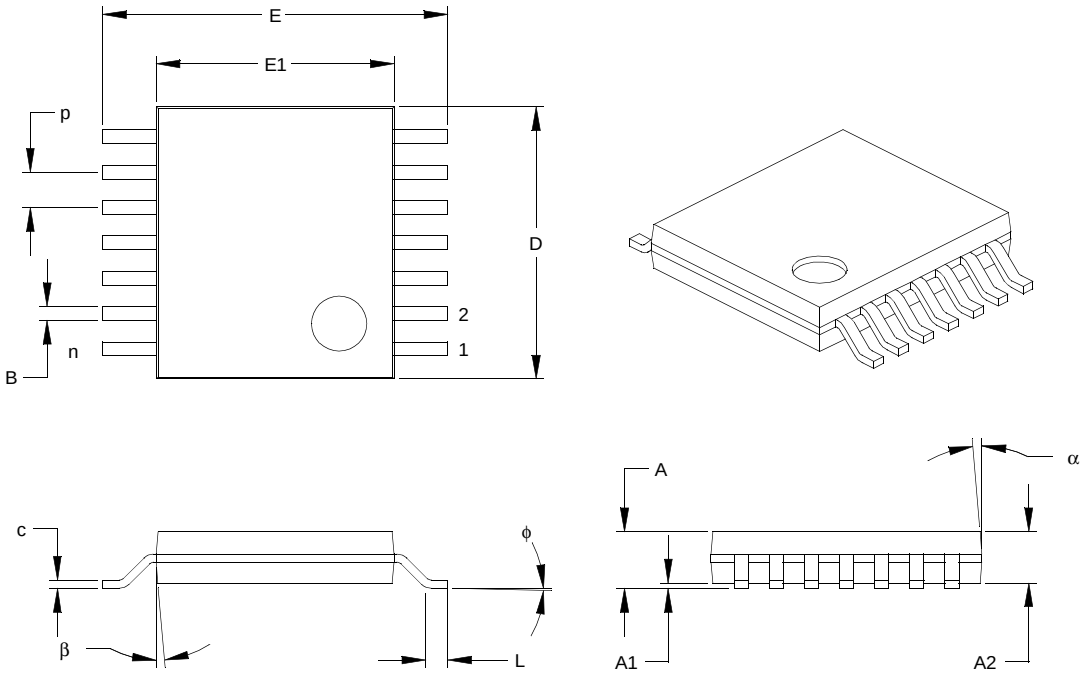
14-Lead Plastic Small Outline (SL) – Narrow, 150 mil Body (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.236	.244	5.79	5.99	6.20
Molded Package Width	E1	.150	.154	.157	3.81	3.90	3.99
Overall Length	D	.337	.342	.347	8.56	8.69	8.81
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

***** Controlling Parameter
§ Significant Characteristic
Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-065

14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body (TSSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.026 BSC			0.65 BSC	
Overall Height	A	.039	.041	.043	1.00	1.05	1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.193	.197	.201	4.90	5.00	5.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	φ	0°	4°	8°	0°	4°	8°
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α		12° REF			12° REF	
Mold Draft Angle Bottom	β		12° REF			12° REF	

***** Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
See ASME Y14.5M

REF: Reference Dimension, usually without tolerance, for information purposes only.
See ASME Y14.5M

JEDEC Equivalent: MO-153 AB-1

Drawing No. C04-087

Revised: 08-17-05

NOTES:

APPENDIX A: REVISION HISTORY

Revision B (November 2005)

The following is the list of modifications:

1. Added the following:
   a) SOT-23-5 package for the MCP6141 single op amps.
   b) SOT-23-6 package for the MCP6143 single op amps with Chip Select.
   c) Extended Temperature (-40°C to +125°C) op amps.
2. Updated specifications in **Section 1.0 "Electrical Characteristics"** for E-temp parts.
3. Corrected and updated plots in **Section 2.0 "Typical Performance Curves"**.
4. Added **Section 3.0 "Pin Descriptions"**.
5. Updated **Section 4.0 "Applications Information"** and added section on unused op amps.
6. Updated **Section 5.0 "Design Tools"** to include FilterLab.
7. Added SOT-23-5 and SOT-23-6 packages and corrected package marking information in **Section 6.0 "Packaging Information"**.
8. Added **Appendix A: "REVISION HISTORY"**.

Revision A (September 2002)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	- X	/ XX
Device	Temperature Range	Package

Device:	MCP6141:	Single Op Amp
	MCP6141T:	Single Op Amp (Tape and Reel for SOT-23, SOIC, MSOP)
	MCP6142:	Dual Op Amp
	MCP6142T:	Dual Op Amp (Tape and Reel for SOIC and MSOP)
	MCP6143:	Single Op Amp w/ $\overline{CS}$
	MCP6143T:	Single Op Amp w/ $\overline{CS}$ (Tape and Reel for SOT-23, SOIC, MSOP)
	MCP6144:	Quad Op Amp
	MCP6144T:	Quad Op Amp (Tape and Reel for SOIC and TSSOP)
Temperature Range:	I =	-40°C to +85°C (Industrial)
	E =	-40°C to +125°C (Extended)
Package:	CH =	Plastic Small Outline Transistor (SOT-23), 6-lead (Tape and Reel - MCP6143 only)
	MS =	Plastic Micro Small Outline (MSOP), 8-lead
	OT =	Plastic Small Outline Transistor (SOT-23), 5-lead (Tape and Reel - MCP6141 only)
	P =	Plastic DIP (300 mil Body), 8-lead, 14-lead
	SL =	Plastic SOIC (150 mil Body), 14-lead
	SN =	Plastic SOIC (150 mil Body), 8-lead
	ST =	Plastic TSSOP (4.4 mm Body), 14-lead

Examples:

a)	MCP6141-I/P:	Industrial Temp., 8LD PDIP package.
b)	MCP6141T-E/OT:	Tape and Reel, Extended Temp., 5LD SOT-23 package.
a)	MCP6142-I/SN:	Industrial Temp., 8LD SOIC package.
b)	MCP6142T-E/MS:	Tape and Reel, Extended Temp., 8LD MSOP package.
a)	MCP6143-I/P:	Industrial Temp., 8LD PDIP package.
b)	MCP6143T-E/CH:	Tape and Reel, Extended Temp., 6LD SOT-23 package.
a)	MCP6144-I/SL:	Industrial Temp., 14LD PDIP package.
b)	MCP6144T-E/ST:	Tape and Reel, Extended Temp., 14LD TSSOP package.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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Trademarks

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
ISO/TS 16949:2002

Microchip received ISO/TS-16949:2002 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona and Mountain View, California in October 2003. The Company's quality system processes and procedures are for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

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