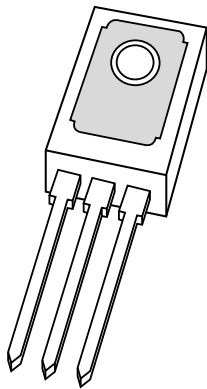


# DATA SHEET



## **BD329** NPN power transistor

Product specification  
Supersedes data of September 1994  
File under Discrete Semiconductors, SC04

1997 Mar 07

## NPN power transistor

BD329

## FEATURES

- High current (max. 3 A)
- Low voltage (max. 20 V).

## APPLICATIONS

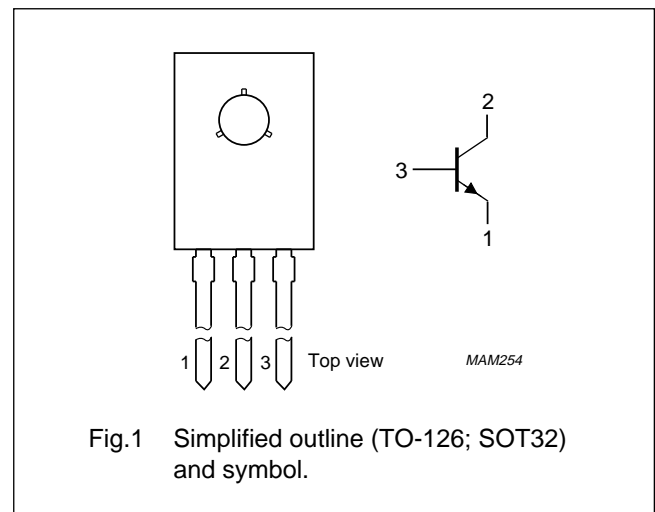
- Especially for battery equipped applications.

## DESCRIPTION

NPN power transistor in a TO-126; SOT32 plastic package. PNP complement: BD330.

## PINNING

PIN	DESCRIPTION
1	emitter
2	collector, connected to metal part of mounting surface
3	base



## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{CBO}$	collector-base voltage	open emitter	–	–	32	V
$V_{CEO}$	collector-emitter voltage	open base	–	–	20	V
$I_{CM}$	peak collector current		–	–	3	A
$P_{tot}$	total power dissipation	$T_{mb} \leq 45\text{ °C}$	–	–	15	W
$h_{FE}$	DC current gain	$I_C = 0.5\text{ A}; V_{CE} = 1\text{ V}$	85	–	375	
$f_T$	transition frequency	$I_C = 50\text{ mA}; V_{CE} = 5\text{ V}; f = 100\text{ MHz}$	–	130	–	MHz

## NPN power transistor

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**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CBO</sub>	collector-base voltage	open emitter	–	32	V
V <sub>CEO</sub>	collector-emitter voltage	open base	–	20	V
V <sub>EBO</sub>	emitter-base voltage	open collector	–	5	V
I <sub>C</sub>	collector current (DC)		–	3	A
I <sub>CM</sub>	peak collector current		–	3	A
I <sub>BM</sub>	peak base current		–	1	A
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> ≤ 45 °C	–	15	W
T <sub>stg</sub>	storage temperature		–65	+150	°C
T <sub>j</sub>	junction temperature		–	150	°C
T <sub>amb</sub>	operating ambient temperature		–65	+150	°C

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R <sub>th j-a</sub>	thermal resistance from junction to ambient	note 1	100	K/W
R <sub>th j-mb</sub>	thermal resistance from junction to mounting base		7	K/W

**Note**

1. Refer to TO-126; SOT32 standard mounting conditions.

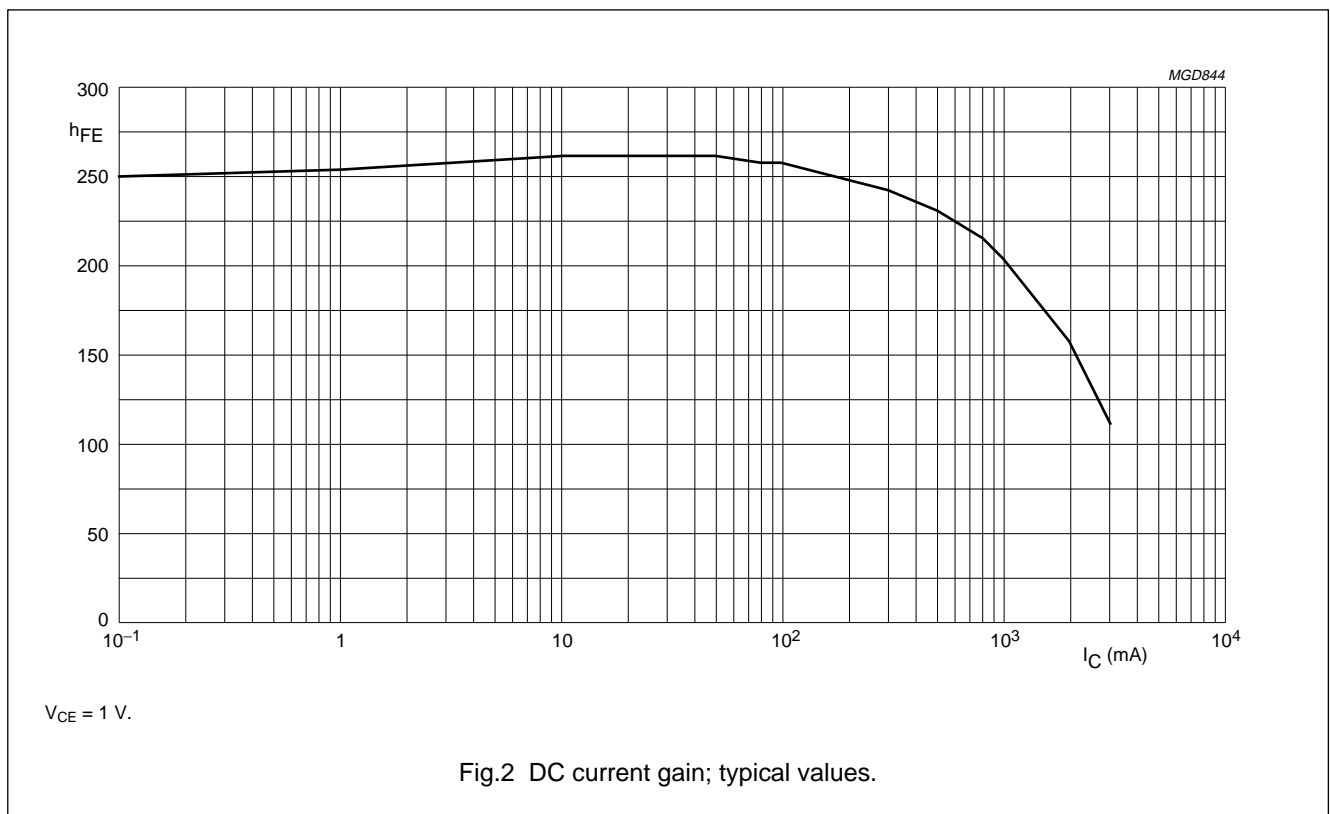
NPN power transistor

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**CHARACTERISTICS**

$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{CBO}$	collector cut-off current	$I_E = 0; V_{CB} = 32\text{ V}$	–	–	100	nA
		$I_E = 0; V_{CB} = 32\text{ V}; T_j = 150\text{ }^\circ\text{C}$	–	–	10	$\mu\text{A}$
$I_{EBO}$	emitter cut-off current	$I_C = 0; V_{EB} = 5\text{ V}$	–	–	100	nA
$h_{FE}$	DC current gain	$I_C = 0.5\text{ A}; V_{CE} = 1\text{ V}; \text{ see Fig.2}$	85	–	375	
		$I_C = 2\text{ A}; V_{CE} = 1\text{ V}; \text{ see Fig.2}$	40	–	–	
		$I_C = 5\text{ mA}; V_{CE} = 10\text{ V}$	50	–	–	
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = 2\text{ A}; I_B = 0.2\text{ A}$	–	–	0.5	V
$V_{BE}$	base-emitter voltage	$I_C = 5\text{ mA}; V_{CE} = 10\text{ V}$	–	0.6	–	V
		$I_C = 2\text{ A}; V_{CE} = 1\text{ V}$	–	–	1.2	V
$f_T$	transition frequency	$I_C = 50\text{ mA}; V_{CE} = 5\text{ V}; f = 100\text{ MHz}$	–	130	–	MHz
$\frac{h_{FE1}}{h_{FE2}}$	DC current gain ratio of the complementary pairs	$ I_C  = 0.5\text{ A};  V_{CE}  = 1\text{ V}$	–	–	1.6	

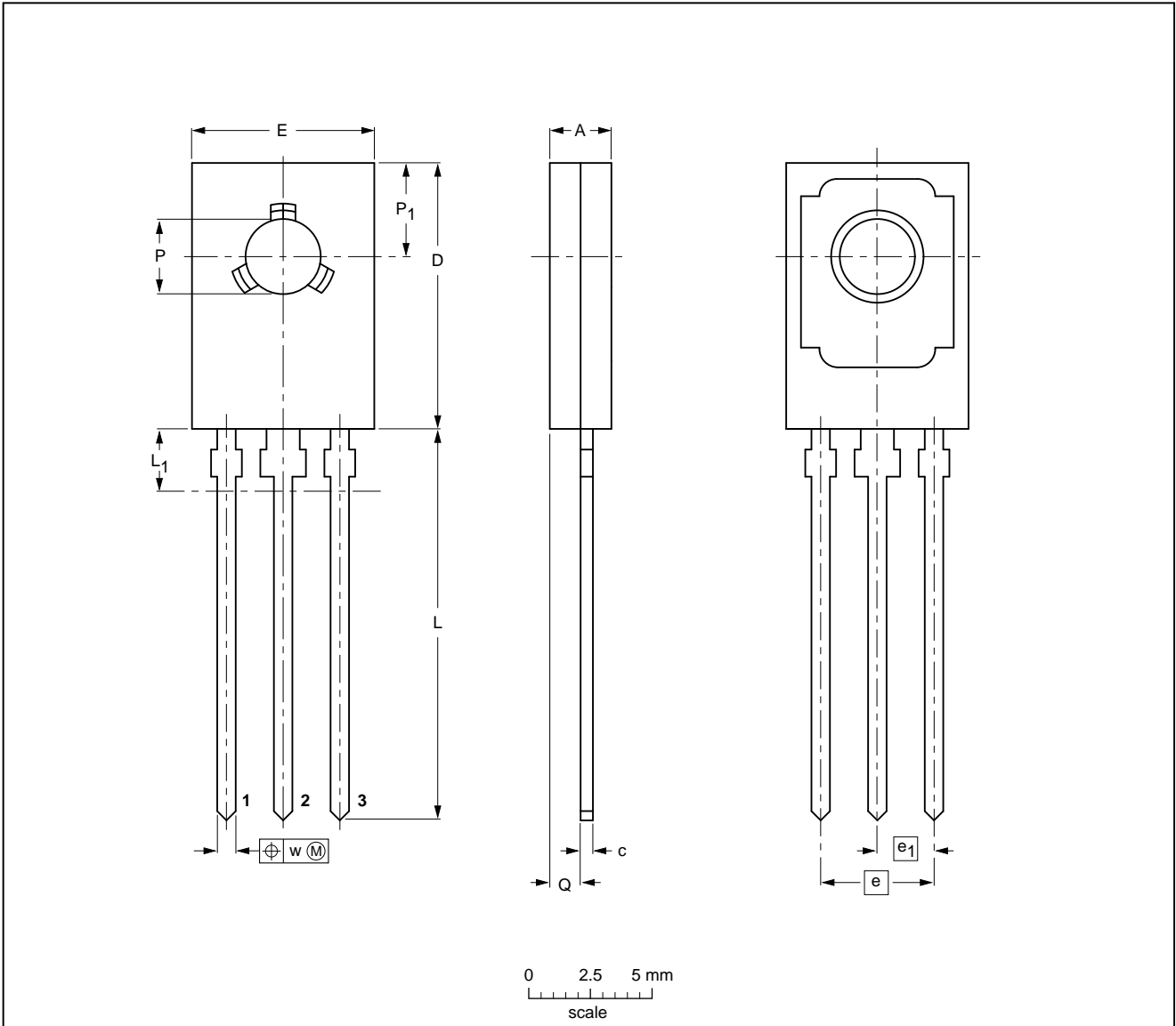


NPN power transistor

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PACKAGE OUTLINE

Plastic single-ended leaded (through hole) package; mountable to heatsink, 1 mounting hole; 3 leads SOT32



DIMENSIONS (mm are the original dimensions)

UNIT	A	$b_p$	c	D	E	e	$e_1$	L	$L_1^{(1)}$ max	Q	P	$P_1$	w
mm	2.7 2.3	0.88 0.65	0.60 0.45	11.1 10.5	7.8 7.2	4.58	2.29	16.5 15.3	2.54	1.5 0.9	3.2 3.0	3.9 3.6	0.254

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT32		TO-126				97-03-04

## NPN power transistor

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**DEFINITIONS**

<b>Data Sheet Status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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NPN power transistor

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