

SN74LVC1G11 Single 3-Input Positive-AND Gate

1 Features

- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 1000-V Charged-Device Model (C101)
- Available in the Texas Instruments NanoFree™ Package
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Maximum t_{pd} of 4.1 ns at 3.3 V
- Low Power Consumption, 10- μ A Maximum I_{CC}
- ± 24 -mA Output Drive at 3.3 V
- I_{off} Supports Partial-Power-Down Mode Operation

2 Applications

- AV Receivers
- DLP Front Projection System
- Digital Picture Frames
- Digital Radio
- Digital Still Cameras
- Digital Video Cameras (DVC)
- Embedded PCs
- E-Books
- Ethernet Switches
- GPS: Personal Navigation Devices
- Handset: Smartphones
- High-Speed Data Acquisition and Generation
- Military: Radar and Sonar
- Mobile Internet Devices
- Notebook PC and Netbooks
- Network-Attached Storage (NAS)
- Power Line Communication Modems
- Server PSU
- STB, DVR, and Streaming Media
- Speakers: USB
- Tablets: Enterprise
- Video Broadcasting and Infrastructure: Scalable Platform and IP-Based Multi-Format Transcoders
- Wireless Headsets, Keyboards, and Mice

3 Description

The SN74LVC1G11 performs the Boolean function $Y = A \cdot B \cdot C$ or $Y = \bar{A} + \bar{B} + \bar{C}$ in positive logic.

NanoFree package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVC1G11DBV	SOT-23 (6)	2.90 mm x 1.60 mm
SN74LVC1G11DCK	SC70 (6)	2.00 mm x 1.25 mm
SN74LVC1G11DRY	SON (6)	1.45 mm x 1.00 mm
SN74LVC1G11DSF	SON (6)	1.00 mm x 1.00 mm
SN74LVC1G11YZP	DSBGA (6)	1.41 mm x 0.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)

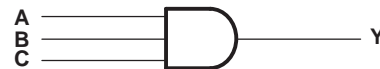


Table of Contents

1 Features	1	8 Detailed Description	10
2 Applications	1	8.1 Overview	10
3 Description	1	8.2 Functional Block Diagram	10
4 Revision History	2	8.3 Feature Description	10
5 Pin Configuration and Functions	3	8.4 Device Functional Modes	10
6 Specifications	4	9 Application and Implementation	11
6.1 Absolute Maximum Ratings	4	9.1 Application Information	11
6.2 ESD Ratings	4	9.2 Typical Application	11
6.3 Recommended Operating Conditions	4	10 Power Supply Recommendations	12
6.4 Thermal Information	5	11 Layout	13
6.5 Electrical Characteristics	5	11.1 Layout Guidelines	13
6.6 Switching Characteristics, $C_L = 15$ pF, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	6	11.2 Layout Example	13
6.7 Switching Characteristics, $C_L = 30$ pF or 50 pF, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	6	12 Device and Documentation Support	14
6.8 Switching Characteristics, $C_L = 30$ pF or 50 pF, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	6	12.1 Documentation Support	14
6.9 Operating Characteristics	6	12.2 Receiving Notification of Documentation Updates	14
6.10 Typical Characteristics	7	12.3 Community Resources	14
7 Parameter Measurement Information	8	12.4 Trademarks	14
		12.5 Electrostatic Discharge Caution	14
		13 Mechanical, Packaging, and Orderable Information	14

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

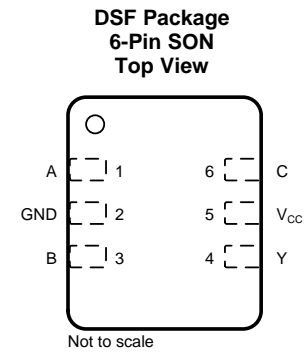
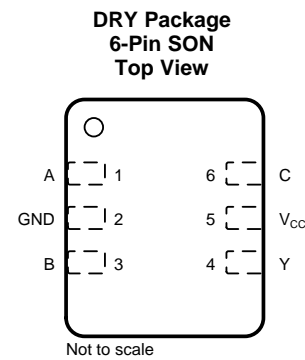
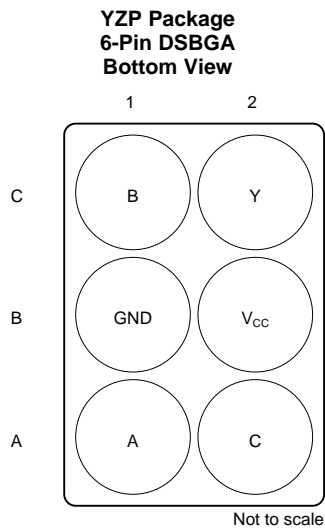
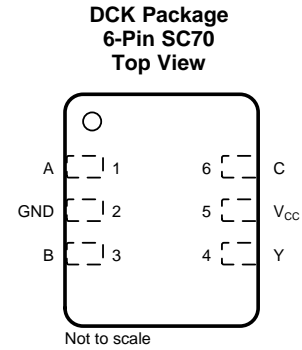
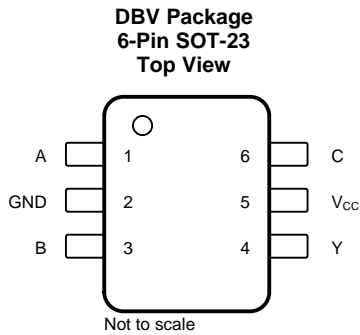
Changes from Revision G (December 2015) to Revision H	Page
• Deleted 200-V Machine Model from <i>Features</i>	1
• Changed pinout images to improve clarity of pin names and pin numbers	3
• Added DSBGA pin numbers to <i>Pin Functions</i> table	3
• Added Operating free-air temperature, T_A for BGA package	5
• Added <i>Receiving Notification of Documentation Updates</i> section	14

Changes from Revision F (December 2013) to Revision G	Page
• Added <i>Applications</i> section, <i>Device Information</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section.	1

Changes from Revision E (December 2011) to Revision F	Page
• Updated document to new TI data sheet format	1
• Removed <i>Ordering Information</i> table.	1
• Updated operating temperature range	4

Changes from Revision D (January 2007) to Revision E	Page
• Added DRY and DSF packages to data sheet	1

5 Pin Configuration and Functions



See mechanical drawings for dimensions.

Pin Functions

NAME	PIN		I/O	DESCRIPTION
	SOT-23, SC70, SON, SON	DSBGA		
A	1	A1	I	A Input
B	3	C1	I	B Input
C	6	A2	I	C Input
GND	2	B1	—	Ground
V _{CC}	5	B2	—	Power Supply
Y	4	C2	O	Y Output

6 Specifications

6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	-0.5	6.5	V
V _I	Input voltage ⁽²⁾	-0.5	6.5	V
V _O	Voltage applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	6.5	V
V _O	Voltage applied to any output in the high or low state ⁽²⁾⁽³⁾	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current V _I < 0		-50	mA
I _{OK}	Output clamp current V _O < 0		-50	mA
I _O	Continuous output current		±50	mA
	Continuous current through V _{CC} or GND		±100	mA
T _J	Junction temperature		150	°C
T _{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

 See note⁽¹⁾.

			MIN	MAX	UNIT
V _{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 3 V to 3.6 V	2		
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V		0.7	
		V _{CC} = 3 V to 3.6 V		0.8	
		V _{CC} = 4.5 V to 5.5 V		0.3 × V _{CC}	
V _I	Input voltage		0	5.5	V
V _O	Output voltage		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65 V		-4	mA
		V _{CC} = 2.3 V		-8	
		V _{CC} = 3 V		-16	
		V _{CC} = 4.5 V		-24	

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#), SCBA004.

Recommended Operating Conditions (continued)

See note⁽¹⁾.

		MIN	MAX	UNIT	
I_{OL}	Low-level output current	$V_{CC} = 1.65\text{ V}$	4	mA	
		$V_{CC} = 2.3\text{ V}$	8		
		$V_{CC} = 3\text{ V}$	16		
			24		
		$V_{CC} = 4.5\text{ V}$	32		
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}, 2.5\text{ V} \pm 0.2\text{ V}$	20	ns/V	
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	10		
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	10		
T_A	Operating free-air temperature	BGA package	-40	85	°C
		All other packages	-40	125	

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	SN74LVC1G11					UNIT	
	DBV (SOT-23)	DCK (SC70)	DRY (SON)	YZP (DSBGA)	DSF (SON)		
	6 PINS	6 PINS	6 PINS	6 PINS	6 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	195.9	260.1	424.6	105.8	413.7	°C/W
$R_{\theta JCTop}$	Junction-to-case (top) thermal resistance	177.4	98.1	309	1.6	226.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51.7	63.1	292	10.8	317	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	61.3	2.2	135.4	3.1	37.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	51.3	62.4	292	10.8	317	°C/W
$R_{\theta JCbott}$	Junction-to-case (bottom) thermal resistance	—	—	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	$I_{OH} = -100\ \mu\text{A}$	1.65 V to 5.5 V	$V_{CC} - 0.1$		V	
	$I_{OH} = -4\text{ mA}$	1.65 V	1.2			
	$I_{OH} = -8\text{ mA}$	2.3 V	1.9			
	$I_{OH} = -16\text{ mA}$	3 V	2.4			
	$I_{OH} = -24\text{ mA}$		2.3			
	$I_{OH} = -32\text{ mA}$	4.5 V	3.8			
V_{OL}	$I_{OL} = 100\ \mu\text{A}$	1.65 V to 5.5 V	0.1		V	
	$I_{OL} = 4\text{ mA}$	1.65 V	0.45			
	$I_{OL} = 8\text{ mA}$	2.3 V	0.3			
	$I_{OL} = 16\text{ mA}$	3 V	0.4			
	$I_{OL} = 24\text{ mA}$		0.55			
	$I_{OL} = 32\text{ mA}$	4.5 V	0.55			
I_i	All inputs	$V_i = 5.5\text{ V}$ or GND	0 to 5.5 V		± 5	μA
I_{off}		V_i or $V_o = 5.5\text{ V}$	0		± 10	μA
I_{CC}		$V_i = 5.5\text{ V}$ or GND, $I_o = 0$	1.65 V to 5.5 V		10	μA
ΔI_{CC}		One input at $V_{CC} - 0.6\text{ V}$, Other inputs at V_{CC} or GND	3 V to 5.5 V		500	μA
C_i		$V_i = V_{CC}$ or GND	3.3 V		3.5	pF

SN74LVC1G11

SCES487H–SEPTEMBER 2003–REVISED NOVEMBER 2016

www.ti.com
6.6 Switching Characteristics, $C_L = 15\text{ pF}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$

 over recommended operating free-air temperature range, $C_L = 15\text{ pF}$ (unless otherwise noted) (see [Figure 2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
t_{pd}	A, B, or C	Y	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	2.6	15.2	ns
			$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	1.6	5.6	
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	1.2	4.1	
			$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	1	3.1	

6.7 Switching Characteristics, $C_L = 30\text{ pF}$ or 50 pF , $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$

 over recommended operating free-air temperature range, $C_L = 30\text{ pF}$ or 50 pF (unless otherwise noted) (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
t_{pd}	A, B, or C	Y	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	2.9	17.2	ns
			$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	1.4	6.2	
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	1.3	4.9	
			$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	1	3.5	

6.8 Switching Characteristics, $C_L = 30\text{ pF}$ or 50 pF , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$

 over recommended operating free-air temperature range, $C_L = 30\text{ pF}$ or 50 pF (unless otherwise noted) (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
t_{pd}	A, B, or C	Y	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	2.9	20	ns
			$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	1.4	7.8	
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	1.3	6.2	
			$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	1	4.6	

6.9 Operating Characteristics
 $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	V_{CC}	TYP	UNIT	
C_{pd}	Power dissipation capacitance	$f = 10\text{ MHz}$	$V_{CC} = 1.8\text{ V}$	18	pF
			$V_{CC} = 2.5\text{ V}$	19	
			$V_{CC} = 3.3\text{ V}$	20	
			$V_{CC} = 5\text{ V}$	23	

6.10 Typical Characteristics

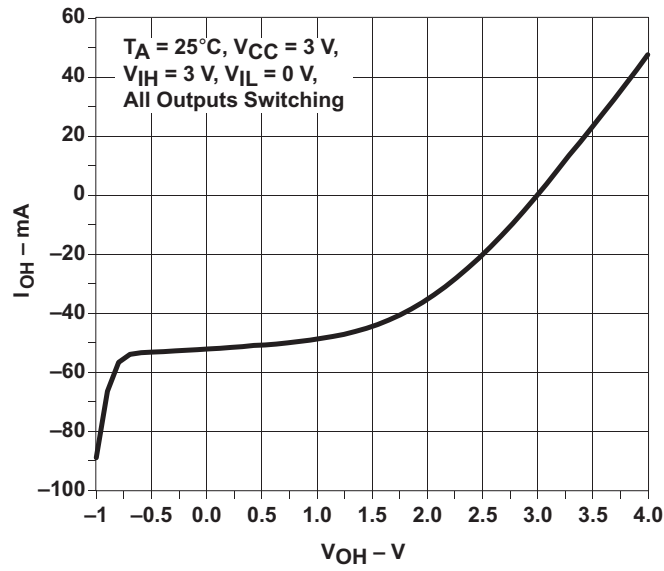
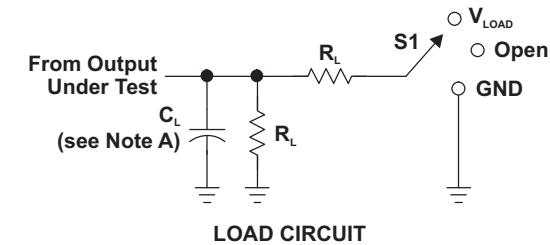


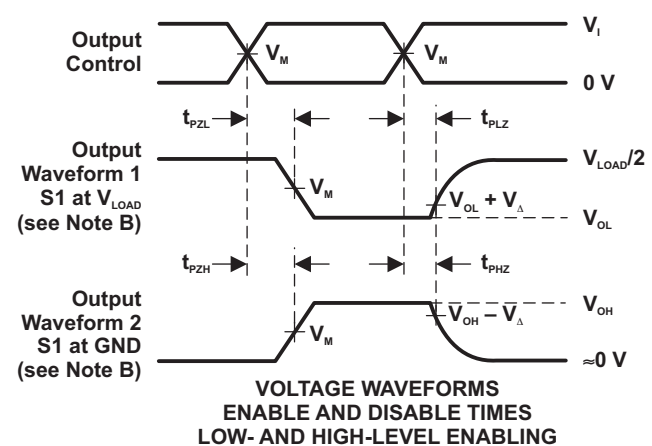
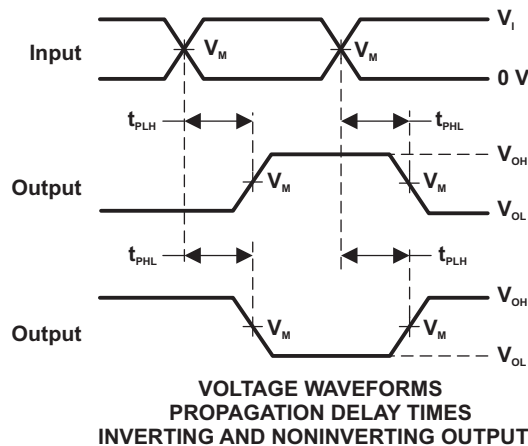
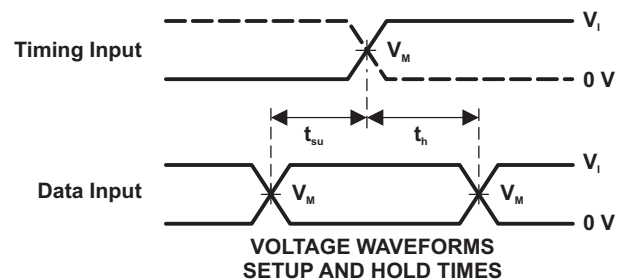
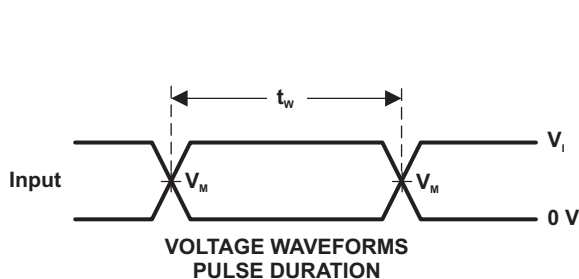
Figure 1. Output Current Drive vs HIGH-level Output Voltage

7 Parameter Measurement Information



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

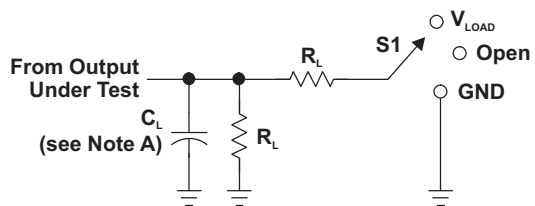
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_i	t_i/t_r					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	15 pF	1 M Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_o = 50\ \Omega$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

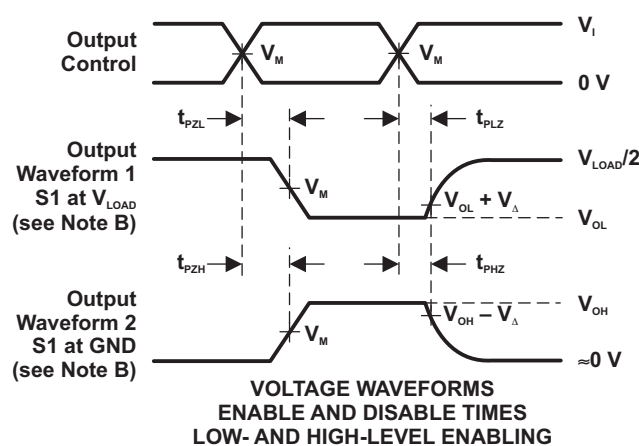
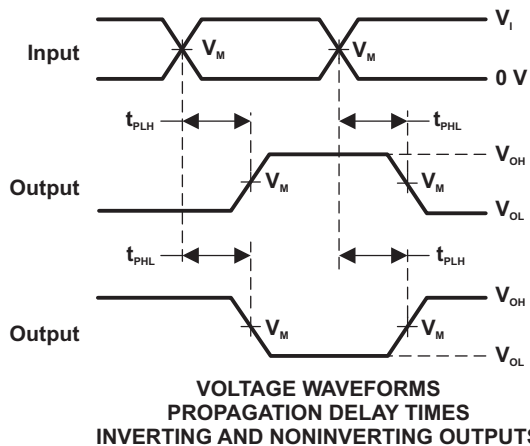
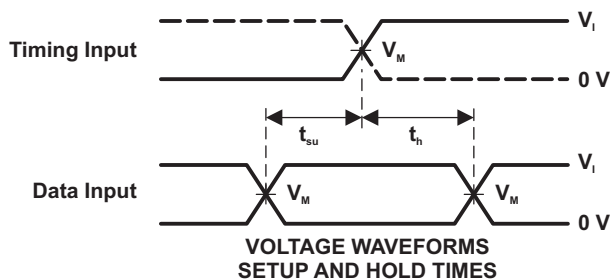
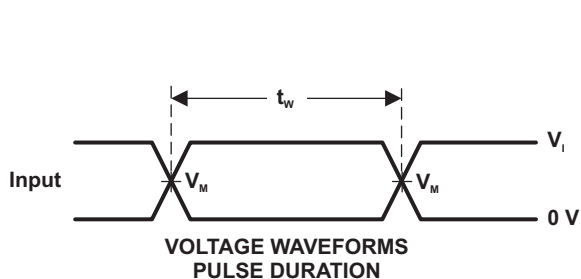
Parameter Measurement Information (continued)



LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_o = 50\ \Omega$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{on} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

This 3-input AND gate is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G11 device features a three-input AND gate. The output state is determined by eight patterns of 3-bit input. All inputs can be connected to V_{CC} or GND.

This device is fully-specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

8.2 Functional Block Diagram



Figure 4. Logic Diagram (Positive Logic)

8.3 Feature Description

The SN74LVC1G11 device has a wide operating V_{CC} range of 1.65 V to 5.5 V, which allows use in a broad range of systems. The 5.5-V I/Os allow down translation and also allow voltages at the inputs when $V_{CC} = 0$ V.

8.4 Device Functional Modes

Table 1 lists the functional modes of SN74LVC1G11.

Table 1. Function Table

INPUTS			OUTPUT Y
A	B	C	
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Validate and test the design implementation to confirm system functionality.

9.1 Application Information

The SN74LVC1G11 device offers logical AND configuration for many design applications. This example describes basic power sequencing using the AND gate configuration. Power sequencing is often used in applications that require a processor or other delicate device with specific voltage timing requirements in order to protect the device from malfunctioning. In the application below, the power-good signals from the supplies tell the MCU to continue an operation.

9.2 Typical Application

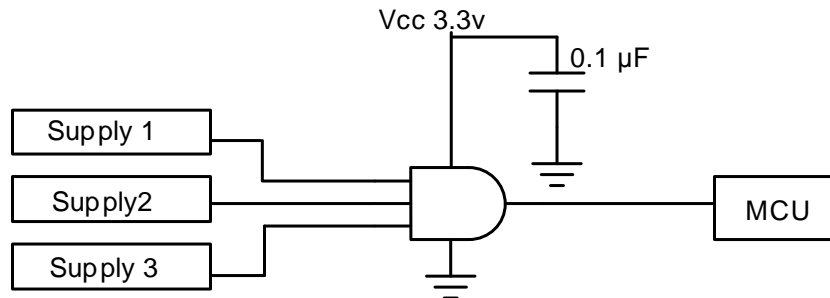


Figure 5. Typical Application Diagram

9.2.1 Design Requirements

- Recommended input conditions:
 - For rise time and fall time specifications, see $\Delta t/\Delta v$ in the [Recommended Operating Conditions](#) table.
 - For specified high and low levels, see V_{IH} and V_{IL} in the [Recommended Operating Conditions](#) table.
 - Inputs and outputs are overvoltage tolerant and can therefore go as high as 5.5 V at any valid V_{CC} .
- Recommended output conditions:
 - Load currents must not exceed ± 50 mA.
- Frequency selection criterion:
 - [Figure 6](#) illustrates the effects of frequency on output current.
 - Added trace resistance and capacitance can reduce maximum frequency capability. Follow the layout practices listed in the [Layout](#) section.

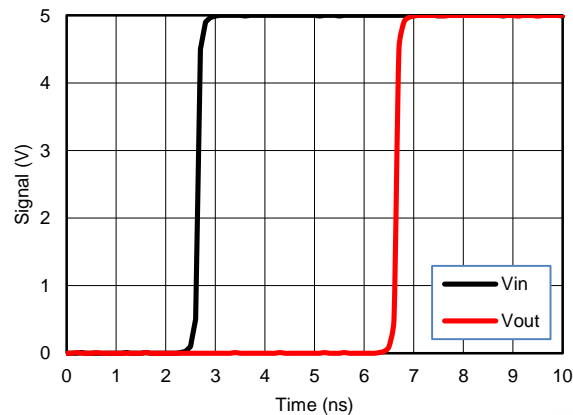
Typical Application (continued)

9.2.2 Detailed Design Procedure

The SN74LVC1G11 device uses CMOS technology and has balanced output drive. Avoid bus contentions that can drive currents that can exceed maximum limits.

The SN74LVC1G11 allows for performing the logical AND function with digital signals. Maintain input signals as close as possible to either 0 V or V_{CC} for optimal operation.

9.2.3 Application Curve



$$V_{CC} = 5 \text{ V}$$

Figure 6. Simulated Input-to-Output Voltage Response Showing Propagation Delay

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the [Recommended Operating Conditions](#) table.

To prevent power disturbance, ensure good bypass capacitance for each V_{CC} terminal. For devices with a single-supply, a 0.1- μF bypass capacitor is recommended. If multiple pins are labeled V_{CC} , then a 0.01- μF or 0.022- μF capacitor is recommended for each V_{CC} because the V_{CC} pins are tied together internally. For devices with dual supply pins operating at different voltages, for example V_{CC} and V_{DD} , a 0.1- μF bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1 μF and 1 μF are commonly used in parallel. Place the bypass capacitor as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple-bit logic devices, inputs must never float.

In many cases, functions (or parts of functions) of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or when only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected, because the undefined voltages at the outside connections result in undefined operational states. Figure 7 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it disables the output section of the part when asserted, which does not disable the input section of the I/Os. Therefore, the I/Os cannot float when disabled.

11.2 Layout Example

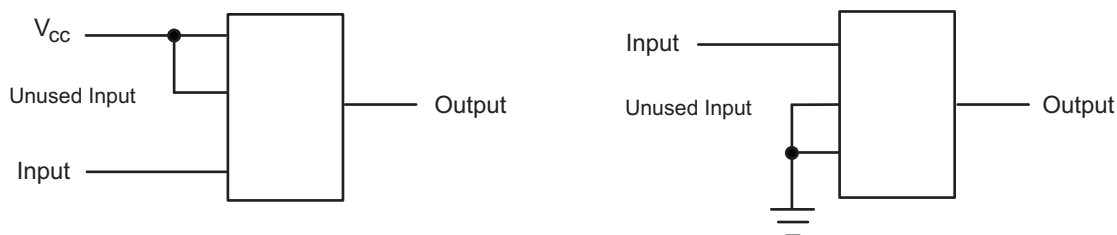


Figure 7. Layout Diagrams

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- [Implications of Slow or Floating CMOS Inputs](#), SCBA004
- [Selecting the Right Texas Instruments Signal Switch](#), SZZA030

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

NanoFree, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC1G11DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-40 to 125	(C115 ~ C11F ~ C11K ~ C11R)	Samples
SN74LVC1G11DBVRE4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C11F	Samples
SN74LVC1G11DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C11F	Samples
SN74LVC1G11DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C35 ~ C3F ~ C3K ~ C3R)	Samples
SN74LVC1G11DCKRE4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C35 ~ C3F ~ C3K ~ C3R)	Samples
SN74LVC1G11DCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C35 ~ C3F ~ C3K ~ C3R)	Samples
SN74LVC1G11DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C3	Samples
SN74LVC1G11DSFR	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C3	Samples
SN74LVC1G11YZPR	ACTIVE	DSBGA	YZP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C3N	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

-
- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC1G11 :

- Automotive: [SN74LVC1G11-Q1](#)
- Enhanced Product: [SN74LVC1G11-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G11DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G11DBVRG4	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G11DCKR	SC70	DCK	6	3000	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC1G11DCKR	SC70	DCK	6	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G11DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74LVC1G11DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G11YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

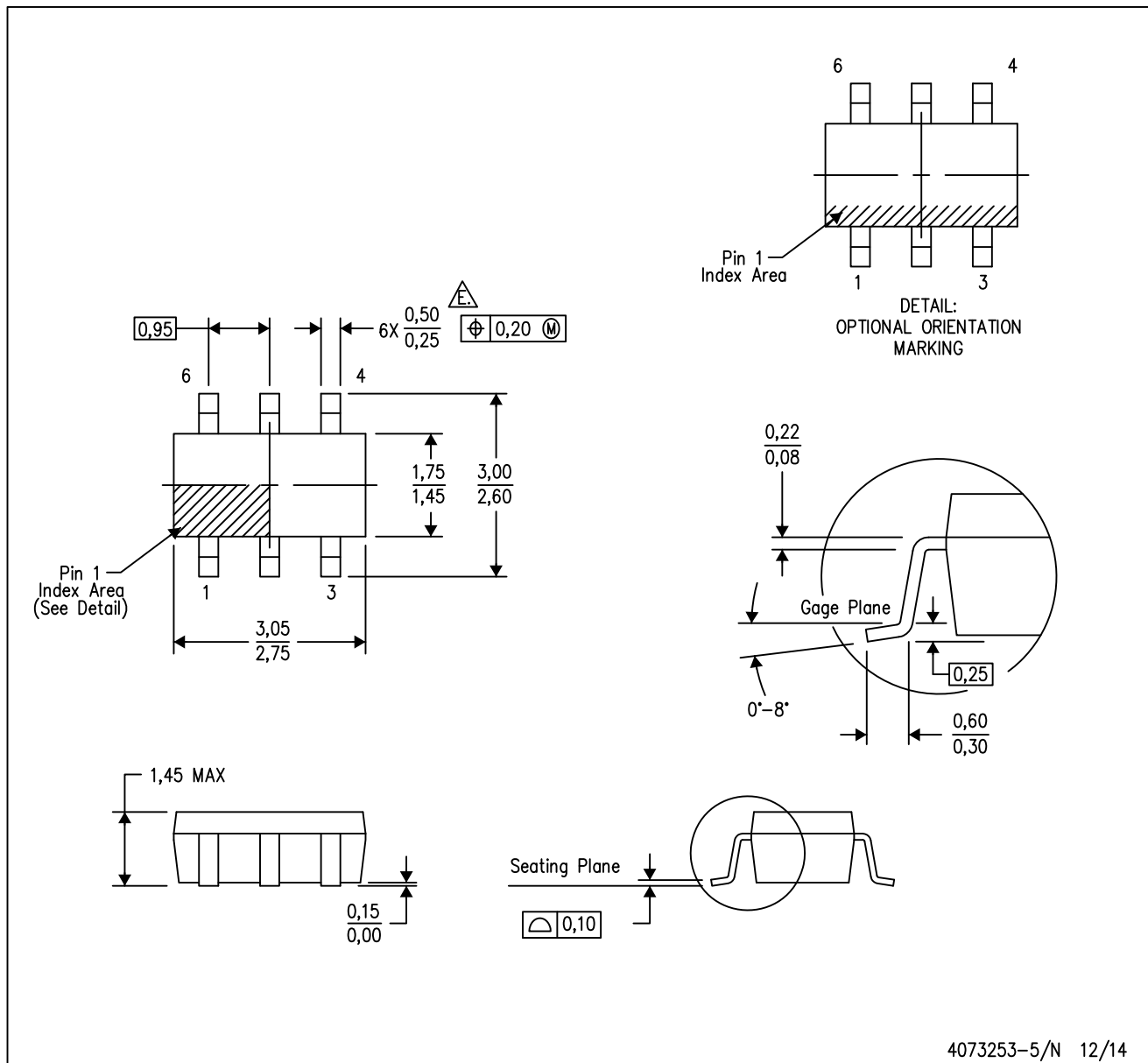

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G11DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
SN74LVC1G11DBVRG4	SOT-23	DBV	6	3000	180.0	180.0	18.0
SN74LVC1G11DCKR	SC70	DCK	6	3000	205.0	200.0	33.0
SN74LVC1G11DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1G11DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G11DSFR	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC1G11YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0

MECHANICAL DATA

DBV (R-PDSO-G6)

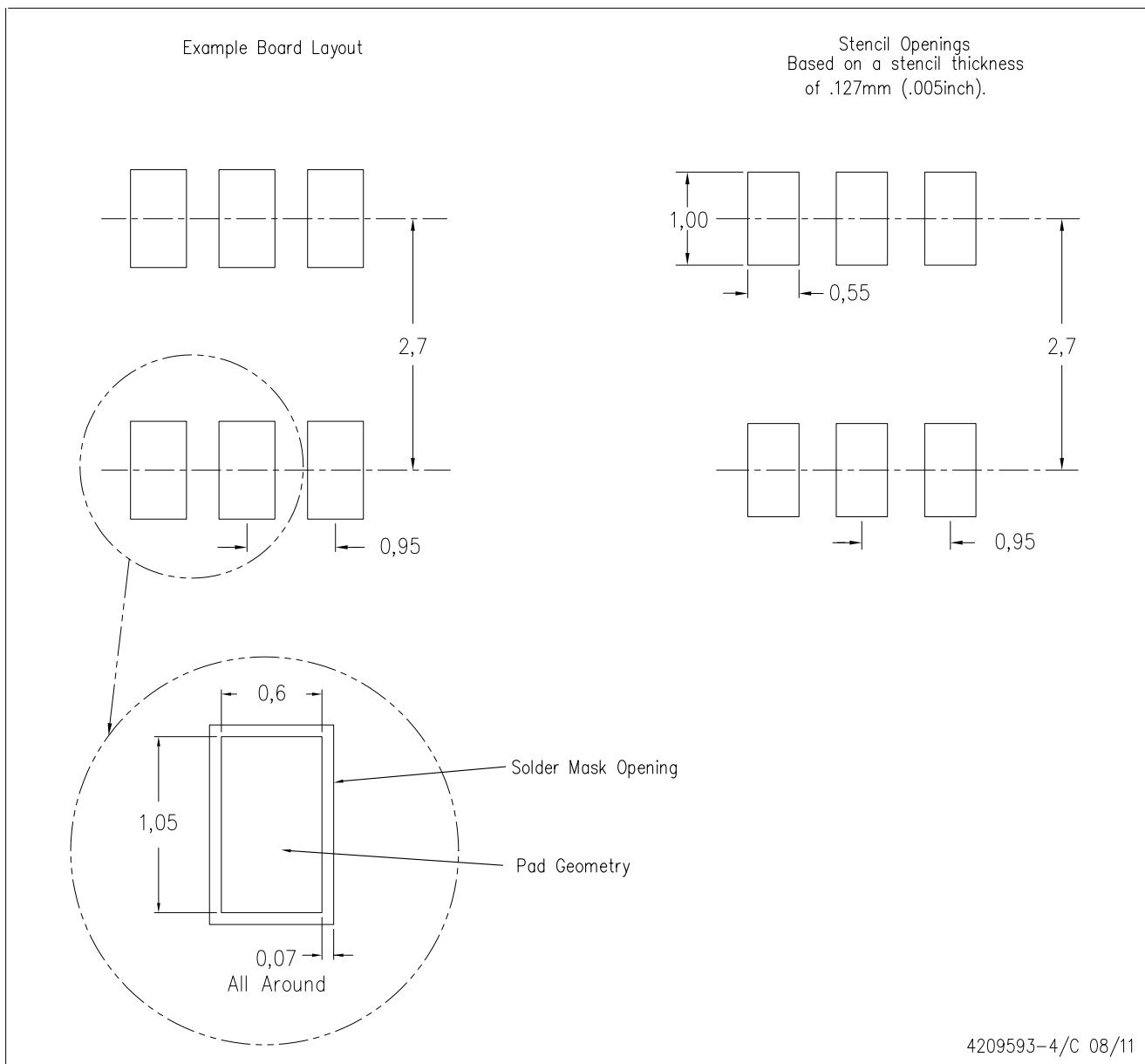
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- ⚠ Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DBV (R-PDSO-G6)

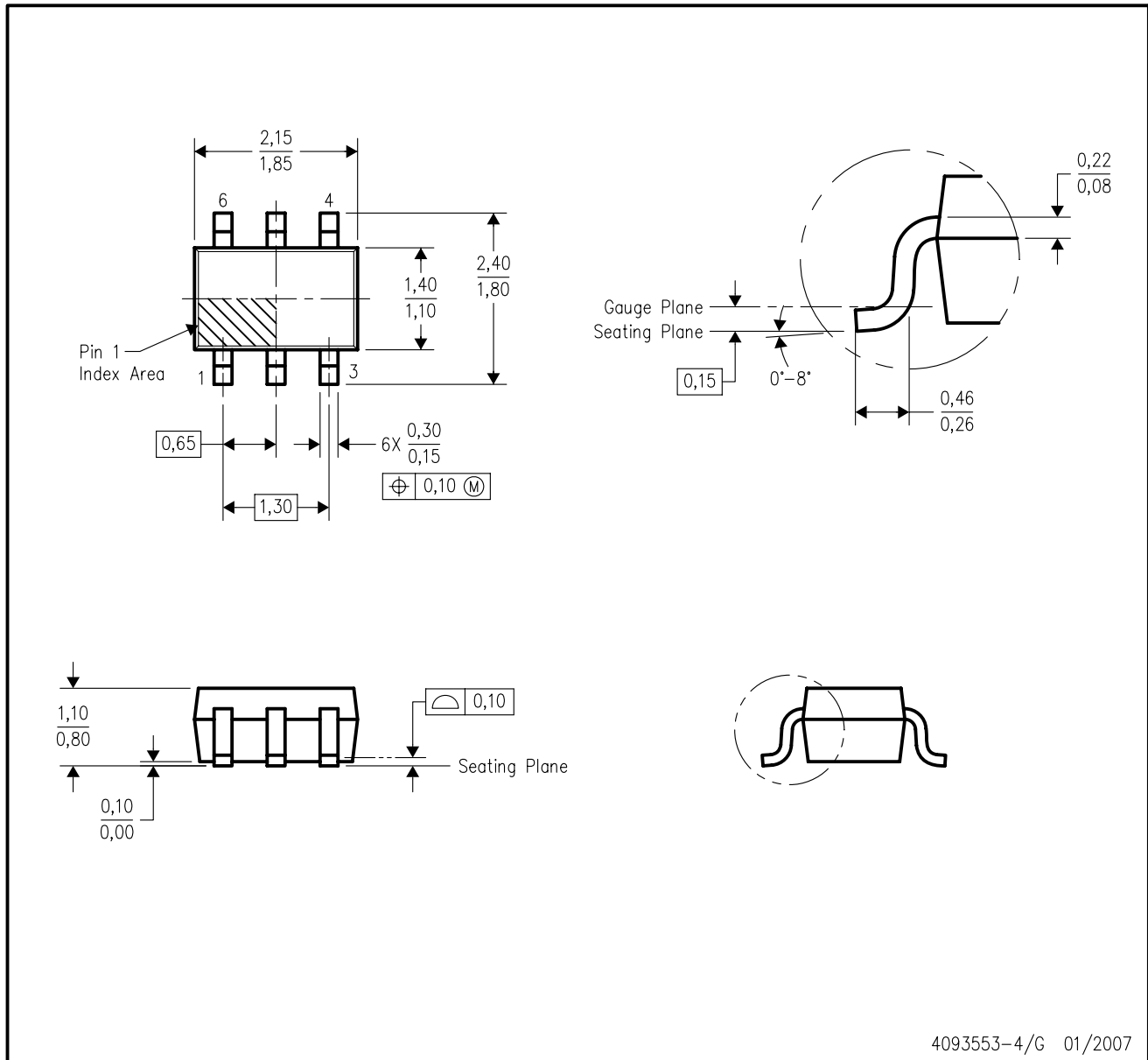
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DCK (R-PDSO-G6)

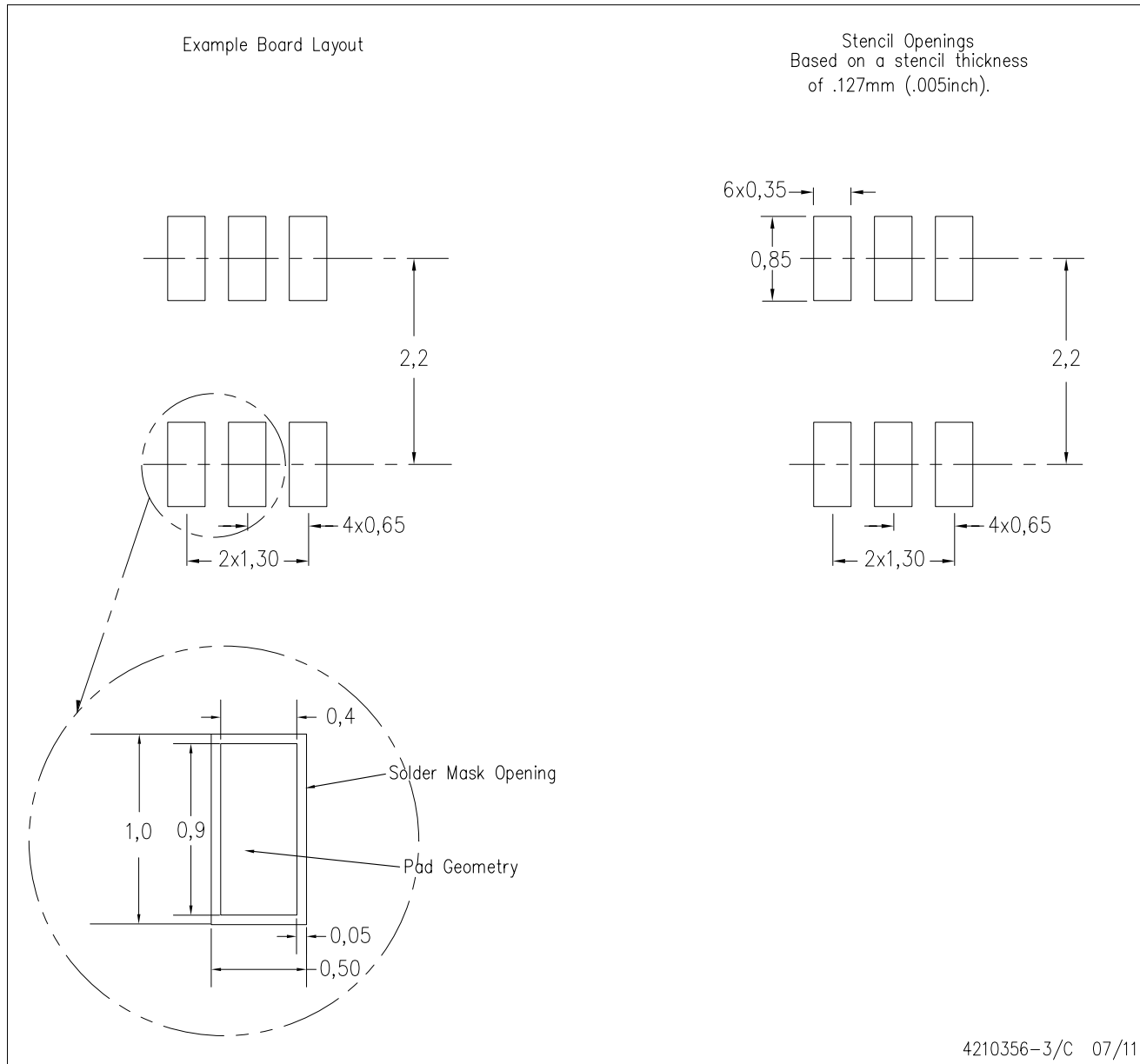
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-203 variation AB.

DCK (R-PDSO-G6)

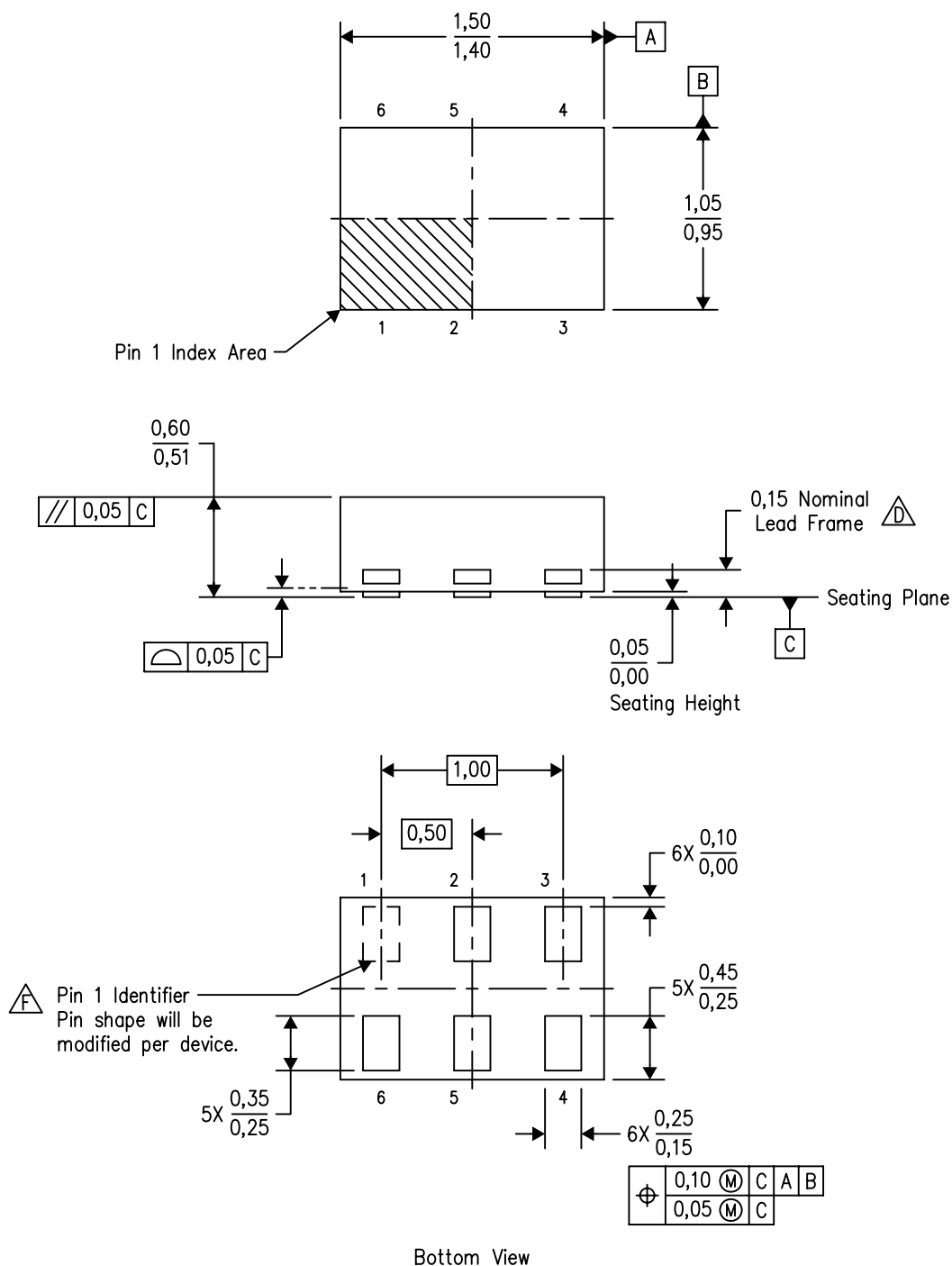
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DRY (R-PUSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD

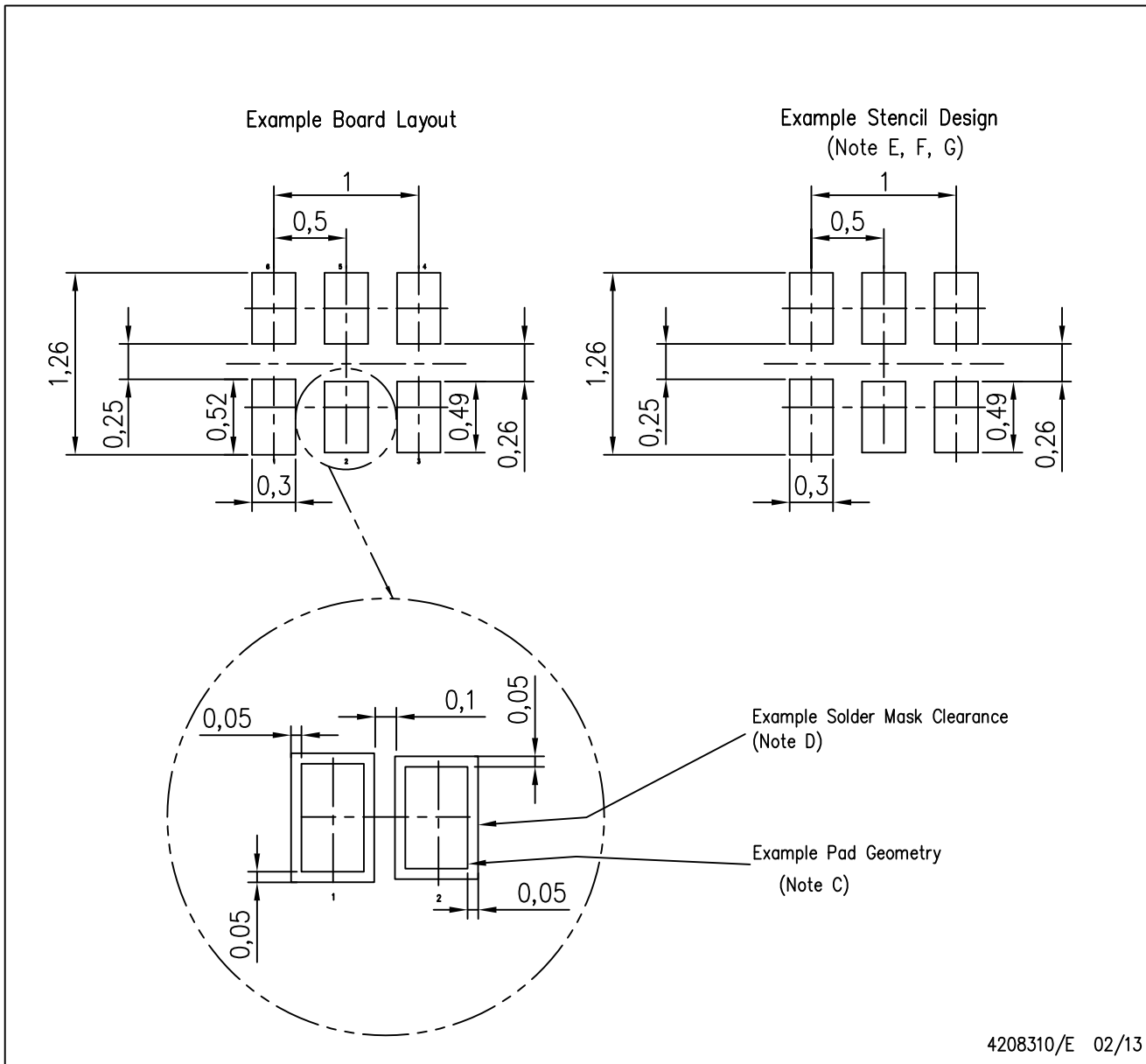


4207181/F 12/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. SON (Small Outline No-Lead) package configuration.
 - $\triangle D$ The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
 - E. This package complies to JEDEC MO-287 variation UFAD.
 - $\triangle F$ See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

DRY (R-PUSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD

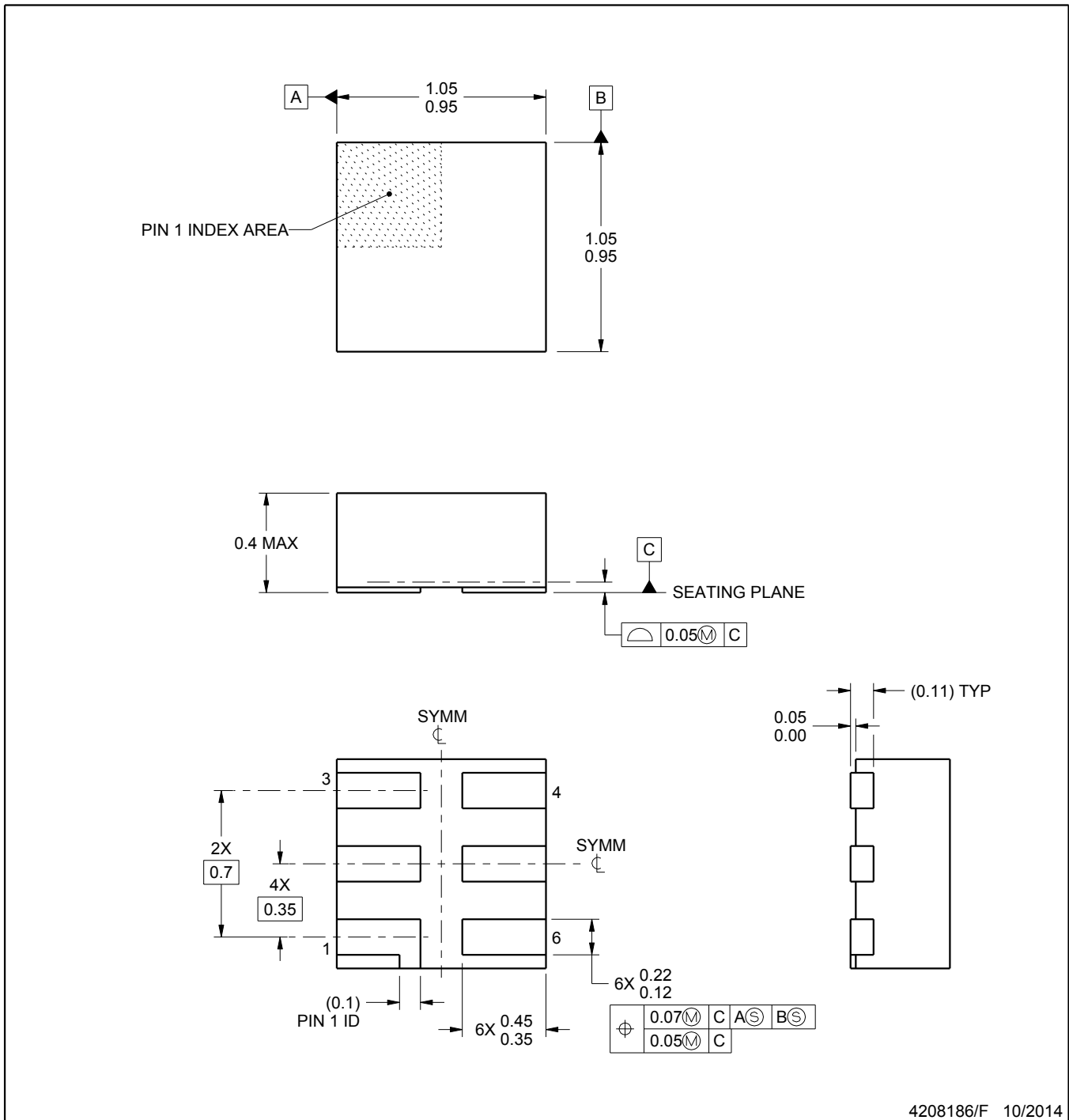


- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

MECHANICAL DATA

DSF (S-PX2SON-N6)

PLASTIC SMALL OUTLINE NO-LEAD

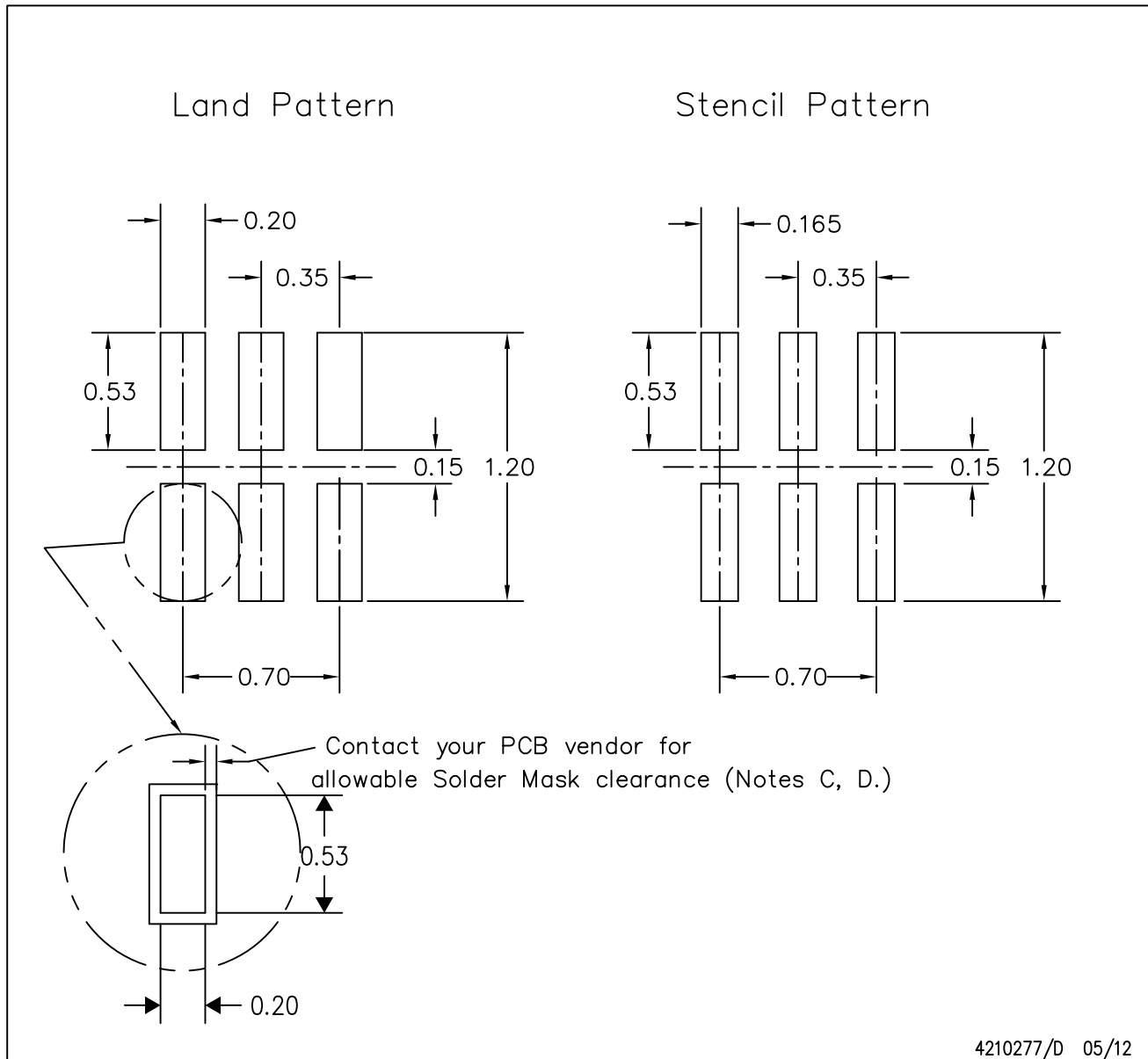


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

DSF (S-PX2SON-N6)

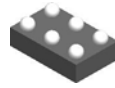
PLASTIC SMALL OUTLINE NO-LEAD



4210277/D 05/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads. If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
 - Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
 - Component placement force should be minimized to prevent excessive paste block deformation.

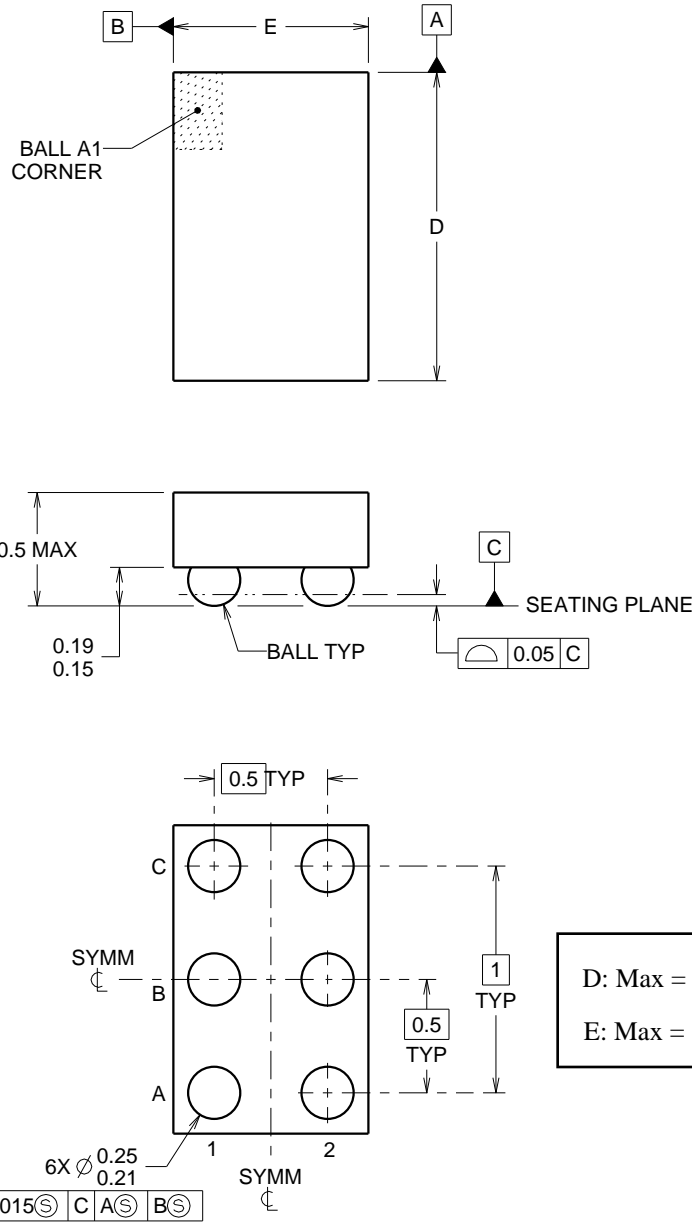
YZP0006



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4219524/A 06/2014

NOTES:

NanoFree Is a trademark of Texas Instruments.

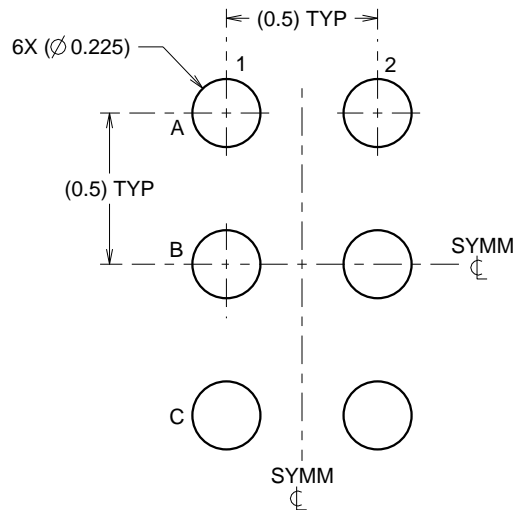
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.

EXAMPLE BOARD LAYOUT

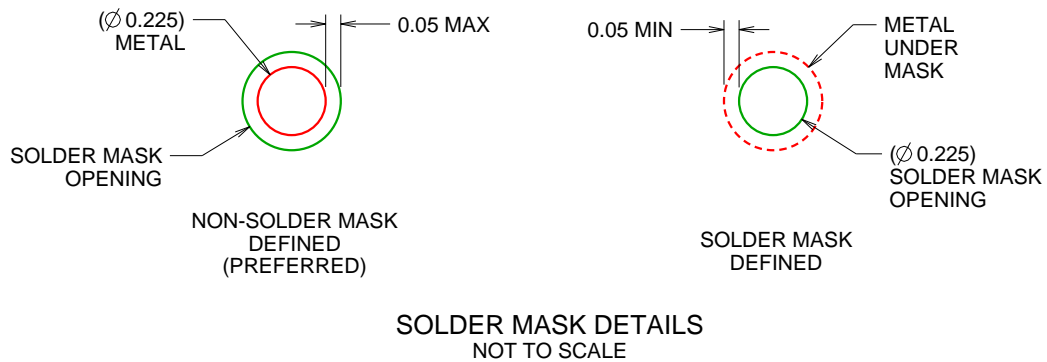
YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4219524/A 06/2014

NOTES: (continued)

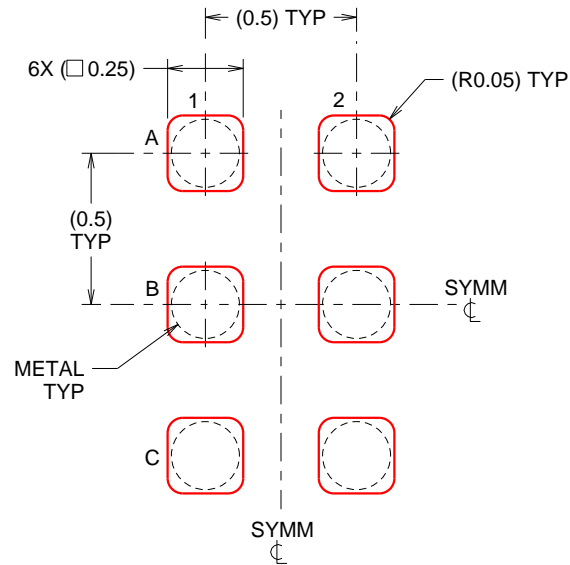
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).

EXAMPLE STENCIL DESIGN

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219524/A 06/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ("TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>), [evaluation modules](#), and [samples](http://www.ti.com/sc/docs/sampterm.htm) (<http://www.ti.com/sc/docs/sampterm.htm>).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2017, Texas Instruments Incorporated