ANALOG DEVICES

DC-to-2.5 GHz
High IP3 Active Mixer

AD8343

FEATURES
High-Performance Active Mixer
Broadband Operation to 2.5 GHz
Conversion Gain: 7.1 dB
Input IP3: 16.5 dBm
LO Drive: –10 dBm
Noise Figure: 14.1 dB
Input P1 dB: 2.8 dBm
Differential LO, IF and RF Ports
50 Ω LO Input Impedance
Single-Supply Operation: 5 V @ 50 mA Typical
Power-Down Mode @ 20 μA Typical

APPLICATIONS
Cellular Base Stations
Wireless LAN
Satellite Converters
SONET/SDH Radio
Radio Links
RF Instrumentation

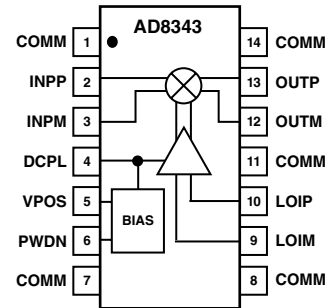## FUNCTIONAL BLOCK DIAGRAM

PRODUCT DESCRIPTION
The AD8343 is a high-performance broadband active mixer. Having wide bandwidth on all ports and very low intermodulation distortion, the AD8343 is well suited for demanding transmit or receive channel applications.

The AD8343 provides a typical conversion gain of 7.1 dB. The integrated LO driver supports a 50 Ω differential input impedance with low LO drive level, helping to minimize external component count.

The open-emitter differential inputs may be interfaced directly to a differential filter or driven through a balun (transformer) to provide a balanced drive from a single-ended source.

The open-collector differential outputs may be used to drive a differential IF signal interface or converted to a single-ended signal through the use of a matching network or transformer. When centered on the VPOS supply voltage, the outputs may swing ±1 V.

The LO driver circuitry typically consumes 15 mA of current. Two external resistors are used to set the mixer core current for required performance resulting in a total current of 20 mA to 60 mA. This corresponds to power consumption of 100 mW to 300 mW with a single 5 V supply.

The AD8343 is fabricated on Analog Devices' proprietary, high-performance 25 GHz silicon bipolar IC process. The AD8343 is available in a 14-lead TSSOP package. It operates over a –40°C to +85°C temperature range. A device-populated evaluation board is available to facilitate device matching.

REV. 0

AD8343–SPECIFICATIONS

BASIC OPERATING CONDITIONS (V_S = 5.0 V, T_A = 25°C)

Parameter	Conditions	Figure	Min	Typ	Max	Unit
INPUT INTERFACE (INPP, INPM)						
Differential Open Emitter						
DC Bias Voltage	Internally Generated		1.1	1.2	1.3	V
Operating Current Each Input (I_O)	Current Set by R3, R4	24	5	16	20	mA
Value of Bias Setting Resistor[1]	1% Bias Resistors; R3, R4	24		68.1		Ω
Port Differential Impedance	f = 50 MHz; R3 and R4 = 68.1 Ω	9		2.7 + j 6.8		Ω
OUTPUT INTERFACE (OUTP, OUTM)						
Differential Open Collector						
DC Bias Voltage	Externally Applied		4.5	5	5.5	V
Voltage Swing			1.65	$V_S \pm 1$	$V_S + 2$	V
Operating Current Each Output	Same as Input Current			I_O		mA
Port Differential Impedance	f = 50 MHz	12		900 – j 77		Ω
LO INTERFACE (LOIP, LOIM)						
Differential Common Base Stage						
DC Bias Voltage[2]	Internally Generated; Port Typically AC-Coupled		300	360	450	mV
LO Input Power	50 Ω Impedance	17	–12	–10	–3	dBm
Port Differential Return Loss		16		–10		dB
POWER-DOWN INTERFACE (PWDN)						
PWDN Threshold	Assured ON				$V_S – 1.5$	V
	Assured OFF		$V_S – 0.5$			V
PWDN Response Time[3]	Time from Device ON to OFF	4		2.2		µs
	Time from Device OFF to ON	5		500		ns
PWDN Input Bias Current	PWDN = 0 V (Device ON)			–85	–195	µA
	PWDN = 5 V (Device OFF)			0		µA
POWER SUPPLY						
Supply Voltage Range			4.5	5.0	5.5	V
Total Quiescent Current	R3 and R4 = 68.1 Ω	24		50	60	mA
	Over Temperature				75	mA
Powered-Down Current	V_S = 5.5 V			20	95	µA
	V_S = 4.5 V			6	15	µA
	Over Temperature, V_S = 5.5 V			50	150	µA

NOTES

[1]The balance in the bias current in the two legs of the mixer input may be important in applications were a low feedthrough of the LO is critical.

[2]This voltage is proportional to absolute temperature (PTAT). Reference section on DC-Coupling the LO for more information regarding this interface.

[3]Response time until device meets all specified conditions.

Specifications subject to change without notice.

Table I. Typical AC Performance
(V$_S$ = 5.0 V, T$_A$ = 25°C; See Figure 24 and Tables III Through V.)

Input Frequency (MHz)	Output Frequency (MHz)	Conversion Gain (dB)	SSB Noise Figure (dB)	Input IP3 (dBm)	Input 1 dB Compression Point (dBm)
RECEIVER CHARACTERISTICS					
400	70	5.6	10.5	20.5	3.3
900	170	3.6	11.4	19.4	3.6
1900	170	7.1	14.1	16.5	2.8
2400	170	6.8	15.3	14.5	2.1
2400	425	5.4	16.2	16.5	2.2
TRANSMITTER CHARACTERISTICS					
150	900	7.5	17.9	18.1	1.9
150	1900	0.25	16.0	13.4	0.8

Table II. Typical Isolation Performance
(V$_S$ = 5.0 V, T$_A$ = 25°C; See Figure 24 and Tables III Through V.)

Input Frequency (MHz)	Output Frequency (MHz)	LO to Output Leakage (dBm)	2 × LO to Output Leakage (dBm)	3 × LO to Output Leakage (dBm)	Input to Output Leakage (dBm)
RECEIVER CHARACTERISTICS					
400	70	−40.1	−51.0	−44.0	−62.4
900	170	−44.4	−35.5	< −75.0	−56.9
1900	170	−65.6	−38.3	−73.3	−65.7
2400	170	−66.7	−44.4	< −75.0	−73.7
2400	425	−51.1	−49.4	< −75.0	−52.3
TRANSMITTER CHARACTERISTICS					
150	900	−27.6	< −75 dBm	< −75 dBm	−35.3
150	1900	< −75 dBm	< −75 dBm	< −75 dBm	−69.7

NOTE: Low-side LO injection used for typical performance.
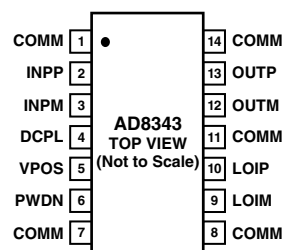
ABSOLUTE MAXIMUM RATINGS[1]
VPOS Quiescent Voltage . . . . 5.5 V
OUTP, OUTM Quiescent Voltage . . . . 5.5 V
INPP, INPM Voltage Differential . . . . 500 mV
Internal Power Dissipation (TSSOP)[2] . . . . 320 mW
θ$_{JA}$ (TSSOP) . . . . 125°C/W
Maximum Junction Temperature . . . . 125°C
Operating Temperature Range . . . . −40°C to +85°C
Storage Temperature Range . . . . −65°C to +150°C
Lead Temperature Range (Soldering 60 sec) . . . . 300°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.
[2]A portion of the device power is dissipated by the external bias resistors R3 and R4.

PIN CONFIGURATION

COMM	1	14	COMM
INPP	2	13	OUTP
INPM	3	12	OUTM
DCPL	4	11	COMM
VPOS	5	10	LOIP
PWDN	6	9	LOIM
COMM	7	8	COMM

AD8343 TOP VIEW (Not to Scale)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8343ARU AD8343ARU-REEL AD8343ARU-REEL7 AD8343-EVAL	−40°C to +85°C	14-Lead Plastic TSSOP	RU-14 13" Tape and Reel 7" Tape and Reel Evaluation Board

AD8343

PIN FUNCTION DESCRIPTIONS

TSSOP	Name	Function	Simplified Interface Schematic
2, 3	INPP/INPM	Differential input pins. Need to be dc-biased; typically ac-coupled.	
12, 13	OUTP/OUTM	Open collector differential output pins. Need to be ac-coupled and dc-biased.	
9, 10	LOIP/LOIM	Differential local oscillator (LO) input pins. Typically ac-coupled.	
6	PWDN	Power-down interface. Connect pin to ground for normal operating mode. Connect pin to supply for power-down mode.	
4	DCPL	Bias rail decoupling capacitor connection for LO Driver.	
5	VPOS	Positive supply voltage (V_S), 4.5 V to 5.5 V. Ensure adequate supply bypassing for proper device operation as shown in Figure 24.	
1, 7, 8, 11, 14	COMM	Connect to low impedance circuit ground.	

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8343 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

WARNING!
ESD SENSITIVE DEVICE

REV. 0

RECEIVER CHARACTERISTICS (f_{IN} = 400 MHz, f_{OUT} = 70 MHz, f_{LO} = 330 MHz [Figure 24, Tables III and IV])
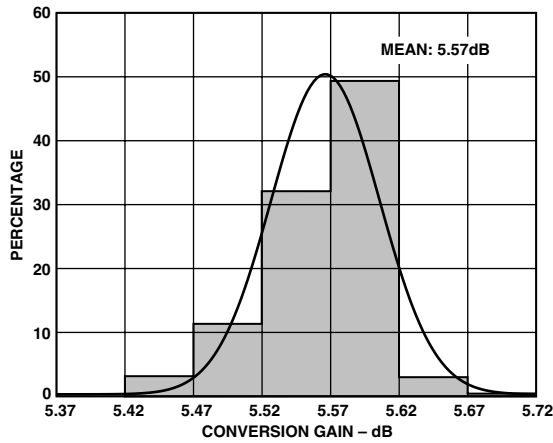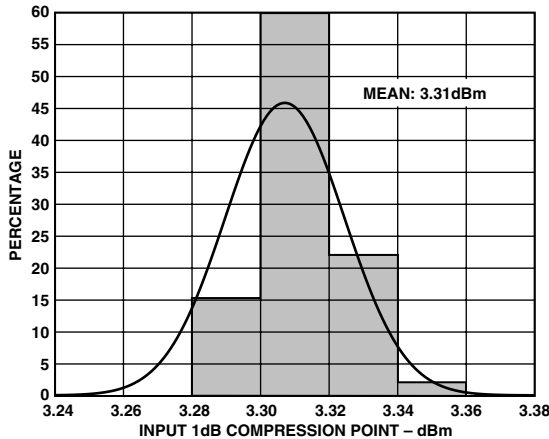

TPC 1. Gain Histogram f_{IN} = 400 MHz, f_{OUT} = 70 MHz
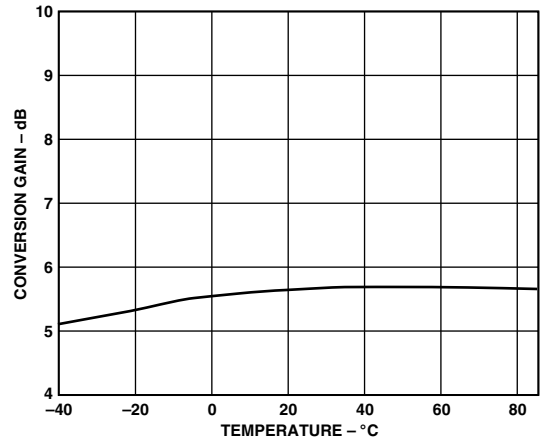
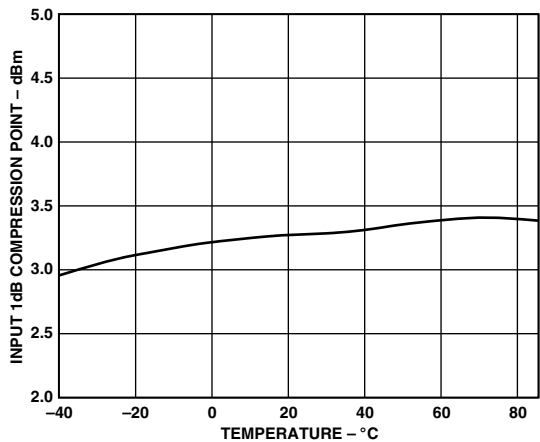TPC 4. Gain Performance Over Temperature f_{IN} = 400 MHz, f_{OUT} = 70 MHz
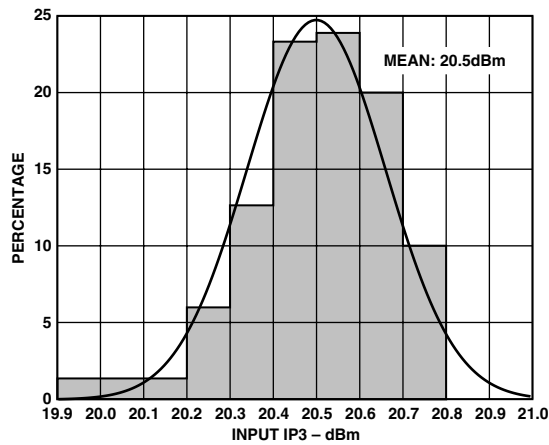
TPC 2. Input IP3 Histogram f_{IN} = 400 MHz, f_{OUT} = 70 MHz
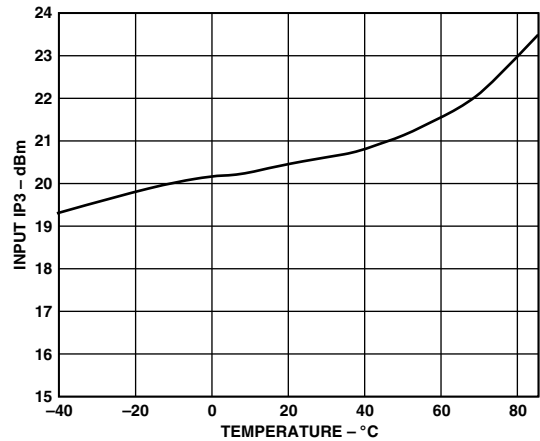
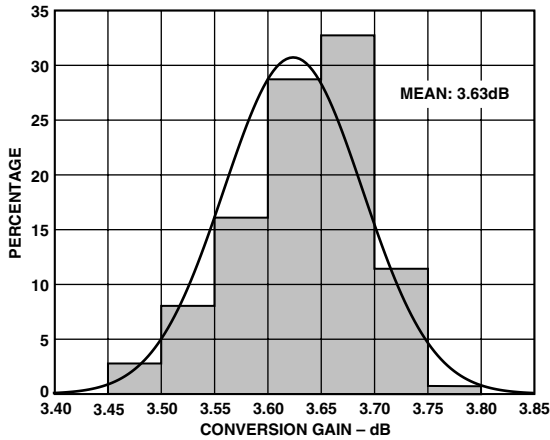TPC 5. Input IP3 Performance Over Temperature f_{IN} = 400 MHz, f_{OUT} = 70 MHz
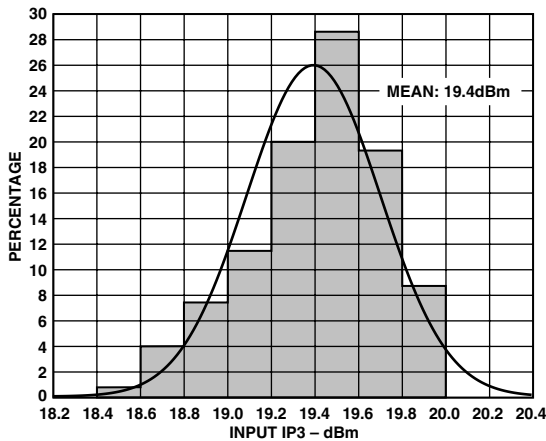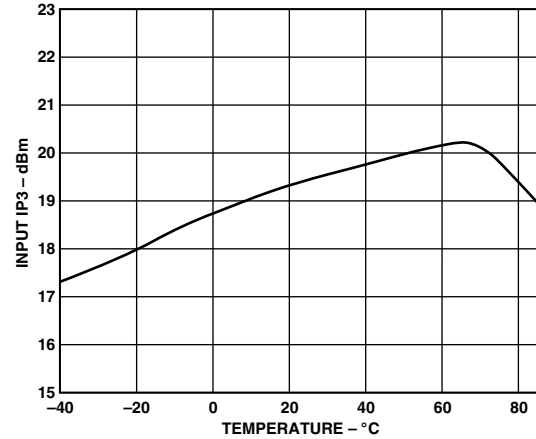

TPC 3. Input 1 dB Compression Point Histogram f_{IN} = 400 MHz, f_{OUT} = 70 MHz

TPC 6. Input 1 dB Compression Point Performance Over Temperature (f_{IN} = 400 MHz, f_{OUT} = 70 MHz)
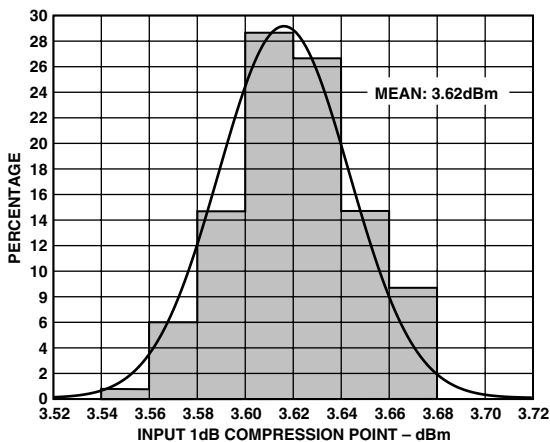
AD8343

TPC 7. Gain Histogram f_{IN} = 900 MHz, f_{OUT} = 170 MHz
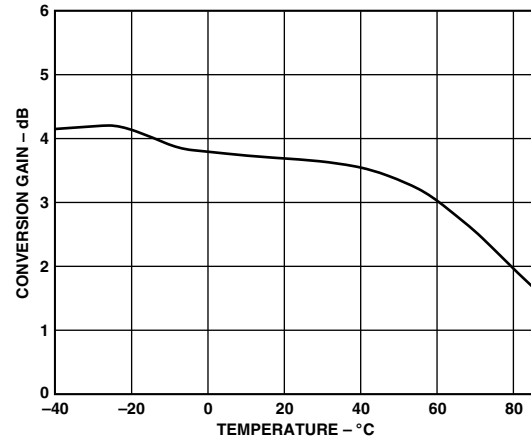
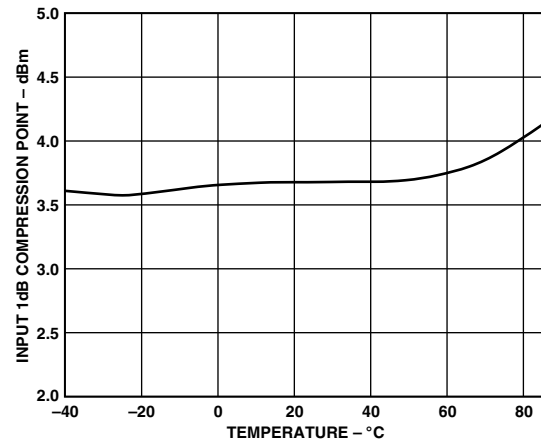TPC 10. Gain Performance Over Temperature
f_{IN} = 900 MHz, f_{OUT} = 170 MHz

TPC 8. Input IP3 Histogram f_{IN} = 900 MHz, f_{OUT} = 170 MHz

TPC 11. Input IP3 Performance Over Temperature
f_{IN} = 900 MHz, f_{OUT} = 170 MHz

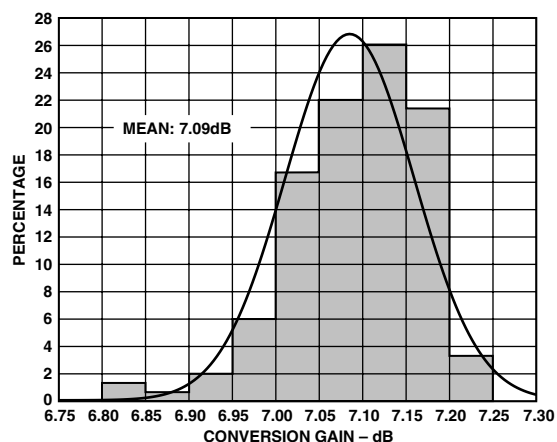TPC 9. Input 1 dB Compression Point Histogram
f_{IN} = 900 MHz, f_{OUT} = 170 MHz
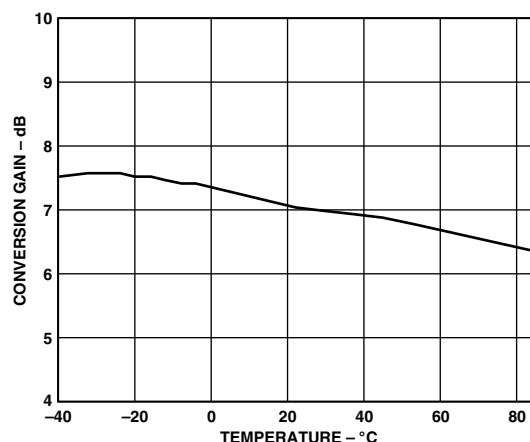

TPC 12. Input 1 dB Compression Point Performance
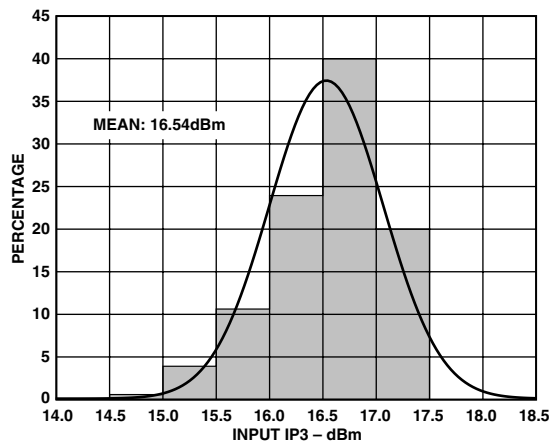Over Temperature f_{IN} = 900 MHz, f_{OUT} = 170 MHz

REV. 0

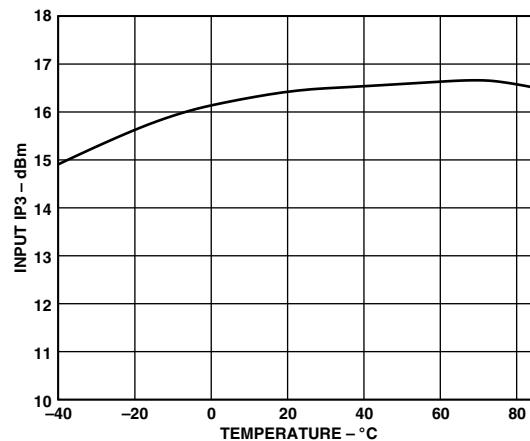**RECEIVER CHARACTERISTICS** (f_{IN} = 1900 MHz, f_{OUT} = 170 MHz, f_{LO} = 1730 MHz [Figure 24, Tables III and IV])

TPC 13. Gain Histogram f_{IN} = 1900 MHz, f_{OUT} = 170 MHz
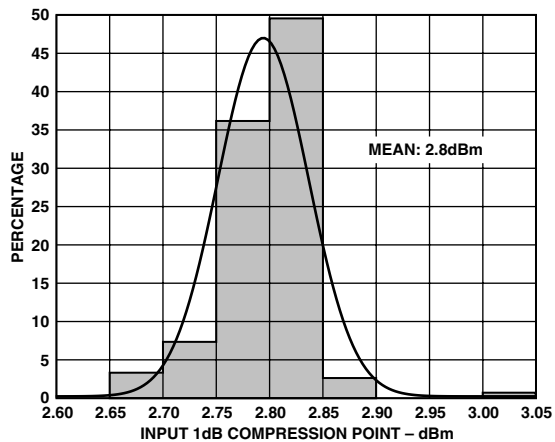

TPC 16. Gain Performance Over Temperature f_{IN} = 1900 MHz, f_{OUT} = 170 MHz
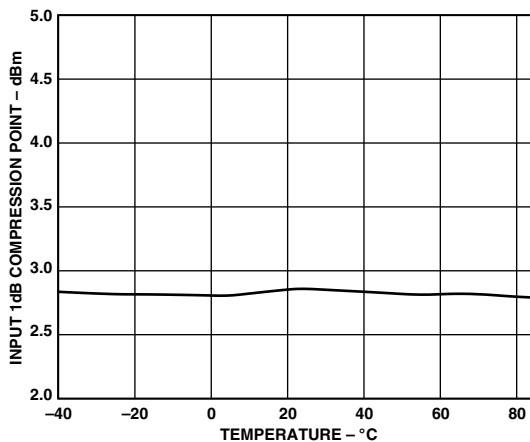

TPC 14. Input IP3 Histogram f_{IN} = 1900 MHz, f_{OUT} = 170 MHz

TPC 17. Input IP3 Performance Over Temperature f_{IN} = 1900 MHz, f_{OUT} = 170 MHz

TPC 15. Input 1 dB Compression Point Histogram f_{IN} = 1900 MHz, f_{OUT} = 170 MHz

TPC 18. Input 1 dB Compression Point Performance Over Temperature f_{IN} = 1900 MHz, f_{OUT} = 170 MHz

AD8343

TPC 19. Gain Histogram f$_{IN}$ = 2400 MHz, f$_{OUT}$ = 170 MHz

TPC 22. Gain Performance Over Temperature
f$_{IN}$ = 2400 MHz, f$_{OUT}$ = 170 MHz
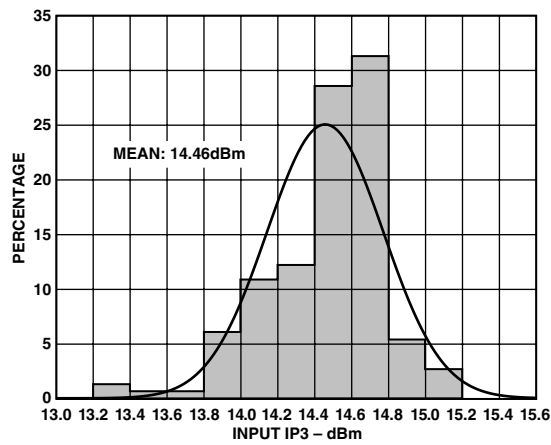
TPC 20. Input IP3 Histogram f$_{IN}$ = 2400 MHz, f$_{OUT}$ = 170 MHz
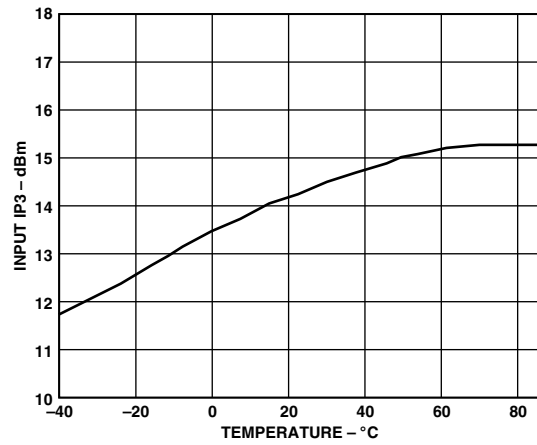
TPC 23. Input IP3 Performance Over Temperature
f$_{IN}$ = 2400 MHz, f$_{OUT}$ = 170 MHz
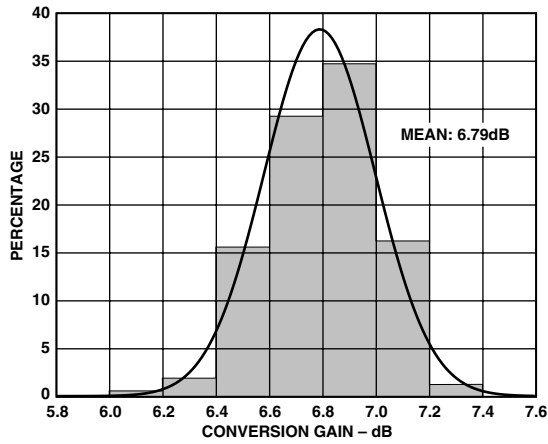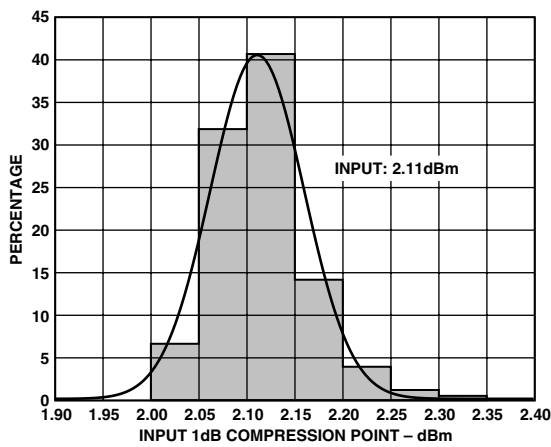
TPC 21. Input 1 dB Compression Point Histogram
f$_{IN}$ = 2400 MHz, f$_{OUT}$ = 170 MHz
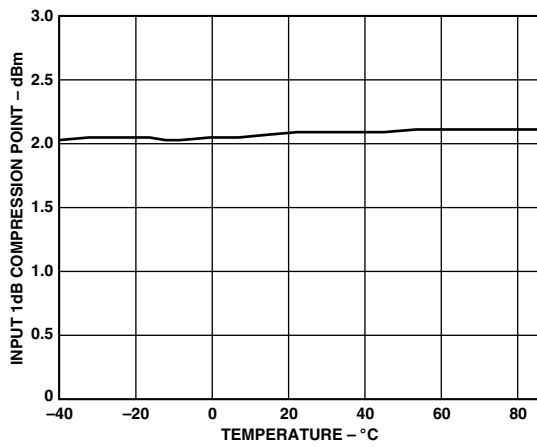
TPC 24. Input 1 dB Compression Point Performance Over
Temperature f$_{IN}$ = 2400 MHz, f$_{OUT}$ = 170 MHz

REV. 0

RECEIVER CHARACTERISTICS (f_{IN} = 2400 MHz, f_{OUT} = 425 MHz, f_{LO} = 1975 MHz [Figure 24, Tables III and IV])

TPC 25. Gain Histogram f_{IN} = 2400 MHz, f_{OUT} = 425 MHz
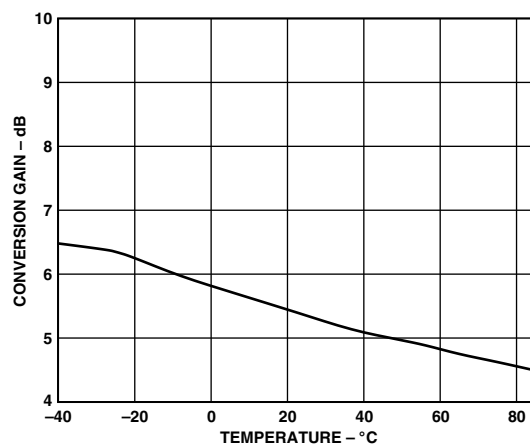
TPC 28. Gain Performance Over Temperature f_{IN} = 2400 MHz, f_{OUT} = 425 MHz
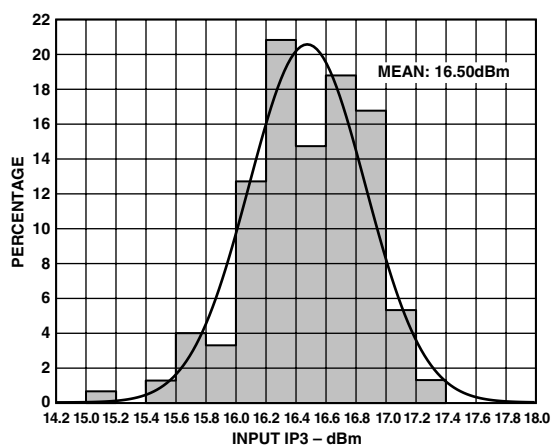
TPC 26. Input IP3 Histogram f_{IN} = 2400 MHz, f_{OUT} = 425 MHz
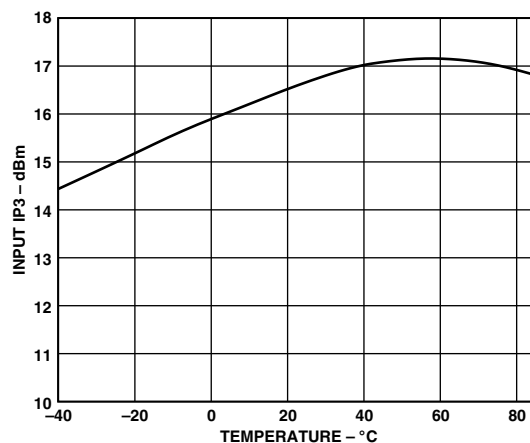
TPC 29. Input IP3 Performance Over Temperature f_{IN} = 2400 MHz, f_{OUT} = 425 MHz
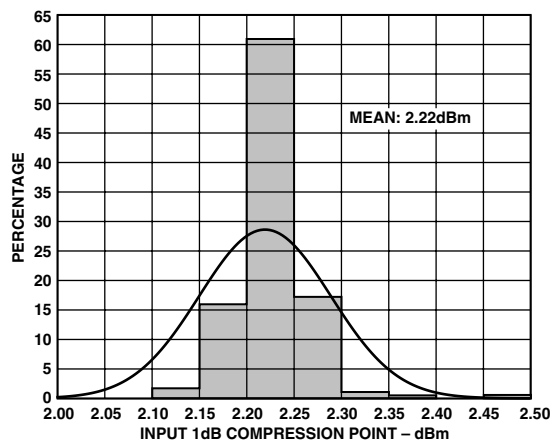
TPC 27. Input 1 dB Compression Point Histogram f_{IN} = 2400 MHz, f_{OUT} = 425 MHz
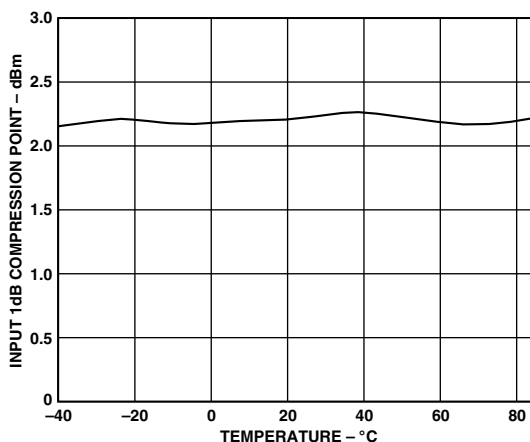
TPC 30. Input 1 dB Compression Point Performance Over Temperature f_{IN} = 2400 MHz, f_{OUT} = 425 MHz

AD8343

TPC 31. Gain Histogram f_{IN} = 150 MHz, f_{OUT} = 900 MHz

TPC 34. Gain Performance Over Temperature
f_{IN} = 150 MHz, f_{OUT} = 900 MHz
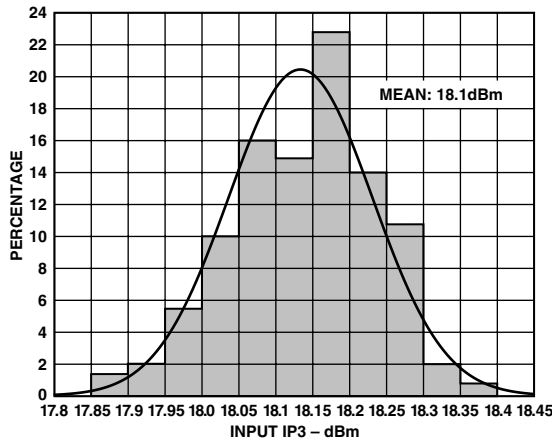
TPC 32. Input IP3 Histogram f_{IN} = 150 MHz, f_{OUT} = 900 MHz
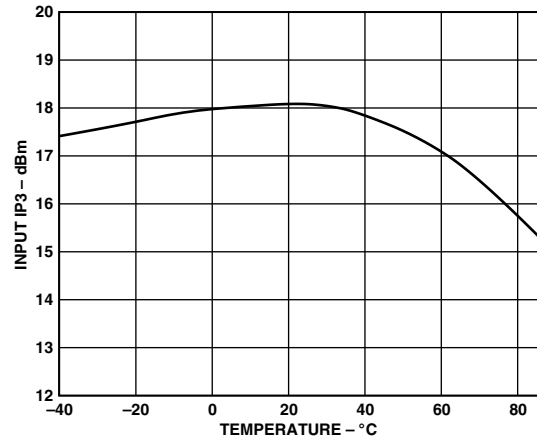
TPC 35. Input IP3 Performance Over Temperature
f_{IN} = 150 MHz, f_{OUT} = 900 MHz
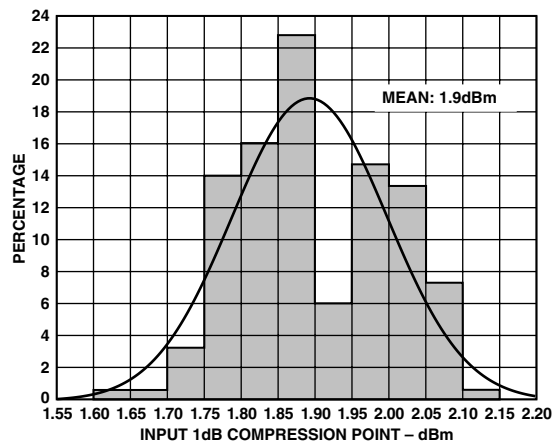
TPC 33. Input 1 dB Compression Point Histogram
f_{IN} = 150 MHz, f_{OUT} = 900 MHz
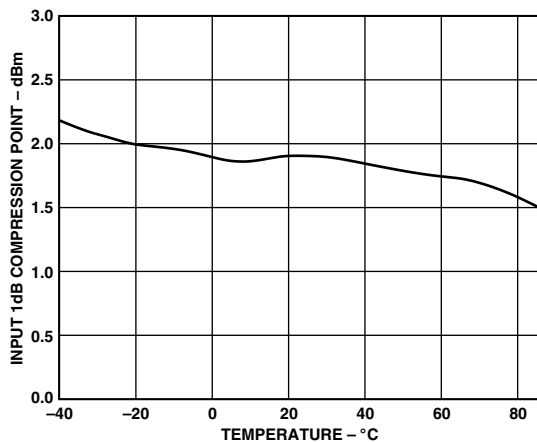
TPC 36. Input 1 dB Compression Point Performance Over
Temperature f_{IN} = 150 MHz, f_{OUT} = 900 MHz

TRANSMIT CHARACTERISTICS (f_{IN} = 150 MHz, f_{OUT} = 1900 MHz, f_{LO} = 1750 MHz [Figure 24, Tables III and IV])
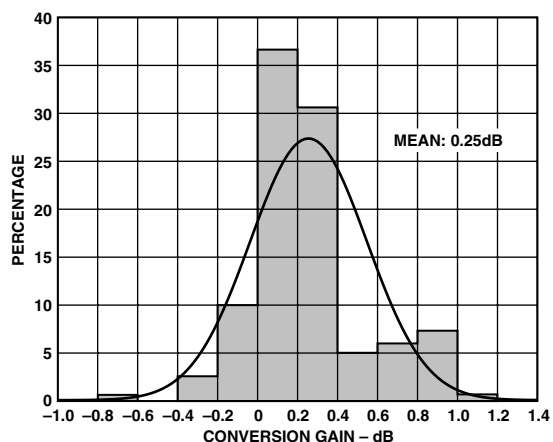
TPC 37. Gain Histogram f_{IN} = 150 MHz, f_{OUT} = 1900 MHz
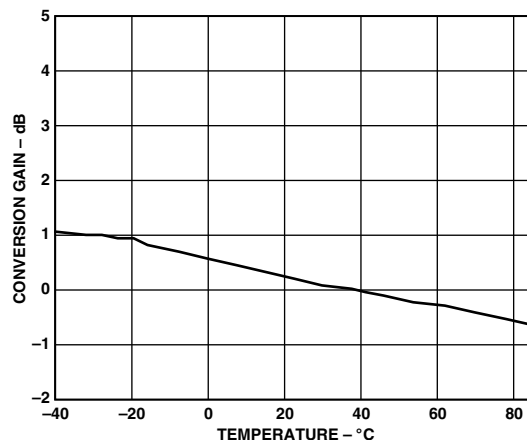
TPC 40. Gain Performance Over Temperature f_{IN} = 150 MHz, f_{OUT} = 1900 MHz

TPC 38. Input IP3 Histogram f_{IN} = 150 MHz, f_{OUT} = 1900 MHz
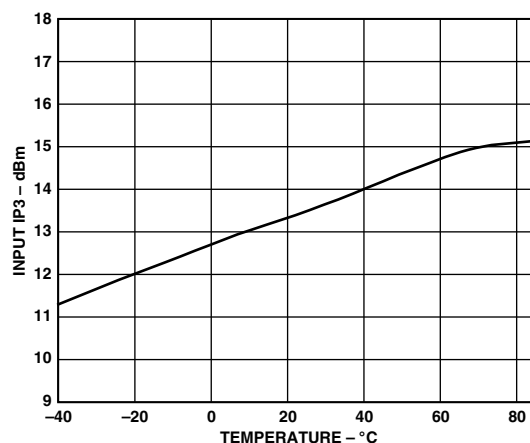
TPC 41. Input IP3 Performance Over Temperature f_{IN} = 150 MHz, f_{OUT} = 1900 MHz
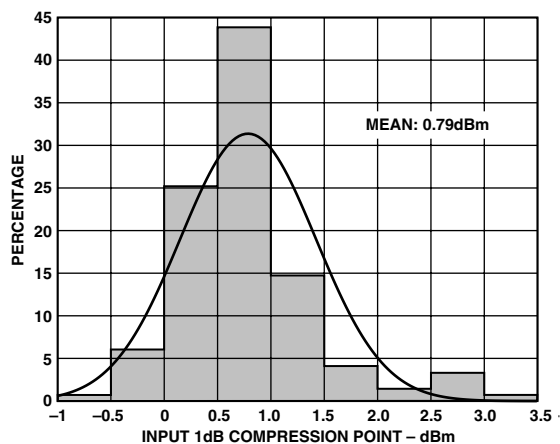
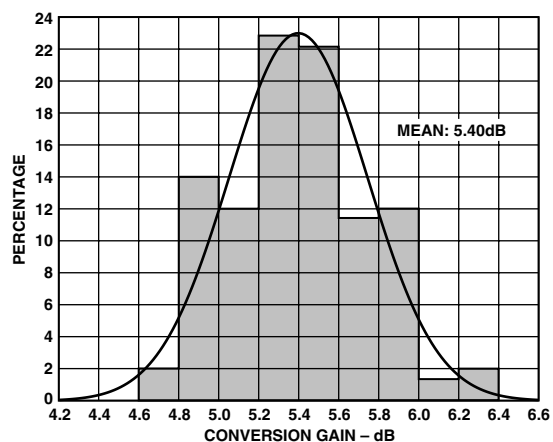

TPC 39. Input 1 dB Compression Point Histogram f_{IN} = 150 MHz, f_{OUT} = 1900 MHz
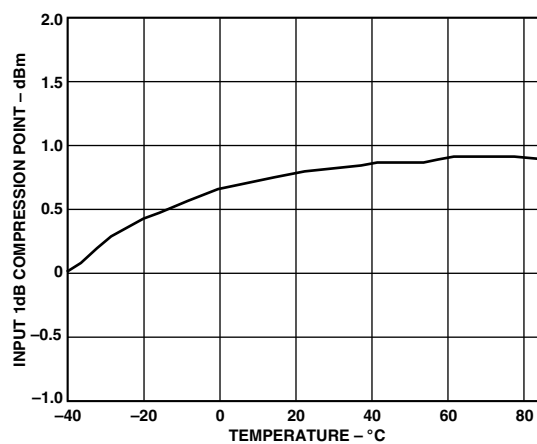
TPC 42. Input 1 dB Compression Point Performance Over Temperature f_{IN} = 150 MHz, f_{OUT} = 1900 MHz

AD8343

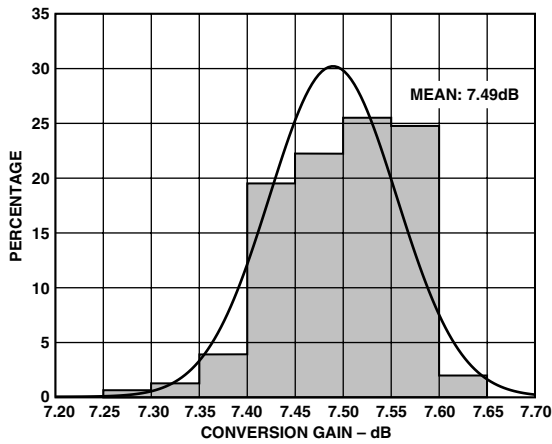## CIRCUIT DESCRIPTION
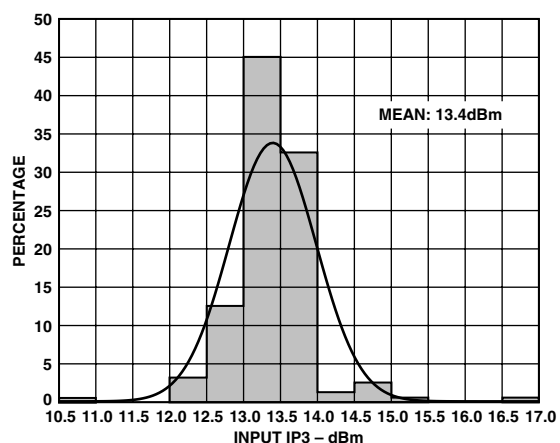
The AD8343 is a mixer intended for high-intercept applications. The signal paths are entirely differential and dc-coupled to permit high-performance operation over a broad range of frequencies; the block diagram (Figure 1) shows the basic functional blocks. The bias cell provides a PTAT (proportional to absolute temperature) bias to the LO Driver and Core. The LO Driver consists of a three-stage limiting differential amplifier that provides a very fast (almost square-wave) drive to the bases of the core transistors.

The AD8343 core utilizes a standard architecture in which the signal inputs are directly applied to the emitters of the transistors in the cell (Figure 7). The bases are driven by the hard-limited LO signal that directs the transistors to steer the input currents into periodically alternating pairs of output terminals, thus providing the periodic polarity reversal that effectively multiplies the signal by a square wave of the LO frequency.
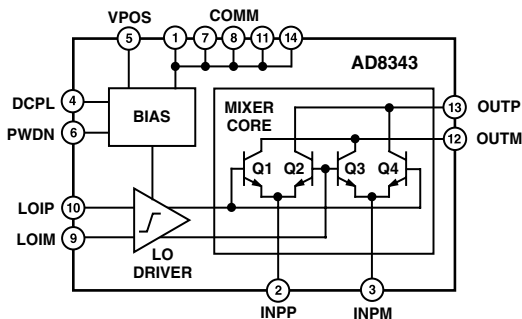
Figure 1. Topology

To illustrate this functionality, when LOIP is positive, Q1 and Q4 are turned ON, and Q2 and Q3 are turned OFF. In this condition Q1 connects I_{INPP} to OUTM and Q4 connects I_{INPM} to OUTP. When LOIP is negative the roles of the transistors reverse, steering I_{INPP} to OUTP and I_{INPM} to OUTM. Isolation and gain are possible because at any instant the signal passes through a common-base transistor amplifier pair.

Multiplication is the essence of frequency mixing; an *ideal* multiplier would make an excellent mixer. The theory is expressed in the following trigonometric identity:

$$sin(\omega_{sig}t)sin(\omega_{LO}t) = 1/2 \ [cos(\omega_{sig}t - \omega_{LO}t) - cos(\omega_{sig}t + \omega_{LO}t)]$$

This states that the product of two sine-wave signals of different frequencies is a pair of sine waves at frequencies equal to the sum and difference of the two frequencies being multiplied.

Unfortunately, practical implementations of analog multipliers generally make poor mixers because of imperfect linearity and because of the added noise that invariably accompanies attempts to improve linearity. The best mixers to date have proven to be those that use the LO signal to periodically reverse the polarity of the input signal.

In this class of mixers, frequency conversion occurs as a result of multiplication of the signal by a square wave at the LO frequency. Because a square wave contains odd harmonics in addition to the fundamental, the signal is effectively multiplied by each frequency component of the LO. The output of the mixer will therefore contain signals at $F_{LO} \pm F_{sig}$, $3 \times F_{LO} \pm F_{sig}$, $5 \times F_{LO} \pm F_{sig}$, $7 \times F_{LO} \pm F_{sig}$, etc. The amplitude of the components arising from signal multiplication by LO harmonics falls off with increasing harmonic order because the amplitude of a square wave's harmonics falls off.

An example of this process is illustrated in Figure 2. The first pane of this figure shows an 800 MHz sinusoid intended to represent an input signal. The second pane contains a square wave representing an LO signal at 600 MHz which has been hard-limited by the internal LO driver. The third pane shows the time domain representation of the output waveform and the fourth pane shows the frequency domain representation. The two strongest lines in the spectrum are the sum and difference frequencies arising from multiplication of the signal by the LO's fundamental frequency. The weaker spectral lines are the result of the multiplication of the signal by various harmonics of the LO square wave.
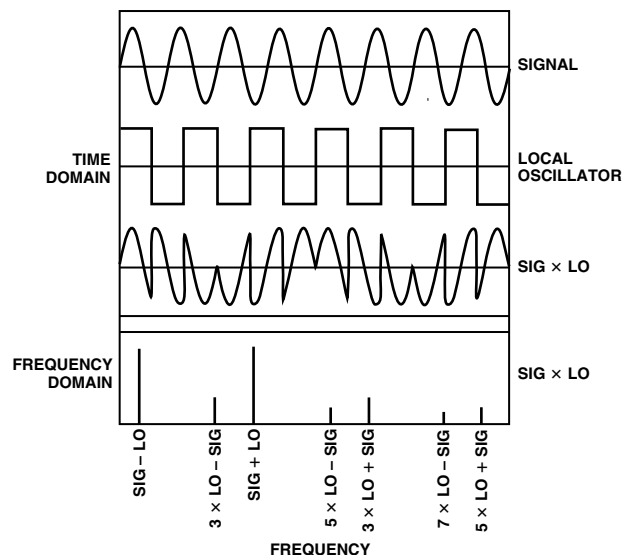
Figure 2. Signal Switching Characteristics of the AD8343

DC INTERFACES

Biasing and Decoupling (VPOS, DCPL)

VPOS is the power supply connection for the internal bias cir-
cuit and the LO driver. This pin should be closely bypassed to
GND with a capacitor in the range of 0.01 μF to 0.1 μF. The
DCPL pin provides access to an internal bias node for noise
bypassing purposes. This node should be bypassed to COMM
with 0.1 μF.

Power-Down Interface (PWDN)

The AD8343 is active when the PWDN pin is held low; other-
wise the device enters a low-power state as shown in Figure 3.
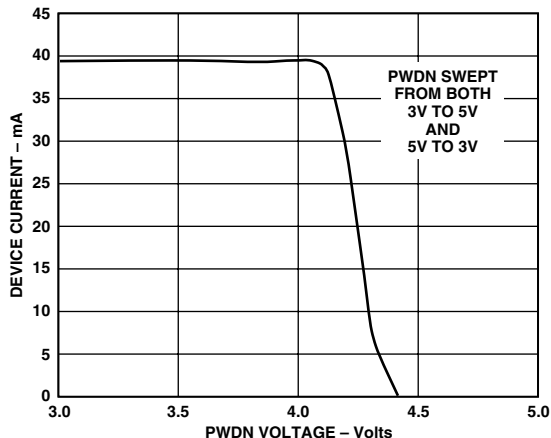
Figure 3. Bias Current vs. PWDN Voltage

To assure full power-down, the PWDN voltage should be within
0.5 V of the supply voltage at VPOS. Normal operation requires
that the PWDN pin be taken at least 1.5 V below the supply
voltage. The PWDN pin sources about 100 μA when pulled to
GND (refer to Pin Function Descriptions). It is not advisable to
leave the pin floating when the device is to be disabled; a resis-
tive pull-up to VPOS is the minimum suggestion.

The AD8343 requires about 2.5 μs to turn OFF when PWDN is
asserted; turn ON time is about 500 ns. Figures 4 and 5 show
typical characteristics (they will vary with bypass component
values). Figure 6 shows the test configuration used to acquire
these waveforms.
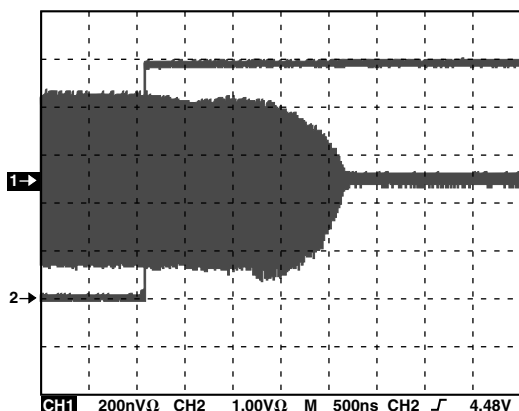
Figure 4. PWDN Response Time Device ON to OFF
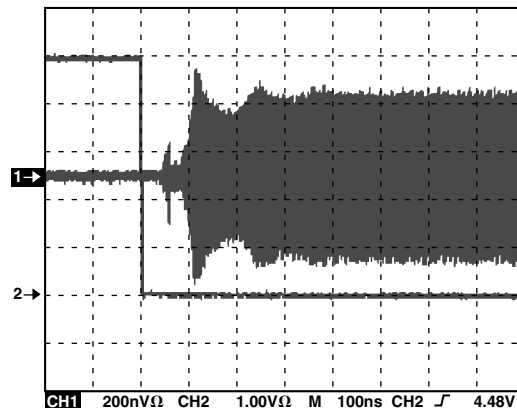
Figure 5. PWDN Response Time Device OFF to ON
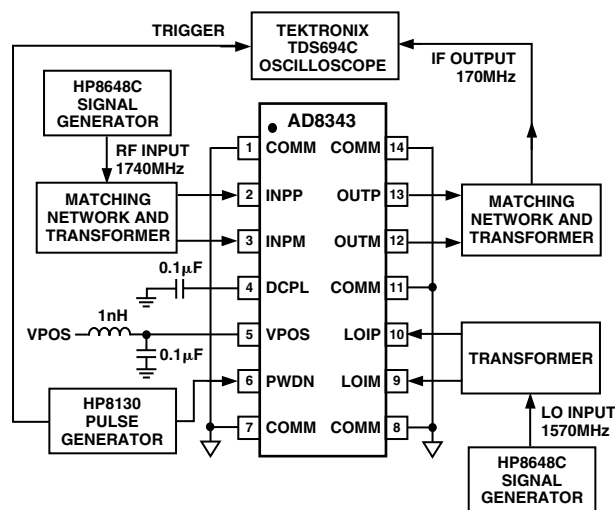
Figure 6. PWDN Response Time Test Schematic

AC INTERFACES

Because of the AD8343's wideband design, there are several
points to consider in its ac implementation; the Basic AC
Signal Connection diagram shown in Figure 7 summarizes
these points. The input signal undergoes a single-ended-to-
differential conversion and is then reactively matched to the
impedance presented by the emitters of the core. The matching
network also provides bias currents to these emitters. Similarly,
the LO input undergoes a single-ended-to-differential transfor-
mation before it is applied to the 50 Ω differential LO port. The
differential output signal currents appear at high-impedance
collectors and may be reactively matched and converted to a
single-ended signal.
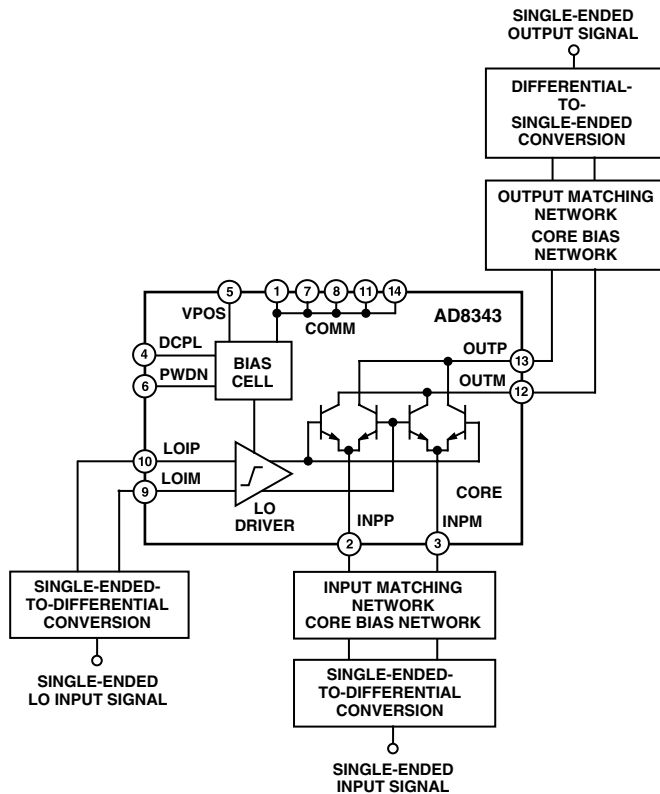
AD8343

Figure 7. Basic AC Signal Connection Diagram

INPUT INTERFACE (INPP AND INPM)
Single-Ended-to-Differential Conversion

The AD8343 is designed to accept differential input signals for best performance. While a single-ended input can be applied, the signal capacity is reduced by 6 dB. Further, there would be no cancellation of even-order distortion arising from the nonlinear input impedances, so the effective signal handling capacity will be reduced even further in distortion-sensitive situations. That is, the intermodulation intercepts are degraded.

For these reasons it is strongly recommended that differential signals be presented to the AD8343's input. In addition to commercially available baluns, there are various discrete and printed circuit elements that can produce the required balanced waveforms and impedance match (i.e., rat-race baluns). These alternate circuits can be employed to further reduce the component cost of the mixer.

Baluns implemented in transmission line form (also known as common-mode chokes) are useful up to frequencies of around 1 GHz, but are often excessively lossy at the highest frequencies that the AD8343 can handle. M/A-Com manufactures these baluns with their ETC line. Murata produces a true surface-mount balun with their LDB20C series. Coilcraft and Toko are also manufacturers of RF baluns.

Input Matching Considerations

The design of the input matching network should be undertaken with two goals in mind: matching the source impedance to the input impedance of the AD8343 and providing a dc bias current path for the bias setting resistors.

The maximum power transfer into the device will occur when there is a conjugate impedance match between the signal source and the input of the AD8343. This match can be achieved with the differential equivalent of the classic "L" network, as illustrated in Figure 8. The figure gives two examples of the transformation from a single-ended "L" network to its differential counterpart. The design of "L" matching networks is adequately covered in texts on RF amplifier design (for example: "Microwave Transistor Amplifiers" by Guillermo Gonzalez).
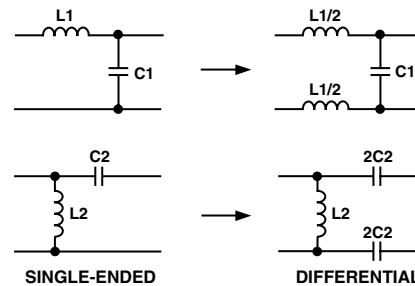
Figure 8. Single-Ended-to-Differential Transformation

Figure 9 shows the differential input impedance of the AD8343 at the pins of the device. The two measurements shown in the figure are for two different core currents set by resistors R3 and R4; the real value impedance shift is caused by the change in transistor r_E due to the change in current. The standard S parameter files are available at the ADI web site (www.analog.com).
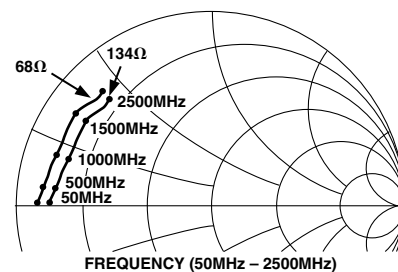
Figure 9. Input Differential Impedance (INPP, INPM) for Two Values of R3 and R4

Figure 9 provides a reasonable starting point for the design of the network. However, the particular board traces and pads will transform the input impedance at frequencies in excess of about 500 MHz. For this reason it is best to make a *differential* input impedance measurement at the board location where the matching network will be installed, as a starting point for designing an accurate matching network.

Differential impedance measurement is made relatively easy through the use of a technique presented in an article by Lutz Konstroffer in *RF Design*, January 1999, entitled "Finding the Reflection Coefficient of a Differential One-Port Device." This article presents a mathematical formula for converting from a two-port single-ended measurement to differential impedance. A full two-port measurement is performed using a vector network analyzer with Port 1 and Port 2 connected to the two differential inputs of the device at the desired measurement plane. The two-port measurement results are then processed with Konstroffer's formula (following), which is straightforward and can be implemented through most RF design packages that can read and analyze network analyzer data.

$$\Gamma_S = \frac{(2 \times S11 - S21)(1 - S22 - S12) + (1 - S11 - S21)(1 + S22 - 2 \times S12)}{(2 - S21)(1 - S22 - S12) + (1 - S11 - S21)(1 + S22)}$$

This measurement can also be made using the ATN 4000 Series Multiport Network Analyzer. This instrument, and accompanying software, is capable of directly producing differential measurements.

At low frequencies and I_O = 16 mA, the differential input impedance seen at ports INPP and INPM of the AD8343 is low (~5 Ω in series with parasitic inductances that total about 3 nH). Because of this low value of impedance, it may be beneficial to choose a transformer-type balun that can also perform all or part of the real value impedance transformation. The turns ratio of the transformer will remove some of the matching burden from the differential "L" network and potentially lead to wider bandwidth.

At frequencies above 1 GHz, the real part of the input impedance rises markedly and it becomes more attractive to use a 1:1 balun and rely on the "L" network for the entire impedance transformation.

In order to obtain the lowest distortion, the inputs of the AD8343 should be driven through external ballast resistors. At low frequencies (up to perhaps 200 MHz) about 5 Ω per side is appropriate; above about 400 MHz, 10 Ω per side is better. The specified RF performance values for the AD8343 apply with these ballast resistors in use. These resistors improve linearity because their linear ac voltage drop partially swamps the nonlinear voltage swing occurring on the emitters.

In cases where the use of a lossy balun is unavoidable, it may be worthwhile to perform simultaneous matching on both the input and output sides of the balun. The idea is to independently characterize the balun as a two-port device and then arrange a simultaneous conjugate match for it. Unfortunately there seems to be no good way to determine the benefit this approach may offer in any particular case; it remains necessary to characterize the balun and then design and simulate appropriate matching networks to make an optimal decision. One indication that such effort may be worthwhile is the discovery that the adjustment of a post-balun-only matching network for best gain, differs appreciably from that which produces best return loss at the balun's input. A better tactic may be to try a different approach for the balun, either purchasing a different balun or designing a discrete network.

For more information on performing the input match, see "A Step-by-Step Approach to Impedance Matching" in the section covering the AD8343 evaluation board.

Input Biasing Considerations
The mixer core bias current of the AD8343 is adjustable from less than 5 mA to a safe maximum of 20 mA. It is important to note that the reliability of the AD8343 will be compromised for core currents set to higher than 20 mA. The AD8343 is tested to ensure that a value of 68.1 Ω ± 1% will ensure safe operation.

Higher operating currents will reduce distortion and affect gain, noise figure, and input impedance (Figures 10 and 11). As the quiescent current is increased by a factor of N the real part of the input impedance decreases by N. Assuming that a match is maintained, the signal current increases by $\sqrt{N}$, but the signal

voltage *decreases* by $\sqrt{N}$, which exercises a smaller portion of the nonlinear V–I characteristic of the common base connected mixer core transistors and results in lower distortion.
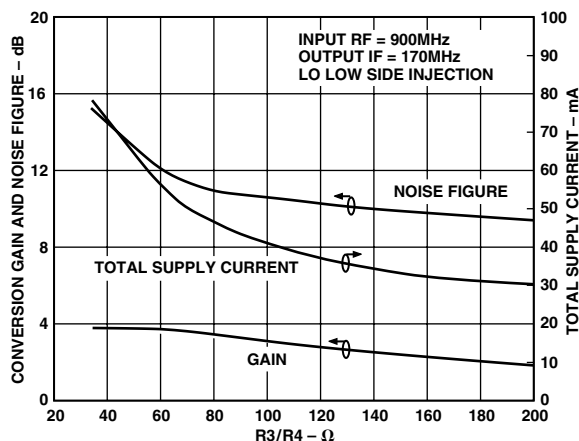
Figure 10. Effect of R3/R4 Value on Gain and Noise Figure
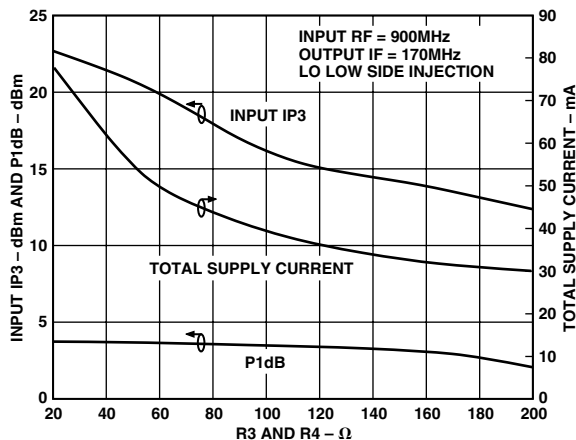
Figure 11. Effect of R3/R4 Value on Input IP3 and Gain Compression

At low frequencies where the magnitude of the complex input impedance is much smaller than the bias resistor values, adequate biasing can be achieved simply by connecting a resistor from each input to GND. The input terminals are internally biased at 1.2 V dc (nominal), so each resistor should have a resistance value calculated as $R_{BIAS} = 1.2/I_{BIAS}$. The resistor values should be well matched in order to maintain full LO to output isolation; 1% tolerance resistors are recommended.

At higher frequencies where the input impedance of the AD8343 rises, it is beneficial to insert an inductor in series between each bias resistor and the corresponding input pin in order to minimize signal shunting (Figure 24). Practical considerations will limit the inductive reactance to a few hundred ohms. The best overall choice of inductor will be that value which places the self-resonant frequency at about the upper end of the desired input frequency range. Note that there is an RF stability concern that argues in favor of erring on the side of too small an inductor value; reference section on Input and Output Stability Considerations. The Murata LQW1608A series of inductors (0603 SMT package) offers values up to 56 nH before the self-resonant frequency falls below 2.4 GHz.

AD8343

For optimal LO-to-Output isolation it is important not to connect the dc nodes of the emitter bias inductors together in an attempt to share a single bias resistor. Doing so will cause isolation degradation arising from V_{BE} mismatches of the transistors in the core.

OUTPUT INTERFACE (OUTP, OUTM)
The output of the AD8343 comprises a balanced pair of open-collector outputs. These should be biased to about the same voltage as is connected to VPOS (see dc specifications table). Connecting them to an appreciably higher voltage is likely to result in conduction of the ESD protection network on signal peaks, which would cause high distortion levels. On the other hand, setting the dc level of the outputs too low is also likely to result in poor device linearity due to collector-base capacitance modulation or saturation of the core transistors.

Output Matching Considerations
The AD8343 requires a differential load for much the same reasons that the input needs a differential source to achieve optimal device performance. In addition, a differential load will provide the best LO to output isolation and the best input to output isolation.

At low output frequencies it is usually not appropriate to arrange a conjugate match between the device output and the load, even though doing so would maximize the small signal conversion gain. This is because the output impedance at low frequencies is quite high (a high resistance in parallel with a small capacitance). Refer to Figure 12 for a plot of the *differential* output impedance measured at the device pins. This data is available in standard file format at the ADI web site (www.analog.com).

If a matching high impedance load is used, sufficient output voltage swing will occur to cause output clipping even at relatively low input levels, which constitutes a loss of dynamic range. The linear range of voltage swing at each output pin is about ±1 volt from the supply voltage VPOS. A good compromise is to provide a load impedance of about 500 Ω between the output pins at the desired output frequency (based on 15 mA to 20 mA bias current at each input). At output frequencies below 500 MHz, more output power can be obtained before the onset of gross clipping by using a lower load impedance; however, both gain and low order distortion performance will be degraded.
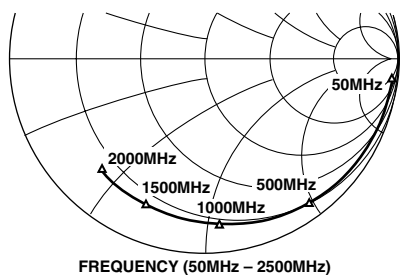

Figure 12. Output Differential Impedance (OUTP, OUTM)

The output load impedance should also be kept reasonably low at the image frequency to avoid developing appreciable extra voltage swing, which would again reduce dynamic range.

If maintaining a good output return loss is not required, a 10:1 (impedance) flux-coupled transformer may be used to present a suitable load to the device and to provide collector bias via a center tap as shown in Figure 21. At all but the lowest output frequencies it becomes desirable to tune out the output capacitance of the AD8343 by connecting an inductor between the output pins.

On the other hand, when a good output return loss is desired, the output may be resistively loaded with a shunt resistance between the output pins in order to set the real value of output impedance. With selection of both the transformer's impedance ratio and the shunting resistance as required, the desired total load (~500 Ω) will be achieved while optimizing both signal transfer and output return loss.

At higher output frequencies the output *conductance* of the device becomes higher (Figure 12), with the consequence that above about 900 MHz it *does* become appropriate to perform a conjugate match between the load and the AD8343's output. The device's own output admittance becomes sufficient to remove the threat of clipping from excessive voltage swing. Just as for the input, it may become necessary to perform differential output impedance measurements on your board layout to effectively develop a good matching network.

Output Biasing Considerations
When the output single-ended-to-differential conversion takes the form of a transformer whose primary winding is center-tapped, simply apply VPOS to the tap, preferably through a ferrite bead in series with the tap in order to avoid a common-mode instability problem (reference section on Input and Output Stability Considerations). Refer to Figure 21 for an example of this network. The collector dc bias voltage should be nominally equal to the supply voltage applied to Pin 5 (VPOS).

If a 1:1 transmission line balun is used for the output, it will be necessary to bring in collector bias through separate inductors. These inductors should be chosen to obtain a high impedance at the RF frequency, while maintaining a suitable self-resonant frequency. Refer to Figure 22 for an example of this network.

INPUT AND OUTPUT STABILITY CONSIDERATIONS
The differential configuration of the input and output ports of the AD8343 raises the need to consider both differential and common-mode RF stability of the device. Throughout the following stability discussion, common mode will be used to refer to a signal that is referenced to ground. The equivalent common-mode impedance will be the value of impedance seen from the node under discussion to ground. The book "Microwave Transistor Amplifiers" by Guillermo Gonzalez also has an excellent section covering stability of amplifiers.

The AD8343 is unconditionally stable for any differential impedance, so device stability need not be considered with respect to the *differential* terminations. However, the device is potentially unstable (k factor is less than one) for some common-mode impedances. Figures 13 and 14 plot the input and output common-mode stability regions, respectively. Figure 15 shows the test equipment configuration to measure these stability circles.

The plotted stability circles in Figure 14 indicate that the guiding principle for preventing stability problems due to common-mode output loading is to avoid high-Q common-mode inductive loading. This stability concern is of particular importance when the output is taken from the device with a center-tapped transformer. The common-mode inductance to the center tap, which arises from imperfect coupling between the halves of the primary winding, produces an unstable common-mode loading condition. Fortunately, there is a simple solution: insert a ferrite bead in series with the center tap, then provide effective RF bypassing on the power supply side of the bead. The bead should develop substantial impedance (tens of ohms) by the time a frequency of about 200 MHz is reached. The Murata BLM21P300S is a possible choice for many applications.

FREQUENCY: 50MHz TO 2500MHz   INCREMENT: 100MHz
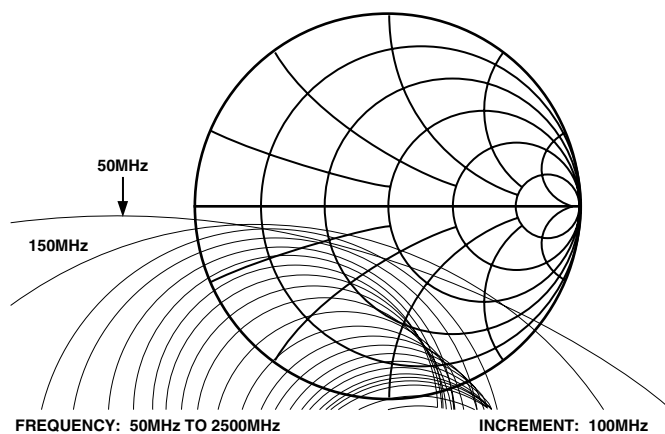
Figure 13. Common-Mode Input Stability Circles

FREQUENCY: 50MHz TO 2500MHz   INCREMENT: 100MHz
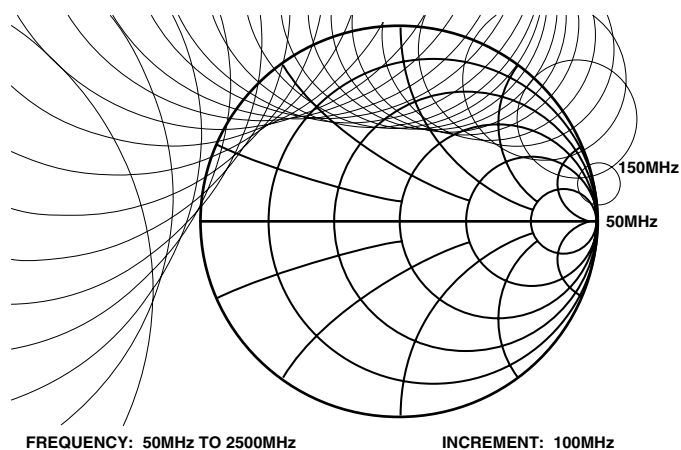
Figure 14. Common-Mode Output Stability Circles
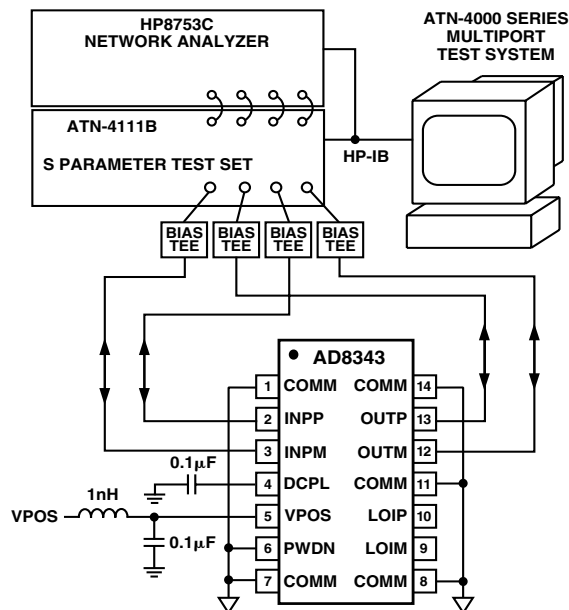
Figure 15. Impedance and Stability Circle Test Schematic

In cases where a transmission line balun is used at the output, the solution needs more exploration. After the differential impedance matching network is designed, it is possible to measure or simulate the common-mode impedance seen by the device. This impedance should be plotted against the stability circles to ensure stable operation. An alternate topology for the matching network may be required if the proposed network produces an unacceptable common-mode impedance.

For the device input, capacitive common-mode loading produces an unstable circuit, particularly at low frequencies (Figure 13). Fortunately, either type of single-ended-to-differential conversion (transmission line balun or flux-coupled transformer) tends to produce inductive loading, although some matching network topologies and/or component values could circumvent this desirable behavior. In general, a simulation of the common-mode termination seen by the AD8343's input port should be plotted against the input stability circles to check stability. This is especially recommended if the single-ended-to-differential conversion is done with a discrete component circuit.

LO Input Interface (LOIP, LOIM)
The LO terminals of the AD8343 are internally biased; connections to these terminals should include dc blocks, except as noted below in the DC Coupling the LO section.

The differential LO input return loss (re 50 Ω is presented in Figure 16. As shown, this port has a typical differential return loss of better than 9.5 dB (2:1 VSWR). If better return loss is desired for this port, differential matching techniques can also be applied.

AD8343
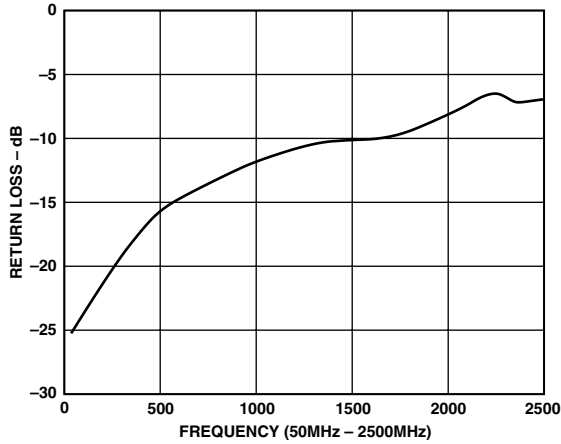
Figure 16. LO Input Differential Return Loss

At low LO frequencies, it is reasonable to drive the AD8343 with a single-ended LO, connecting the undriven terminal to GND through a dc block. This will result in an input impedance closer to 25 Ω at low frequencies, which should be factored into the design. At higher LO frequencies, differential drive is recommended.

The suggested minimum LO power level is about –12 dBm. This can be seen in Figure 17.

Figure 17. Gain and Noise Figure vs. LO Input Power

DC Coupling the LO
The AD8343's LO limiting amplifier chain is internally dc-coupled. In some applications or experimental situations it is useful to exploit this property. This section addresses some ways in which to do it.

The LO pins are internally biased at about 360 mV with respect to COMM. Driving the LO to either extreme requires injecting several hundred microamps into one LO pin and 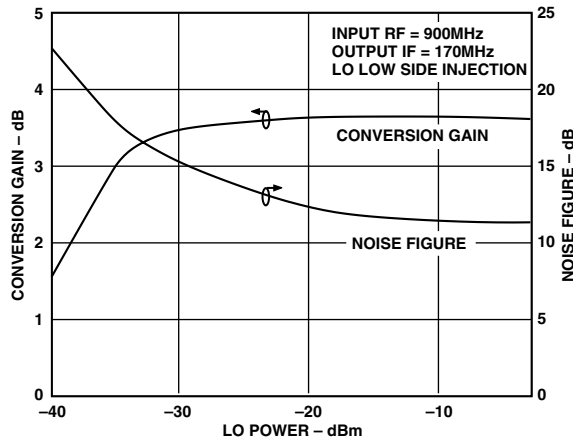extracting about the same amount of current from the other. The incremental impedance at each pin is about 25 Ω, so the voltage level on each pin is disturbed very little by the application of external currents in that range.

Figure 18 illustrates how to drive the LO port with continuous dc and also from standard ECL powered by –5.2 V.
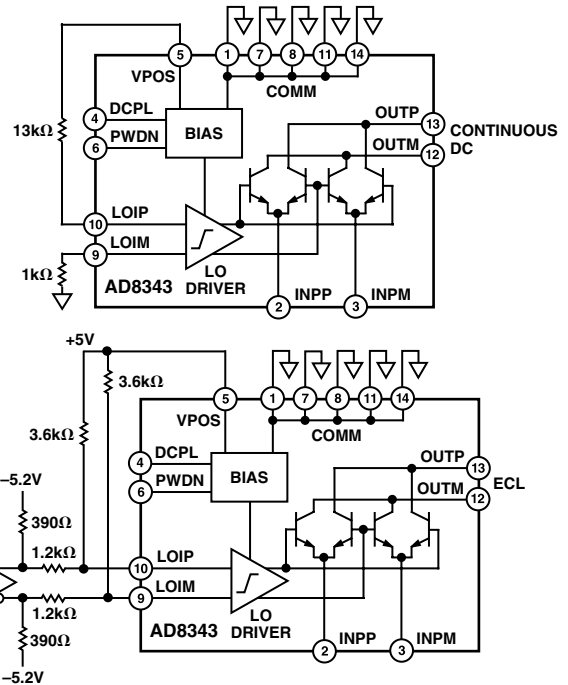
Figure 18. DC Interface to LO Port

A Step-by-Step Approach to Impedance Matching
The following discussion addresses, in detail, the matter of establishing a differential impedance match to the AD8343. This section will specifically deal with the input match, and using side "A" of the evaluation board (Figure 23). An analogous procedure would be used to establish a match to the output if desired.

Step 1: Circuit Setup
In order to do this work the AD8343 must be powered up, driven with LO; its outputs should be terminated in a manner that avoids the common-mode stability problem as discussed in the Input and Output Stability section. A convenient way to deal with the output termination is to place ferrite chokes at L3A and L4A and omit the output matching components altogether.

It is also important to establish the means of providing bias currents to the input pins because this network may have unexpected loading effects and inhibit matching progress.

Step 2: Establish Target Impedance
This step is necessary when the single-ended-to-differential network (input balun) does not produce a 50 Ω output impedance. In order to provide for maximum power transfer, the input impedance of the matching network, loaded with the AD8343 input impedance (including ballast resistors), should be the conjugate of the output impedance of the single-ended-to-differential network. This step is of particular importance when utilizing transmission line baluns because the differential output impedance of the input balun may differ significantly from what is expected. Therefore, it is a good idea to make a separate measurement of this impedance at the desired operating frequency before proceeding with the matching of the AD8343.

The idea is to make a differential measurement at the output of the balun, with the single-ended port of the balun terminated in 50 Ω. Again, there are two methods available for making this measurement: use of the ATN Multiport Network Analyzer to measure the differential impedance directly, or use of a standard two-port network analyzer and Konstroffer's transformation equation.

In order to utilize a standard two-port analyzer, connect the two ports of the calibrated vector network analyzer (VNA) to the balanced output pins of the balun, measure the two-port S parameters, then use Konstroffer's formula to convert the two-port parameters to one-port differential Γ.

$$\Gamma_S = \frac{(2 \times S11 - S21)(1 - S22 - S12) + (1 - S11 - S21)(1 + S22 - 2 \times S12)}{(2 - S21)(1 - S22 - S12) + (1 - S11 - S21)(1 + S22)}$$

Step 3: Measure AD8343 Differential Impedance at Location of First Matching Component
Once the target impedance is established, the next step in matching to the AD8343 is to measure the differential impedance at the location of the first matching component. The "A" side of the evaluation board is designed to facilitate doing so.

Before doing the board measurements, it is necessary to perform a full two-port calibration of the VNA at the ends of the cables that will be used to connect to the board's input connectors, using the SOLT (Short, Open, Load, Thru) method or equivalent. It is a good idea to set the VNA's sweep span to a few hundred MHz or more for this work because it is often useful to see what the circuit is doing over a large range of frequencies, not just at the intended operating frequency. This is particularly useful for detecting stability problems.

After the calibration is completed, connect network analyzer ports one and two to the differential inputs of the AD8343 Evaluation Board.

On the AD8343 Evaluation Board, it is necessary to temporarily install jumpers at Z1A and Z3A if Z4A is the desired component location. Zero ohm resistors or capacitors of sufficient value to exhibit negligible reactance work nicely for this purpose.

Next, extend the reference plane to the location of your first matching component. This is accomplished by solidly shorting both pads at the component location to GND (*Note: Power to the board must be OFF for this operation!*) Adjust the VNA reference plane extensions to make the entire trace collapse to a point (or best approximation thereof near the desired frequency) at the zero impedance point of the Smith Chart. Do this for each port. A reasonable way to provide a good RF short is to solder a piece of thin copper or brass sheet on edge across the pads to the nearby GND pads.

Now, remove the short, apply power to the board, and take readings. Take a look at both S11 and S22 to verify that they remain inside the unit circle of the Smith Chart over the whole frequency range being swept. If they fail to do so, this is a sign that the device is unstable (perhaps due to an inappropriate common-mode load) or that the network analyzer calibration is wrong. Either way the problem must be addressed before proceeding further.

Assuming that the values look reasonable, use Konstroffer's formula to convert to differential Γ.

Step 4: Design the Matching Network
The next step is to perform a trial design of a matching network utilizing standard impedance matching techniques. The network may be designed using single-ended network values, then converted to differential form as illustrated in Figure 8. Figure 19 shows a theoretical design of a series C/shunt C "L" network applied between 50 Ω and a typical load at 1.8 GHz.
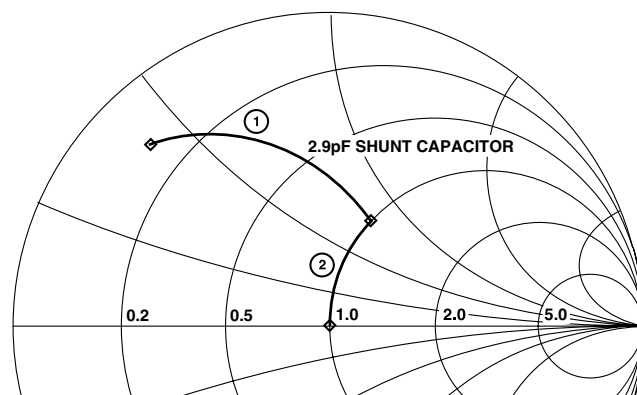
Figure 19. Theoretical Design of Matching Network

This theoretical design is important because it establishes the basic topology and the initial matching value for the network. The theoretical value of 2.9 pF for the initial matching component is not available in standard capacitor values, so a 3.0 pF is placed in the first shunt matching location. This value may prove to be too large, causing an overshoot of the 50 Ω real impedance circle, or too small, causing the opposite effect. Always keep in mind that this is a measure of *differential* impedance. The value of the capacitor should be modified to achieve the desired 50 Ω real impedance.

However, it may occasionally happen that the inserted shunt capacitor moves the impedance in completely unexpected and undesired ways. This is almost always an indication that the reference plane was improperly extended for the measurement. The user should readjust the reference planes and attempt the shunt capacitor match with another calculated value.

When a differential impedance of 50 Ω (real part) is achieved, the board should be deenergized and another short placed on the board in preparation for resetting the port extensions to a new reference plane location. This short should be placed where next the series components are expected to be added, and it is important that both ports one and two be extended to this point on the board.

Another differential measurement must be taken at this point to establish the starting impedance value for the next matching component. Note that if 50 Ω PCB traces of finite length are used to connect pads, the impedance will experience an angular rotation to another location on the Smith Chart as indicated in Figure 20.

AD8343

Figure 20. Effect of 50 Ω PCB Trace on 50 Ω Real Impedance Load
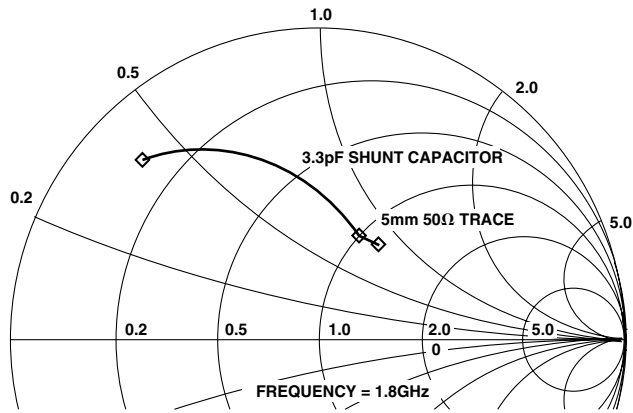
With the reference plane extended to the location of the series matching components, it may now be necessary to readjust the shunt capacitance value to achieve the desired 50 Ω real impedance. However, this rotation will not be very noticeable if the board traces are fairly short or the application frequency is low.

As before, calculate the series capacitance value required to move in the direction shown as step two in Figure 19, choose the nearest standard component remembering to perform the differential conversion, and install on the board. Again, if any unexpected impedance transformations occur the reference planes were probably extended incorrectly making it necessary to readjust these planes.

This value of series capacitance should be adjusted to obtain the desired value of differential impedance.

The above steps may be applied to any of the previously discussed matching topologies suitable for the AD8343. Also, if a non-50 Ω target impedance is required, simply calculate and adjust the components to obtain the desired load impedance.

Caution: If the matching network topology requires a differential shunt inductor between the inputs, it may be necessary to place a series blocking capacitor of low reactance in series with the inductor to avoid creating a low resistance dc path between the input terminals of the AD8343. Failure to heed this warning will result in very poor LO-output isolation

Step 5:   Transfer the Matching Network to the Final Design
On the "B" side of the AD8343 evaluation board, install the matching network and the input balun. Install the same output network as used for the work on the "A" side, then power up the board and measure the input return loss at the RF input connector on the board. Strictly speaking, the above procedure (if carried out accurately) for matching the AD8343 will obtain the best conversion gain; this *may* differ materially from the condition which results in best return loss at the board's input if the balun is lossy.

If the result is not as expected, the balun is probably producing an unexpected impedance transformation. If the performance is extremely far from the desired result and it was assumed that the output impedance of the balun was 50 Ω, it may be necessary to measure the output impedance of the balun in question. The design process should be repeated using the balun's output impedance instead of 50 Ω as the target. However, if the perfor-

mance is close to the desired result it should be possible to "tweak" the values of the matching network to achieve a satisfactory outcome. These changes should begin with a change from one standard value to the adjacent standard value. With these minor modifications to the matching network, one is able to evaluate the trend required to reach the desired result.

If the result is unsatisfactory and an acceptable compromise cannot be reached by further adjustment of the matching network, there are two options: obtain a better balun, or attempt a simultaneous conjugate match to both ports of the balun. Accomplishing the latter (or even evaluating the prospects for useful improvement) requires obtaining full two-port single-ended-to-differential S parameters for the balun, which requires the use of the ATN 4000 or similar multiport network analyzer test set. Gonzalez presents formulas for calculating the simultaneous conjugate match in the section entitled, "Simultaneous Conjugate Match: Bilateral Case" in his book, "Microwave Transistor Amplifiers."

At higher frequencies the measurement process described above becomes increasingly corrupted by unaccounted for impedance transformations occurring in the traces and pads between the input connectors and the extended reference plane. One approach to dealing with this problem is to access the desired measurement points by soldering down semirigid coax cables that have been connected to the VNA and directly calibrated at the free ends.

APPLICATIONS
Downconverting Mixer
A typical downconversion application is shown in Figure 21 with the AD8343 connected as a receive mixer. The input single-ended-to-differential conversion is obtained through the use of a 1:1 transmission line balun. The input matching network is positioned between the balun and the input pins, while the output is taken directly from a 4:1 impedance ratio (2:1 turns ratio) transformer. The local oscillator signal at a level of −12 dBm to −3 dBm is brought in through a second 1:1 balun.
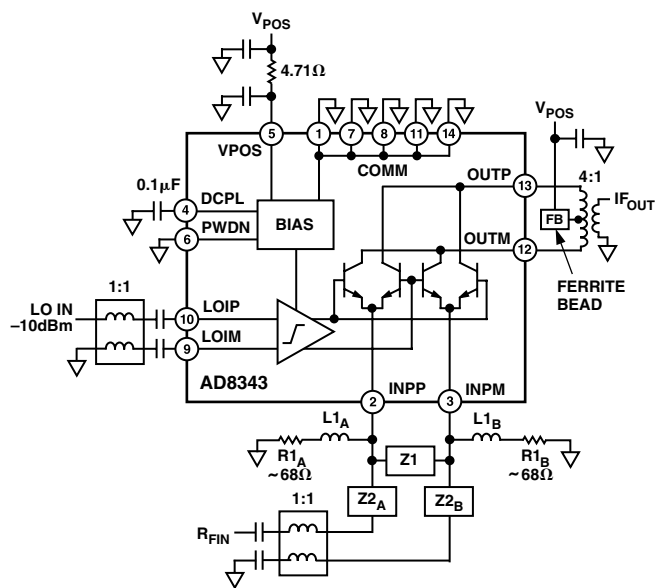

Figure 21. Typical Downconversion Application

R1A and R1B set the core bias current of 18.5 mA per side. L1A and L1B provide the RF choking required to avoid shunting the signal. Z1, Z2A, and Z2B comprise a typical input matching network that is designed to match the AD8343's differential input impedance to the differential output impedance of the balun.

The IF output is taken through a 4:1 (impedance ratio) transformer that reflects a 200 Ω differential load to the collectors. This output coupling arrangement is reasonably broadband, although in some cases the user might want to consider adding a resonator tank circuit between the collectors to provide a measure of IF selectivity. The ferrite bead (FB), in series with the output transformer's center tap, addresses the common-mode stability concern.

In this circuit the PWDN pin is shown connected to GND, which enables the mixer. In order to enter power-down mode and conserve power, the PWDN pin should be taken within 500 mV of VPOS.

The DCPL pin should be bypassed to GND with about 0.1 μF. Failure to do so could result in a higher noise level at the output of the device.

Upconverting Mixer
A typical upconversion application is shown in Figure 22. Both the input and output single-ended-to-differential conversions are obtained through the use of 1:1 transmission line baluns. The differential input and output matching networks are designed between the balun and the I/O pins of the AD8343. The local oscillator signal at a level of –12 dBm to –3 dBm is brought in through a third 1:1 balun.

R1A and R1B set the core bias current of 18.5 mA per side. Z1, Z2A, and Z2B comprise a typical input matching network that is designed to match the AD8343's differential input impedance to the differential output impedance of the balun. It was assumed for this example that the input frequency is low and that the magnitude of the device's input impedance is therefore much smaller than the bias resistor values, allowing the input bias inductors to be eliminated with very little penalty in gain or noise performance.

In this example, the output signal is taken via a differential matching network comprising Z3 and Z4A/B, then through the 1:1 balun and dc blocking capacitors to the single-ended output. The output frequency is assumed to be high enough that conjugate matching to the output of the AD8343 is desirable, so the goal of the matching network is to provide a conjugate match between the device's output and the differential input of the output balun.

This circuit uses shunt feed to provide collector bias for the transistors because the output balun in this circuit has no convenient center-tap. The ferrite beads, in series with the output's bias inductors, provide some small degree of damping to ease the common-mode stability problem. Unfortunately this type of output balun may present a common-mode load that enters the region of output instability, so most of the burden of avoiding overt instability falls on the input circuit, which should present an inductive common-mode termination over as broad a band of frequencies as possible.

The PWDN pin is shown as tied to GND, which enables the mixer. The DCPL pin should be bypassed to GND with about 0.1 μF in order to bypass noise from the internal bias circuit.
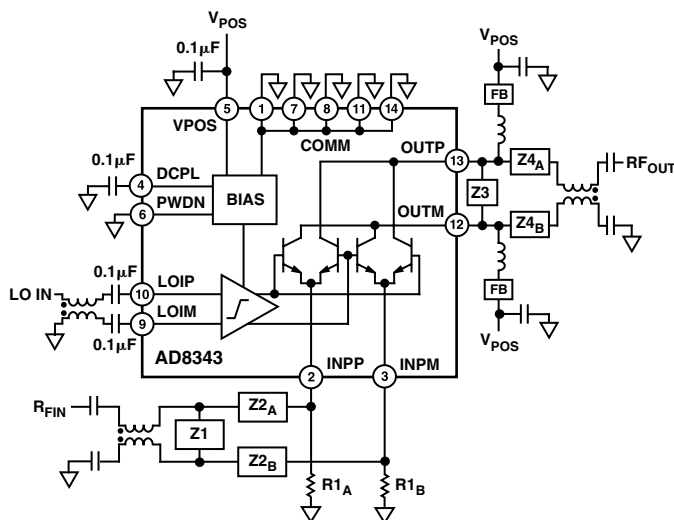

Figure 22. Typical Upconversion Application

AD8343

EVALUATION BOARD

The AD8343 Evaluation Board has two independent areas, denoted A and B. The circuit schematics are shown in Figures 23 and 24. An assembly drawing is included in Figure 25 to ease identification of components, and representations of the board layout are included in Figures 26 through 29.

The A region is configured for ease in making device impedance measurements as part of the process of developing suitable matching networks for a final application. The B region is designed for operating the AD8343 in a single-ended application environment and therefore includes pads for attaching baluns or transformers at both the input and output.

The following Tables (III through V) delineate the components used for the characterization procedure used to generate TPC 1 through 42 and most other data contained in this data sheet. Table III lists the support components that are delivered with the AD8343 evaluation board. Note that the board is shipped without any frequency specific components installed. Table IV lists the components used to obtain the frequency selection necessary for the product receiver evaluation, and Table V lists the transmitter evaluation components.

Table III. Values of Support Components Shipped with Evaluation Board and Used for Device Characterization

Component Designator	Value	Qty.	Part Number
C1A, C1B, C3A, C3B, C11A, C11B	0.1 μF	6	Murata GRM40Z5U104M50V
C2A, C2B, C4A, C4B, C5A, C5B, C6A, C6B, C9A, C9B, C10A, C10B, C12A, C12B, C13A, C13B	0.01 μF	16	Murata GRM40X7R103K50V
R3A, R3B, R4A, R4B	68.1 Ω ± 1%	4	Panasonic ERJ6ENF68R1V (T and R Packaging)
R1A, R1B, R2A, R2B	3.9 Ω ± 5%	4	Panasonic ERJ6GEYJ3R9V (T and R Packaging)
R5A, R5B	0 Ω	2	Panasonic ERJ6GEYJR00V (T and R Packaging)
J1A, J1B	Ferrite Bead	2	Murata BLM21P300S (2.0 mm SMT)
T1A, T1B, T2B (Various)	1:1	3	M/A-Com ETC1-1-13 Wideband Balun*
T3B (Various)	4:1	1	Mini-Circuits TC4-1W Transformer
R6A, R6B, R7A, R7B	10 Ω ± 1%	4	Panasonic ERJ6GEYJ100V (T and R Packaging)
L1A, L1B, L2A, L2B	56 nH	4	Panasonic ELJ-RE56NJF3

Table IV. Values of Matching Components Used for Receiver Characterization

Component Designator	Value	Qty.	Part Number
f_{IN} = 400 MHz, f_{OUT} = 70 MHz			
T1B, T2B	1:1	2	M/A-Com ETC1-1-13 Wideband Balun[1]
T3B	4:1	1	Mini-Circuits TC4-1W Transformer
R6B, R7B	10 Ω	2	Panasonic ERJ6GEYJ100V (T and R Packaging)
Z1B, Z3B	jumper	2	#30 AWG Wire Across Pads
Z2B	8.2 pF	1	Murata MA188R2J
Z5B, Z7B	150 nH	2	Murata LQW1608AR15G00
Z6B	3.4 pF	1	Murata MA182R4B ‖ MA181R0B
L1B, L2B	56 nH	2	Panasonic ELJ-RE56NJF3
Z4B, Z8B, L3B, L4B, R9B — Not Populated			
f_{IN} = 900 MHz, f_{OUT} = 170 MHz			
T1B, T2B	1:1	2	M/A-Com ETC1-1-13 Wideband Balun[1]
T3B	4:1	1	Mini-Circuits TC4-1W Transformer
R6B, R7B	10 Ω	2	Panasonic ERJ6GEYJ100V (T and R packaging)
Z1B, Z3B	jumper	2	#30 AWG Wire Across Pads
Z4B	3.0 pF	1	Murata GRM39C0G3R0B50V
Z5B, Z7B	120 nH	2	Murata LQW1608AR12G00
Z6B	0.4 pF	1	Murata MA180R4B
L1B, L2B	56 nH	2	Panasonic ELJ-RE56NJF3
Z2B, Z8B, L3B, L4B, R9B — Not Populated			
f_{IN} = 1900 MHz, f_{OUT} = 425 MHz			
T1B, T2B	1:1	3	M/A-Com ETC1-1-13 Wideband Balun[1]
T3B	4:1	1	Mini-Circuits TC4-1W Transformer
R6B, R7B	10 Ω	2	Panasonic ERJ6GEYJ100V (T and R packaging)
Z1B, Z3B	6.8 nH	2	Murata LQW1608A6N8C00
Z2B	0.6 pF	1	Murata MA180R6B
Z5B, Z7B	39 nH	2	Murata LQW1608A39NG00
Z8B	2.0 pF	1	Murata MA182R0B
L1B, L2B	56 nH	2	Panasonic ELJ-RE56NJF3
Z6B, Z4B, L3B, L4B, R9B — Not Populated			

Table IV. Values of Matching Components Used for Receiver Characterization (Continued)

Component Designator	Value	Qty.	Part Number
f_{IN} = 1900 MHz, f_{OUT} = 170 MHz			
T1B, T2B	1:1	2	M/A-Com ETC1-1-13 Wideband Balun[1]
T3B	4:1	1	Mini-Circuits TC4-1W Transformer
R6B, R7B	10 Ω	2	Panasonic ERJ6GEYJ100V (T and R Packaging)
Z1B, Z3B	6.8 nH	2	Murata LQW1608A6N8C00
Z4B	0.5 pF	1	Murata MA180R5B
Z5B, Z7B	100 nH	2	Murata LQW1608AR10G00
Z6B	2.4 pF	1	Murata MA182R4B
L1B, L2B	56 nH	2	Panasonic ELJ-RE56NJF3
Z2B, Z8B, L3B, L4B, R9B — Not Populated			

**Table V. Values of Matching Components Used for Transmitter Characterization**

| Component Designator	Value	Qty.	Part Number
f_{IN} = 150 MHz, f_{OUT} = 900 MHz			
T1B, T3B	1:1	2	M/A-Com ETC1-1-13 Wideband Balun[1]
T2B	1:1	1	Mini-Circuits ADTL1-18-75
R6B, R7B	5.1 Ω	2	Panasonic ERJ6GEYJ510V (T and R Packaging)
Z1B, Z3B	8.2 nH	2	Murata LQW1608A8N2C00
Z2B	33 pF	1	Murata GRM39C0G330J100V
Z5B, Z7B	8.2 nH	2	Murata LQG11A8N2J00
Z8B	6.2 pF	1	Murata MA186R2C
L1B, L2B	56 nH	2	Panasonic ELJ-RE56NJF3
L3B, L4B	150 nH	2	Murata LQW1608AR15G00
Z4B, Z6B, R9B — Not Populated			
f_{IN} = 150 MHz, f_{OUT} = 1900 MHz			
T1B, T3B	1:1	2	M/A-Com ETC1-1-13 Wideband Balun[1]
T2B	1:1	1	Mini-Circuits ADTL1-18-75
R6B, R7B	5.1 Ω	2	Panasonic ERJ6GEYJ510V (T and R Packaging)
Z1B, Z3B	8.2 nH	2	Murata LQG11A8N2J00
Z2B	33 pF	1	Murata GRM39C0G330J100V
Z5B, Z7B	1.8 nH	2	Murata LQG11A1N8S00
Z8B	1.8 pF	1	Murata MA181R8B
L1B, L2B	56 nH	2	Panasonic ELJ-RE56NJF3
L3B, L4B	68 nH	2	Murata LQW1608A68NG00
Z4B, Z6B, R9B — Not Populated			

NOTES

[1]The ECT1-1-13 wideband balun was chosen for ease in customer's independent evaluation. These baluns are quite acceptable for use as T1 on the LO port, but may not be acceptable for use as T2 on the high performance RF input. It has been found that board to board performance variations become unacceptable when this balun is used at higher (> 500 MHz) frequencies. A narrow-band balun is suggested for this critical interface. Refer to the Device Interfaces and A Step-by-Step Approach to Impedance Matching section of this document for more information.

AD8343
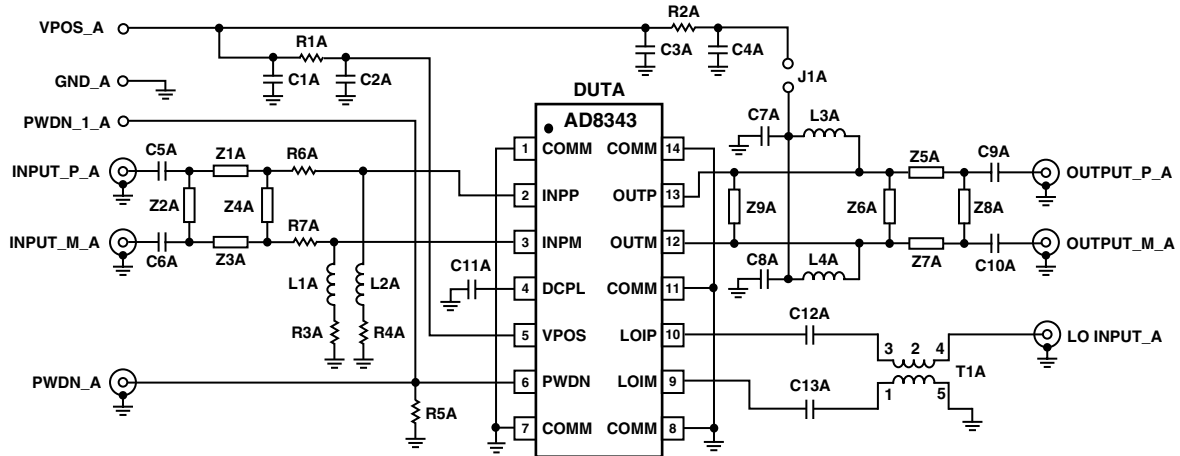
REFERENCE TABLE I FOR COMPONENT VALUES AS SHIPPED.
REFERENCE TABLE I, II, AND III FOR CHARACTERIZATION VALUES.

Figure 23. Characterization and Evaluation Board Circuit A
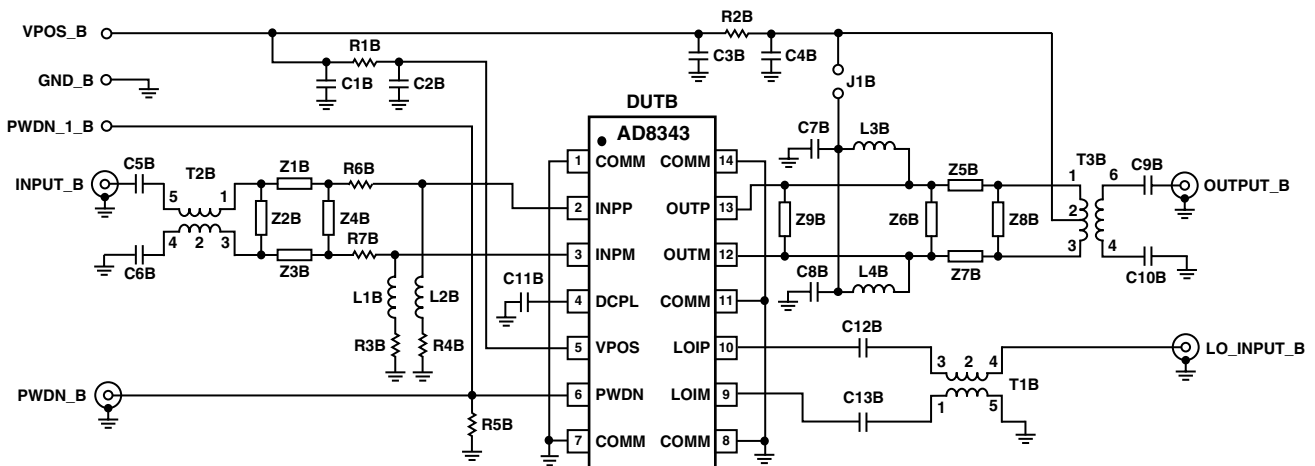
REFERENCE TABLE I FOR COMPONENT VALUES AS SHIPPED.
REFERENCE TABLE I, II, AND III FOR CHARACTERIZATION VALUES.

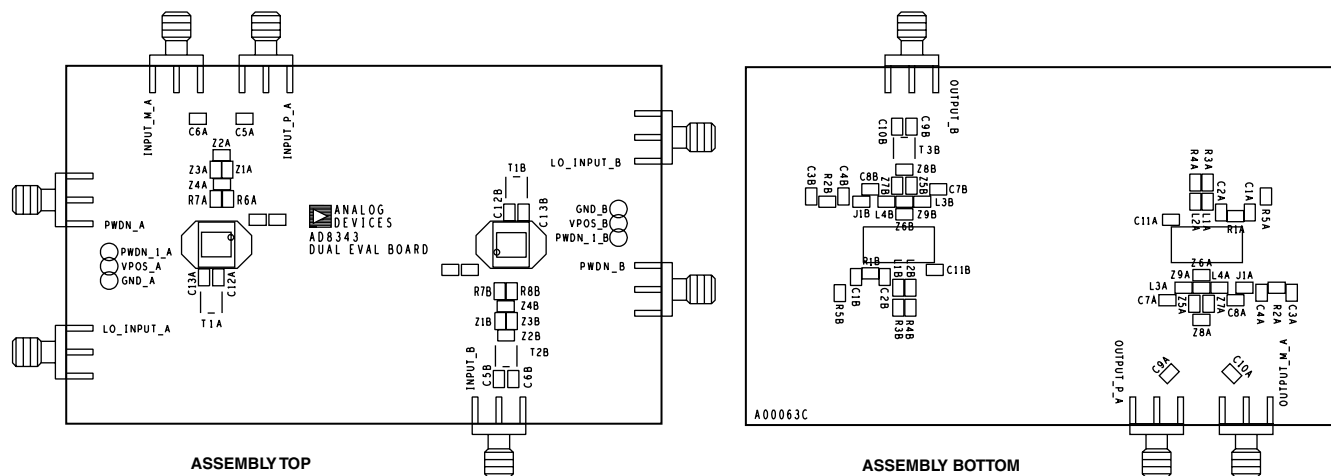*Figure 24. Characterization and Evaluation Board Circuit B*
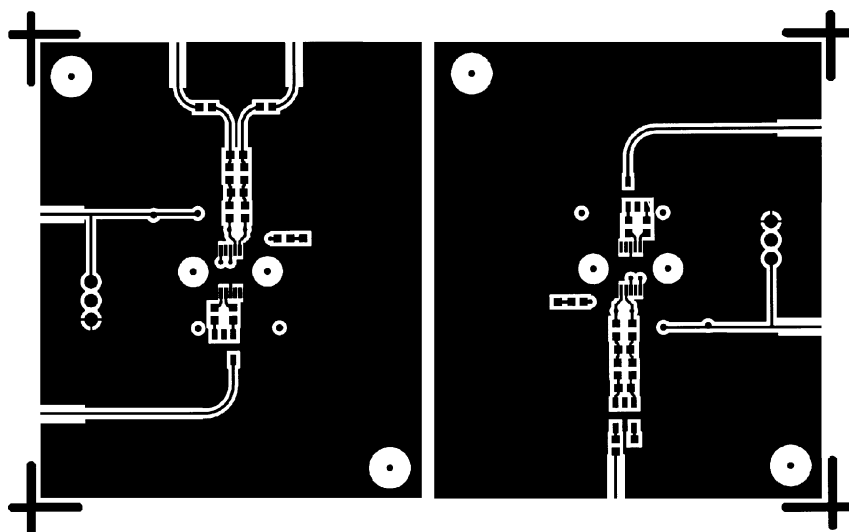
Figure 25. Evaluation Board Assembly Drawing
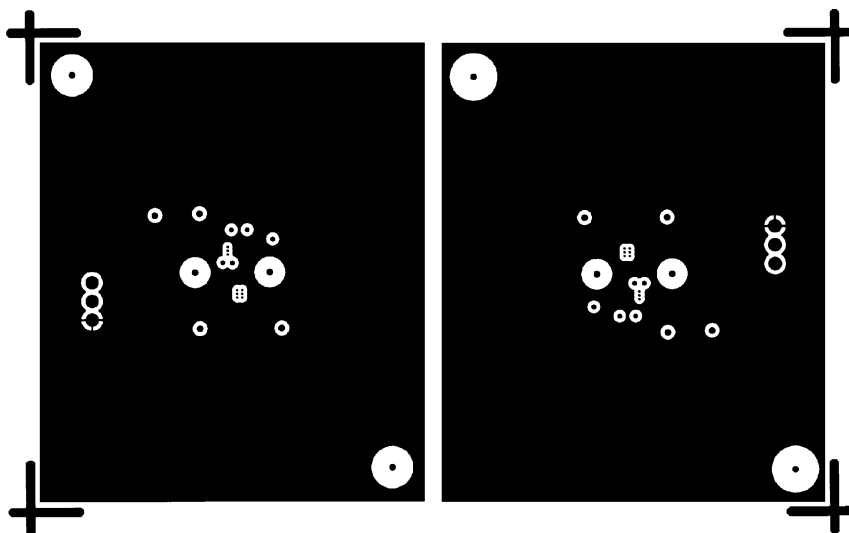

Figure 26. Evaluation Board Artwork Top

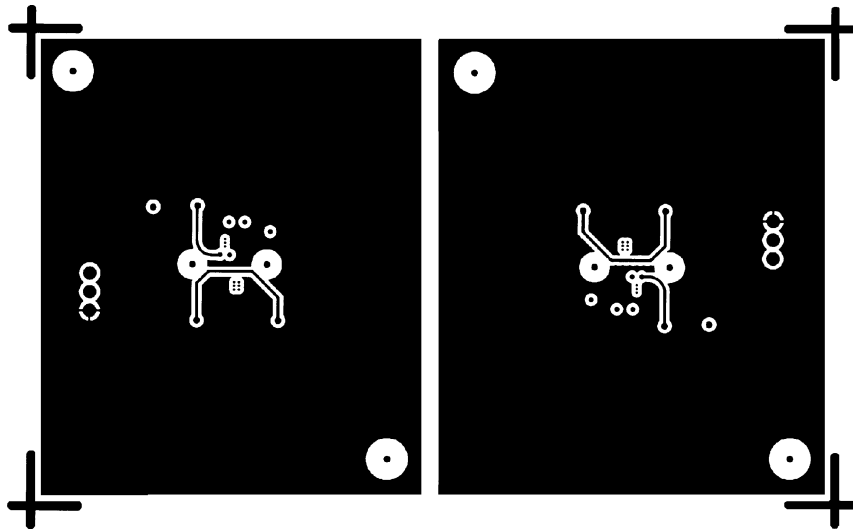*Figure 27. Evaluation Board Artwork Internal 1*

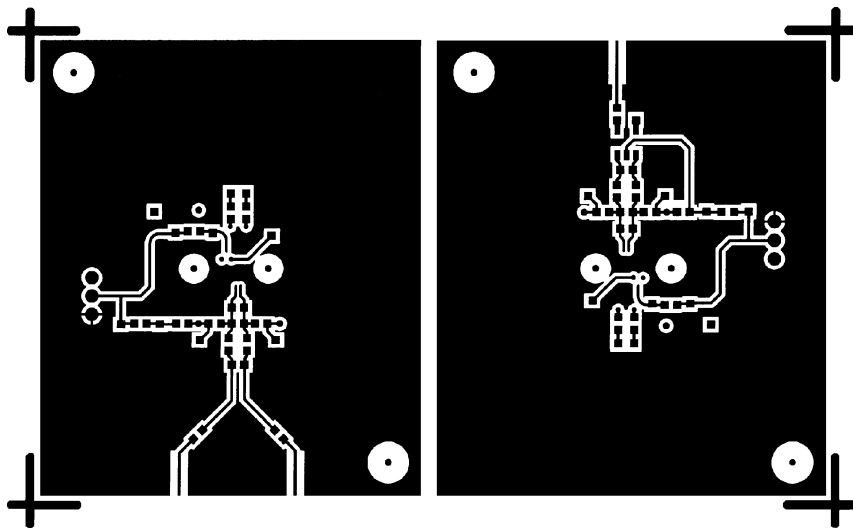*Figure 28. Evaluation Board Artwork Internal 2*
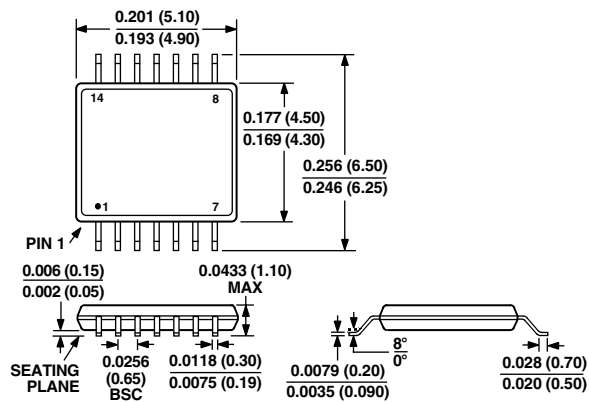

Figure 29. Evaluation Board Artwork Bottom

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

14-Lead Plastic Thin Shrink Small Outline Package (TSSOP)
RU-14