FM24C256

256Kb FRAM Serial Memory

Features

256Kbit Ferroelectric Nonvolatile RAM

- Organized as 32,768 x 8 bits
- High Endurance 10 Billion (10^{10}) Read/Writes
- 45 year Data Retention
- NoDelay™ Writes
- Advanced High-Reliability Ferroelectric Process

Fast Two-wire Serial Interface

- Up to 1 MHz Maximum Bus Frequency
- Supports Legacy Timing for 100 kHz & 400 kHz

Low Power Operation

- 5V Operation
- 200 µA Active Current (100 kHz)
- 100 µA Standby Current

Industry Standard Configuration

- Industrial Temperature -40° C to +85° C
- 8-pin "Green"/RoHS EIAJ SOIC Package

Description

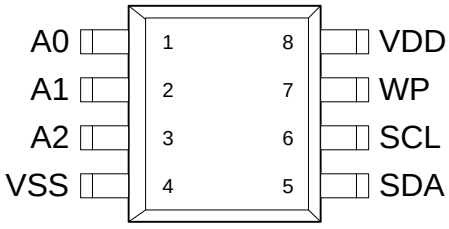
The FM24C256 is a 256-kilobit nonvolatile memory employing an advanced ferroelectric process. A ferroelectric random access memory or FRAM is nonvolatile and performs reads and writes like a RAM. It provides reliable data retention for 45 years while eliminating the complexities, overhead, and system level reliability problems caused by EEPROM and other nonvolatile memories.

The FM24C256 performs write operations at bus speed. No write delays are incurred. The next bus cycle may commence immediately without the need for data polling. In addition, the product offers write endurance orders of magnitude higher than EEPROM. Also, FRAM exhibits much lower power during writes than EEPROM since write operations do not require an internally elevated power supply voltage for write circuits.

These capabilities make the FM24C256 ideal for nonvolatile memory applications requiring frequent or rapid writes. Examples range from data collection where the number of write cycles may be critical, to demanding industrial controls where the long write time of EEPROM can cause data loss. The combination of features allows more frequent data writing with less overhead for the system.

The FM24C256 is available in an 8-pin EIAJ SOIC package using an industry standard two-wire protocol. Ramtron's "green" packages are RoHS compliant. Specifications are guaranteed over an industrial temperature range of -40°C to +85°C.

Pin Configuration



Pin Names	Function
A0-A2	Device Select Address
SDA	Serial Data/Address
SCL	Serial Clock
WP	Write Protect
VSS	Ground
VDD	Supply Voltage 5V

Ordering Information	
FM24C256-G	"Green"/RoHS 8-pin EIAJ SOIC

This product conforms specifications per the terms of the Ramtron standard warranty. The product has completed Ramtron's internal qualification testing and has reached production status.

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Rev. 3.2
May 2008

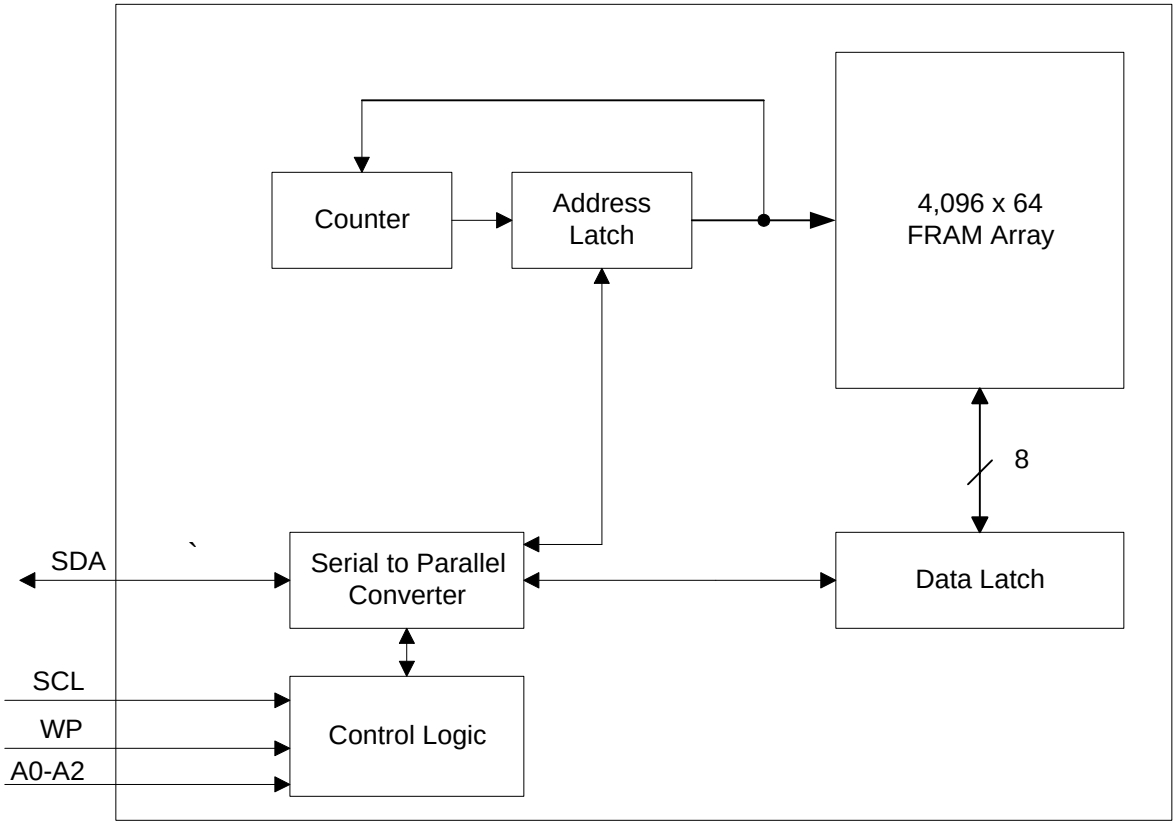


Figure 1. Block Diagram

Pin Description

Pin Name	Type	Pin Description
A0-A2	Input	Address 2-0: These pins are used to select one of up to 8 devices of the same type on the same two-wire bus. To select the device, the address value on the three pins must match the corresponding bits contained in the device address. The address pins are pulled down internally.
WP	Input	Write Protect: When WP is high, the entire array will be write-protected. When WP is low, all addresses may be written. This pin is internally pulled down.
SDA	I/O	Serial Data/Address: This is a bi-directional input used to shift serial data and addresses for the two-wire interface. It employs an open-drain output and is intended to be wire-OR'd with other devices on the two-wire bus. The input buffer incorporates a Schmitt trigger for improved noise immunity and the output driver has slope control for falling edges. An external pull-up resistor is required.
SCL	Input	Serial Clock: The serial clock input for the two-wire interface. Data is clocked out of the device on the SCL falling edge, and clocked in on the SCL rising edge. The SCL input also incorporates a Schmitt trigger input for improved noise immunity.
VDD	Supply	Supply Voltage: 5V
VSS	Supply	Ground

Overview

The FM24C256 is a serial FRAM memory. The memory array is logically organized as 32,768 x 8 bit memory array and is accessed using an industry standard two-wire interface. Functional operation of the FRAM is similar to serial EEPROMs. The major difference between the FM24C256 and a serial EEPROM relates to its superior write performance.

Memory Architecture

When accessing the FM24C256, the user addresses 32,768 locations each with 8 data bits. These data bits are shifted serially. The 32,768 addresses are accessed using the two-wire protocol, which includes a slave address (to distinguish from other non-memory devices), and an extended 16-bit address. Only the lower 15 bits are used by the decoder for accessing the memory. The upper address bit should be set to 0 for compatibility with higher density devices in the future.

The memory is read or written at the speed of the two-wire bus. Unlike an EEPROM, it is not necessary to poll the device for a ready condition since writes occur at bus speed. By the time a new bus transaction can be shifted into the part, a write operation is complete. This is explained in more detail in the interface section below.

Users can expect several obvious system benefits from the FM24C256 due to its fast write cycle and high endurance as compared with EEPROM. However there are less obvious benefits as well. For example in a high noise environment, the fast-write operation is less susceptible to corruption than an EEPROM since the write cycle is completed quickly. By contrast, an EEPROM requiring milliseconds to write is vulnerable to noise during much of the cycle.

Note that the FM24C256 contains no power management circuits other than a simple internal power-on reset. It is the user's responsibility to ensure that V_{DD} is maintained within data sheet tolerances to prevent incorrect operation.

Two-wire Interface

The FM24C256 employs a bi-directional two-wire bus protocol using few pins and little board space. Figure 2 illustrates a typical system configuration using the FM24C256 in a microcontroller-based system. The industry standard two-wire bus is familiar to many users but is described in this section.

By convention, any device that is sending data onto the bus is the transmitter while the target device for this data is the receiver. The device that is controlling the bus is the master. The master is responsible for generating the clock signal for all operations. Any device on the bus that is being controlled is a slave. The FM24C256 is always a slave device.

The bus protocol is controlled by transition states in the SDA and SCL signals. There are four conditions including Start, Stop, Data bit, and Acknowledge. Figure 3 illustrates the signal conditions that specify the four states. Detailed timing diagrams are shown in the Electrical Specifications section.

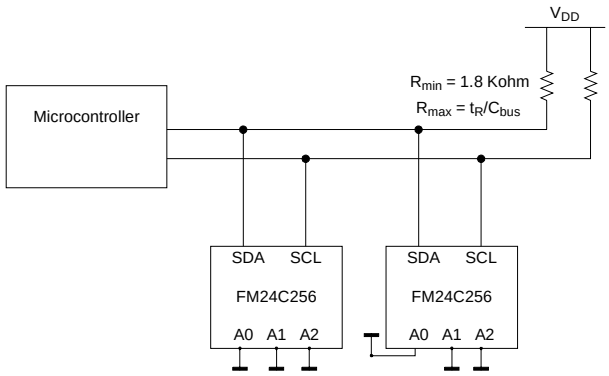


Figure 2. Typical System Configuration

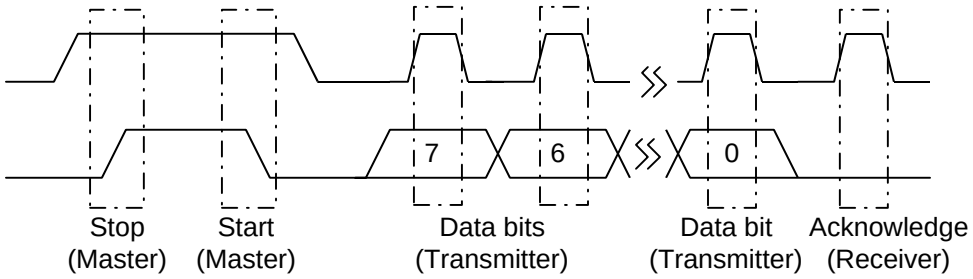


Figure 3. Data Transfer Protocol

Stop Condition

A Stop condition is indicated when the bus master drives SDA from low to high while the SCL signal is high. All operations using the FM24C256 must end with a Stop condition. If an operation is pending when a Stop is asserted, the operation will be aborted. The master must have control of SDA (not a memory read) in order to assert a Stop condition.

Start Condition

A Start condition is indicated when the bus master drives SDA from high to low while the SCL signal is high. All read and write transactions begin with a Start condition. An operation in progress can be aborted by asserting a Start condition at any time. Aborting an operation using the Start condition will ready the FM24C256 for a new operation.

If during operation the power supply drops below the specified VDD minimum, the system should issue a Start condition prior to performing another operation.

Data/Address Transfer

All data transfers (including addresses) take place while the SCL signal is high. Except under the two conditions described above, the SDA signal should not change while SCL is high.

Acknowledge

The Acknowledge takes place after the 8th data bit has been transferred in any transaction. During this state the transmitter should release the SDA bus to allow the receiver to drive it. The receiver drives the SDA signal low to acknowledge receipt of the byte. If the receiver does not drive SDA low, the condition is a No-Acknowledge and the operation is aborted.

The receiver would fail to acknowledge for two distinct reasons. First is that a byte transfer fails. In this case, the No-Acknowledge ends the current operation so that the part can be addressed again. This allows the last byte to be recovered in the event of a communication error.

Second and most common, the receiver does not acknowledge to deliberately end an operation. For example, during a read operation, the FM24C256 will continue to place data onto the bus as long as the receiver sends Acknowledges (and clocks). When a read operation is complete and no more data is needed, the receiver must not acknowledge the last byte. If the receiver acknowledges the last byte, this will cause the FM24C256 to attempt to drive the bus on the next clock while the master is sending a new command such as Stop.

Slave Address

The first byte that the FM24C256 expects after a Start condition is the slave address. As shown in Figure 4, the slave address contains the Slave ID (device type), the device select address bits, and a bit that specifies if the transaction is a read or a write. Bits 7-4 define the device type and must be set to 1010b for the FM24C256. These bits allow other types of function types to reside on the 2-wire bus within an identical address range. Bits 3-1 are the device select bits which are equivalent to chip select bits. They must match the corresponding value on the external address pins to select the device. Up to eight FM24C256 devices can reside on the same two-wire bus by assigning a different address to each. Bit 0 is the read/write bit. A 1 indicates a read operation, and a 0 indicates a write.

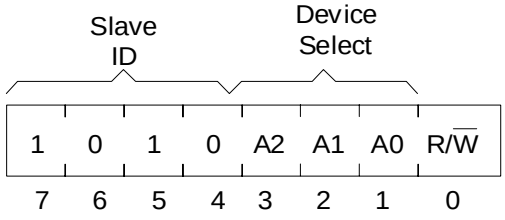


Figure 4. Slave Address

Addressing Overview

After the FM24C256 (as receiver) acknowledges the device address, the master can place the memory address on the bus for a write operation. The address requires two bytes. The first is the MSB (upper byte). Since the device uses only 15 address bits, the value of the upper bits is a "don't care". Following the MSB is the LSB (lower byte) with the remaining eight address bits. The address value is latched internally. Each access causes the latched address value to be incremented automatically. The current address is the value that is held in the latch, either a newly written value or the address following the last access. The current address will be held as long as power remains or until a new value is written. Reads always use the current address. A random read address can be loaded by beginning a write operation as explained below.

After transmission of each data byte, just prior to the acknowledge, the FM24C256 increments the internal address latch. This allows the next sequential byte to be accessed with no additional addressing externally. After the last address (7FFFh) is reached, the address latch will roll over to 0000h. There is no limit to the number of bytes that can be accessed with a single read or write operation.

Data Transfer

After the address information has been transmitted, data transfer between the bus master and the FM24C256 can begin. For a read operation the FM24C256 will place 8 data bits on the bus then wait for an Acknowledge from the master. If the Acknowledge occurs, the FM24C256 will transfer the next sequential byte. If the Acknowledge is not sent, the FM24C256 will end the read operation. For a write operation, the FM24C256 will accept 8 data bits from the master then send an acknowledge. All data transfer occurs MSB (most significant bit) first.

Memory Operation

The FM24C256 is designed to operate in a manner very similar to other 2-wire interface memory products. The major differences result from the higher performance write capability of FRAM technology. These improvements result in some differences between the FM24C256 and a similar configuration EEPROM during writes. The complete operation for both writes and reads is explained below.

Write Operation

All writes begin with a device address, then a memory address. The bus master indicates a write operation by setting the LSB of the device address to a 0. After addressing, the bus master sends each byte of data to the memory and the memory generates an acknowledge condition. Any number of sequential bytes may be written. If the end of the address range is reached internally, the address counter will wrap from 7FFFh to 0000h.

Unlike other nonvolatile memory technologies, there is essentially no write delay with FRAM. Since the read and write access times of the underlying memory are the same, the user experiences no delay on the bus. The entire memory cycle occurs in less time than a single bus clock. Therefore, any operation including a read or write can occur immediately following a write. Acknowledge polling, a technique used with EEPROMs to determine if a write has completed is unnecessary and will always return a ready condition.

Internally, an actual memory write occurs after the 8th data bit is transferred. It will be complete before the Acknowledge is sent. Therefore, if the user desires to abort a write without altering the memory contents, this should be done using a Start or Stop condition prior to the 8th data bit. The FM24C256 uses no page buffering.

The memory array can be write protected using the WP pin. Pulling the WP pin high will write-protect all addresses. The FM24C256 will not acknowledge data bytes that are written when WP is active. In addition, the address counter will not increment if writes are attempted to these addresses. Setting WP low will deactivate this feature. WP is internally pulled down. The state of WP should remain stable from the Start command until the address is complete.

Figure 5 and 6 below illustrate both a single-byte and multiple-write.

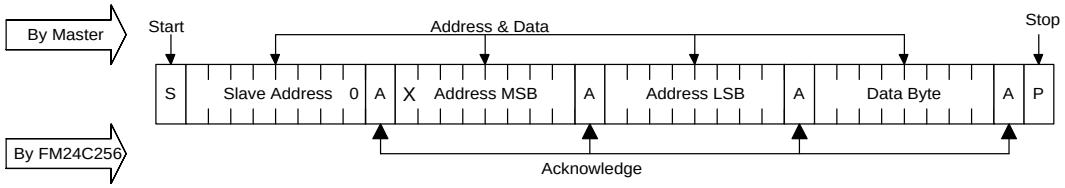


Figure 5. Single Byte Write

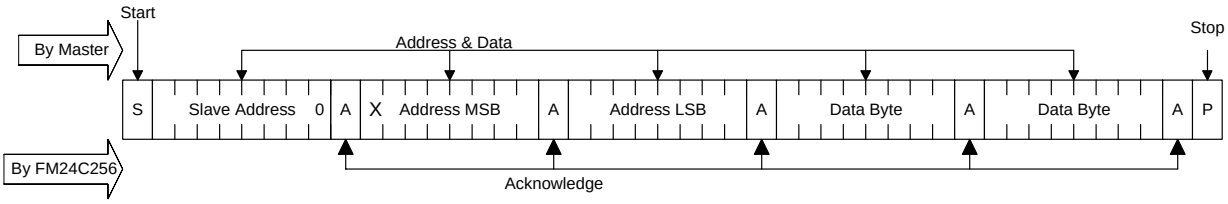


Figure 6. Multiple Byte Write

Read Operation

There are two types of read operations. They are current address read and selective address read. In a current address read, the FM24C256 uses the internal address latch to supply the address. In a selective read, the user performs a procedure to set the address to a specific value.

Current Address & Sequential Read

As mentioned above the FM24C256 uses an internal latch to supply the address for a read operation. A current address read uses the existing value in the address latch as a starting place for the read operation. The system reads from the address immediately following that of the last operation.

To perform a current address read, the bus master supplies a device address with the LSB set to 1. This indicates that a read operation is requested. After receiving the complete device address, the FM24C256 will begin shifting out data from the current address on the next clock. The current address is the value held in the internal address latch.

Beginning with the current address, the bus master can read any number of bytes. Thus, a sequential read is simply a current address read with multiple byte transfers. After each byte, the internal address counter will be incremented.

Each time the bus master acknowledges a byte, this indicates that the FM24C256 should read out the next sequential byte.

There are four ways to properly terminate a read operation. Failing to properly terminate the read will most likely create a bus contention as the FM24C256 attempts to read out additional data onto the bus. The four valid methods are as follows.

1. The bus master issues a no-acknowledge in the 9th clock cycle and a stop in the 10th clock cycle. This is illustrated in the diagrams below. This is preferred.
2. The bus master issues a no-acknowledge in the 9th clock cycle and a start in the 10th.
3. The bus master issues a stop in the 9th clock cycle.
4. The bus master issues a start in the 9th clock cycle.

If the internal address reaches 7FFFh, it will wrap around to 0000h on the next read cycle. Figures 7 and 8 show the proper operation for current address reads.

Selective (Random) Read

There is a simple technique that allows a user to select a random address location as the starting point for a read operation. This involves using the first three bytes of a write operation to set the internal address followed by subsequent read operations.

To perform a selective read, the bus master sends out the device address with the lsb set to 0. This specifies a write operation. According to the write protocol, the bus master then sends the address bytes that are loaded into the internal address latch. After the FM24C256 acknowledges the address, the bus master issues a Start condition. This simultaneously aborts the write operation and allows the read command to be issued with the device address LSB set to a 1. The operation is now a current address read.

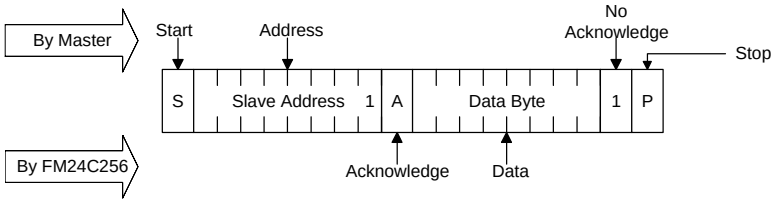


Figure 7. Current Address Read

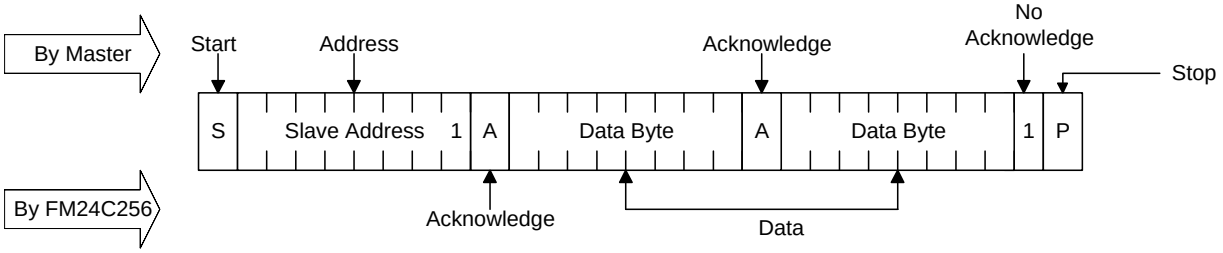


Figure 8. Sequential Read

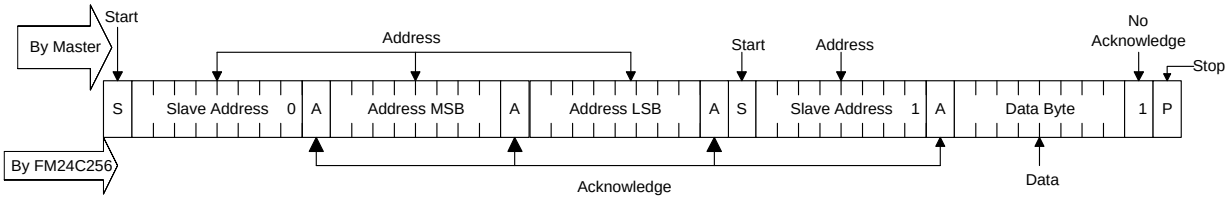


Figure 9. Selective (Random) Read

Endurance

A FRAM internally operates with a read and restore mechanism. Therefore, endurance cycles are applied for each read and write access. The FRAM architecture is based on an array of rows and columns. Rows (A14-A6) are subdivided into 8 segments (A5-A3). Each access causes an endurance cycle for a row segment. In the FM24C256, there are 8 bytes per segment. Endurance can be optimized by ensuring frequently accessed data is located in different segments. Regardless, FRAM read and write endurance is effectively unlimited at the 1MHz two-wire speed. Even at 30 accesses per second to the same segment, 10 years time will elapse before 10 billion endurance cycles occur.

Electrical Specifications

Absolute Maximum Ratings

Symbol	Description	Ratings
V_{DD}	Voltage on V_{DD} with respect to V_{SS}	-1.0V to +7.0V
V_{IN}	Voltage on any signal pin with respect to V_{SS}	-1.0V to +7.0V and $V_{IN} < V_{DD}$+1.0V *
T_{STG}	Storage Temperature	-55°C to + 125°C
T_{LEAD}	Lead temperature (Soldering, 10 seconds)	300° C
V_{ESD}	Electrostatic Discharge Voltage - Human Body Model (JEDEC Std JESD22-A114-B) - Machine Model (JEDEC Std JESD22-A115-A)	 4kV 400V
	Package Moisture Sensitivity Level	MSL-1

* Exception: The "$V_{IN} < V_{DD}$+1.0V" restriction does not apply to the SCL and SDA inputs.
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

DC Operating Conditions (T_A = -40° C to + 85° C, V_{DD} = 4.5V to 5.5V unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{DD}	Main Power Supply	4.5	5.0	5.5	V	
I_{DD}	VDD Supply Current @ SCL = 100 kHz @ SCL = 400 kHz @ SCL = 1 MHz			 200 500 1.2	 µA µA mA	1
I_{SB}	Standby Current			100	µA	2
I_{LI}	Input Leakage Current			10	µA	3
I_{LO}	Output Leakage Current			10	µA	3
V_{IH}	Input High Voltage	0.7 V_{DD}		V_{DD} + 0.5	V	4
V_{IL}	Input Low Voltage	-0.3		0.3 V_{DD}	V	4
V_{OL}	Output Low Voltage @ I_{OL} = 3 mA			0.4	V	
R_{IN}	Address Input Resistance (WP, A2-A0) For $V_{IN} = V_{IL}$ (max) For $V_{IN} = V_{IH}$ (min)	 20 1			 KΩ MΩ	5
V_{HYS}	Input Hysteresis	0.05 V_{DD}			V	4

Notes
1. SCL toggling between V_{DD}-0.3V and V_{SS}, other inputs V_{SS} or V_{DD}-0.3V
2. SCL = SDA = V_{DD}. All inputs V_{SS} or V_{DD}. Stop command issued.
3. V_{IN} or $V_{OUT} = V_{SS}$ to V_{DD}. Does not apply to WP, A2-A0 pins.
4. This parameter is characterized but not tested.
5. The input pull-down circuit is strong (20KΩ) when the input voltage is below V_{IL} and weak (1MΩ) when the input voltage is above V_{IH}. This resistance is characterized and not tested.

AC Parameters (T_A = -40° C to + 85° C, V_{DD} = 4.5V to 5.5V, C_L = 100 pF unless otherwise specified)

Symbol	Parameter	Min	Max	Min	Max	Min	Max	Units	Notes
f_{SCL}	SCL Clock Frequency	0	100	0	400	0	1000	kHz	
t_{LOW}	Clock Low Period	4.7		1.3		0.6		µs	
t_{HIGH}	Clock High Period	4.0		0.6		0.4		µs	
t_{AA}	SCL Low to SDA Data Out Valid		3		0.9		0.55	µs	
t_{BUF}	Bus Free Before New Transmission	4.7		1.3		0.5		µs	
$t_{HD:STA}$	Start Condition Hold Time	4.0		0.6		0.25		µs	
$t_{SU:STA}$	Start Condition Setup for Repeated Start	4.7		0.6		0.25		µs	
$t_{HD:DAT}$	Data In Hold	0		0		0		ns	
$t_{SU:DAT}$	Data In Setup	250		100		100		ns	
t_R	Input Rise Time		1000		300		300	ns	1
t_F	Input Fall Time		300		300		100	ns	1
$t_{SU:STO}$	Stop Condition Setup	4.0		0.6		0.25		µs	
t_{DH}	Data Output Hold (from SCL @ VIL)	0		0		0		ns	
t_{SP}	Noise Suppression Time Constant on SCL, SDA		50		50		50	ns	

Notes : All SCL specifications as well as start and stop conditions apply to both read and write operations.

1 This parameter is periodically sampled and not 100% tested.

Capacitance (T_A = 25° C, f=1.0 MHz, V_{DD} = 5V)

Symbol	Parameter	Max	Units	Notes
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	1
C_{IN}	Input Capacitance	6	pF	1

Notes

1 This parameter is periodically sampled and not 100% tested.

AC Test Conditions

Input Pulse Levels	0.1 V_{DD} to 0.9 V_{DD}
Input rise and fall times	10 ns
Input and output timing levels	0.5 V_{DD}

Equivalent AC Load Circuit

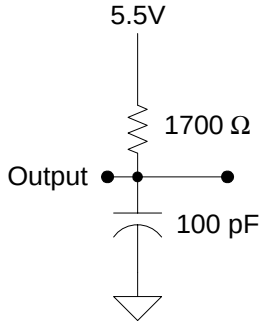
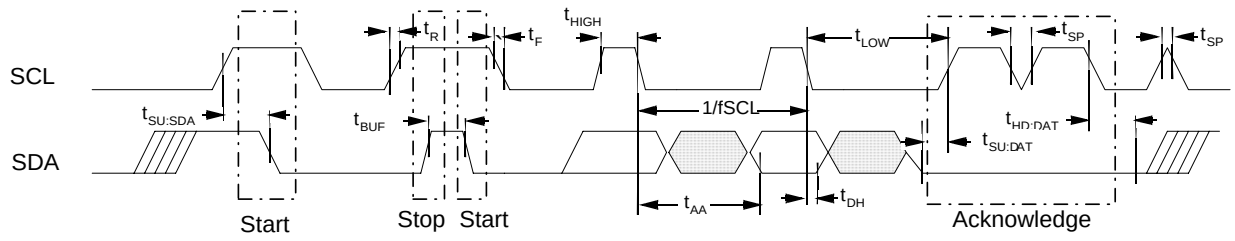


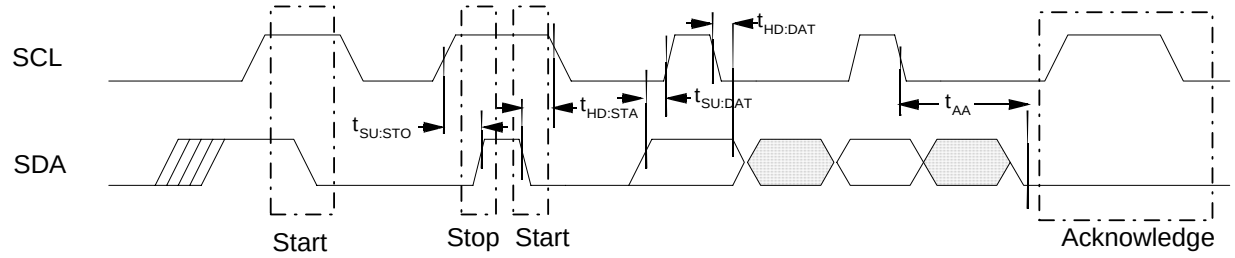
Diagram Notes

All start and stop timing parameters apply to both read and write cycles. Clock specifications are identical for read and write cycles. Write timing parameters apply to slave address, word address, and write data bits. Functional relationships are illustrated in the relevant data sheet sections. These diagrams illustrate the timing parameters only.

Read Bus Timing



Write Bus Timing

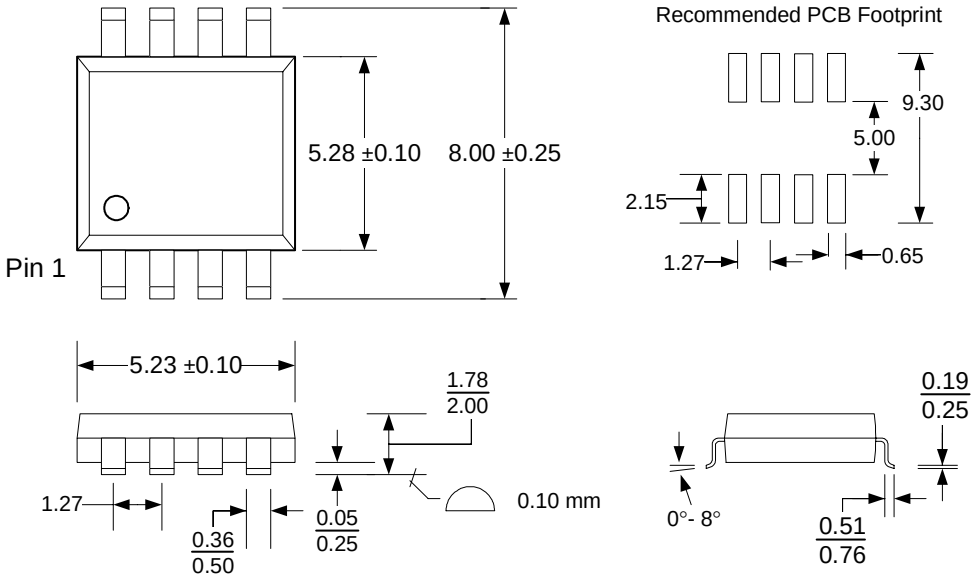


Data Retention (V_{DD} = 4.5V to 5.5V, +85° C)

Parameter	Min	Units	Notes
Data Retention	45	Years	

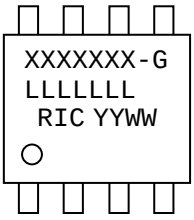
Mechanical Drawing

8-pin EIAJ SOIC



All dimensions in millimeters.

EIAJ SOIC Package Marking Scheme



Legend:
XXXXXX= part number
LLLLLLL= lot code
RIC=Ramtron Int'l Corp, YY=year, WW=work week

FM24C256, "Green" EIAJ SOIC package, Year 2004, Work Week 50
FM24C256-G
A40003S1
RIC 0450

Revision History

Revision	Date	Summary
1.0	4/10/01	Initial Release
1.1	9/28/01	Changed Idd and Isb specifications. Changed test load to 1700 ohms to reflect 3mA V_{OL} test condition.
1.2	1/31/02	Updated package drawing and dimensions. Rewrote description of the internal memory architecture and endurance section.
1.3	2/3/04	Added "part marking" note to Ordering Information (pg 1).
3.0	2/16/05	Added "green" packaging option. Added ESD and package MSL ratings. Changed storage temperature. New rev. number and 1st page footer to comply with updated scheme. Changed Data Retention spec.
3.1	5/5/05	Clarified Package Marking Scheme text and drawings.
3.2	5/27/2008	Removed –SE option from ordering information.